SIEMENS

ICs for Communications

Two Channel Codec Filter for Terminal Applications SICOFI®2-TE

PSB 2132 Version 1.2

Four Channel Codec Filter for Terminal Applications SICOFI®4-TE

PSB 2134 Version 1.2

Data Sheet 09.97

PSB 2132 Revision History:		Current Version: 09.97
Previous Version:		Preliminary Data Sheet 02.97
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
		Feature list updated

Edition 09.97

This edition was realized using the software system FrameMaker®.

Published by Siemens AG,
HL TS,
Balanstraße 73,
81541 München

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1 Overview

The Signal Processing Codec Filter for terminal applications PSB 2132/4 SICOFI2/4-TE is a special derivative of the SIEMENS programmable codec-filter-IC family designed for terminal applications featuring two or four POTS interfaces.

It can be directly connected to the IOM-2 interface in terminal mode running at 1.536 MHz clock rate. PCM data is transfered using the bit clock signal at 768 kHz.

Programming of internal registers is done via the serial microcontroller interface.

Only two external capacitors per channel are needed to complete the functionality of the PSB 2132/4. The internal level accuracy is based on a very accurate bandgap reference. The frequency behaviour is mainly determined by digital filters, which do not have any fluctuations. As a result of the new ADC- and DAC- concepts linearity is only limited by second order parasitic effects. Although the device works only from one single 5 V supply there is a very good dynamic range available.

The PSB 2132/4 is a DSP based codec which allows the integration of filters and tone generators besides the regular A- or u-law conversion. In addition it integrates I/O extentions to the microcontroller and provides the necessary I/O pins to control the SLIC or discrete SLIC replacement. Interrupts are generated to the microcontroller if changes (e.g. Off-Hook detection) have been occured. The PSB 2132/4 provides a ring frequency output pin. This pin has a programmable clock frequency to meet the European and US ringing frequency requirements using only one external divider.

The IOM-2 data lines DU and DD can both be used for transmitting or receiving voice data. The position of each receive and transmit timeslot is programmable. Internal communication between analog ports is supported by programming each channel to the same timeslot but reversing the data lines. Thus the transmitted PCM data is transmitted by one port and received by the second port via the same timeslot. An additional IC for switch matrix is eliminated.

The PSB 2132/4 is specially of interest for applications, which need to serve different country specific characteristics on the POTS interface. Since all filters are programmable, adaptation to these country specific requirements may be done only by software parameters using the same hardware.

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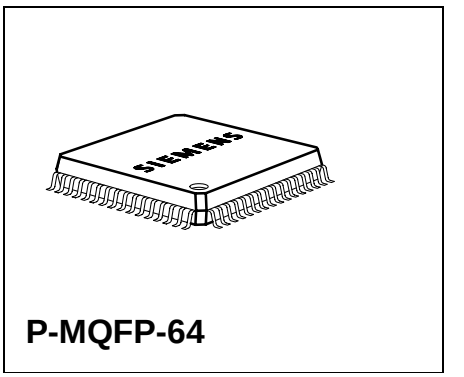
Two Channel Codec Filter for Terminal Applications SICOFI®2-TE **PSB 2132**

Four Channel Codec Filter for Terminal Applications SICOFI®4-TE **PSB 2134**

Preliminary Data **CMOS**

1.1 Features

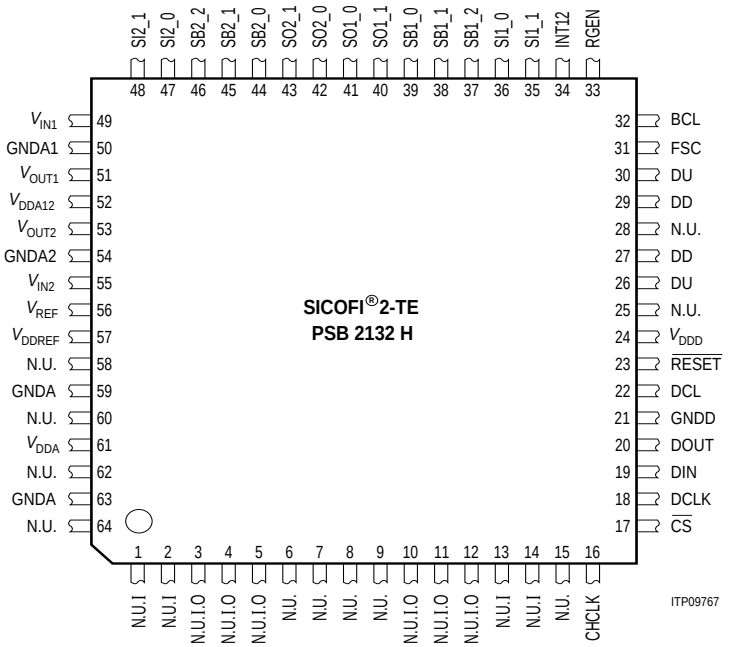


P-MQFP-64

- Single chip programmable CODEC and FILTER to handle two or four POTS interfaces
- IOM-2 compatible interface (1.536 MHz DCL, 768 kHz Bit clock)
- Internal communication between POTS interfaces
- Programmable I/O lines for signaling information per channel
- Programmable ring generator output
- Two programmable tone generators per channel
- Serial microcontroller interface
- Digital signal processing technique
- High analog driving capability (300 Ω) for direct driving of transformers
- Programmable digital filters to adapt the transmission behaviour especially for
  - AC impedance matching
  - transhybrid balancing
  - frequency response
  - gain
  - A/μ-law conversion
- Single 5 V power supply
- Low power 0.9 μm analog CMOS technology
- Advanced test capabilities
- P-MQFP-64 package

1.2 Pin Configuration

(top view)



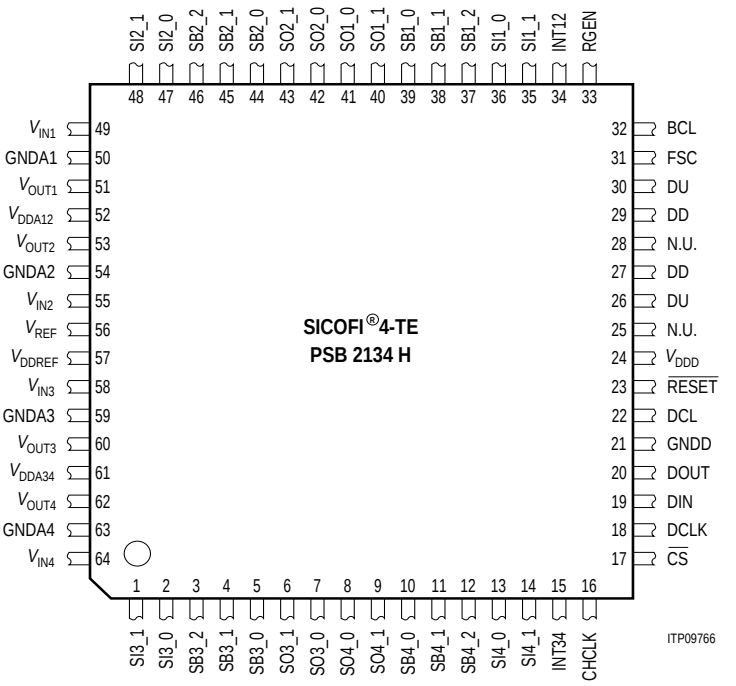


Figure 1

1.3 Pin Definition and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Common Pins for all Channels			
24	V_{DDD}	I	+ 5 V supply for the digital circuitry [1)]
21	GNDD	I	Ground Digital, not internally connected to GNDA1,2,(3,4) All digital signals are referred to this pin
52	V_{DDA12}	I	+ 5 V Analog supply voltage for channel 1 and 2 [1)]
56	V_{REF}	I/O	Reference voltage, has to be connected to a 220 nF cap. to ground, can also be used as virtual ground for analog inputs and outputs (high-ohmic buffer needed !!!)
57	V_{DDREF}	I	+ 5 V Analog supply voltage (100 nF cap. required)
31	FSC	I	Frame synchronization clock, 8 kHz, identifies the beginning of the frame, individual time slots are referenced to this pin, FSC must be synchronous to DCL and BCL
32	BCL	I	IOM-2 bit clock 768 kHz, determines the rate at which PCM data is shifted into or out of the PCM-ports
26,30	DU	I/O	IOM-2 Data Upstream interface. Transmits or receives PCM data in 8 bit bursts. Both pins must be connected together.
27,29	DD	I/O	IOM-2 Data Downstream interface. Transmits or receives PCM data in 8 bit bursts. Both pins must be connected together.
23	$\overline{\text{RESET}}$	I	Reset input - forces the device to default mode, active low
22	DCL	I	Master clock input 1536 kHz, synchronous to FSC, must be available if the SICOFI2/4-TE is operating
17	$\overline{\text{CS}}$	I	µ-Controller interface: chip select enable to read or write data, active low
18	DCLK	I	µ-Controller interface: data clock, shifts data from or to device, the maximum clock rate is 8192 kHz

Pin No.	Symbol	Input (I) Output (O)	Function
19	DIN	I	µ-Controller interface: control data input pin, DCLK determines the data rate
20	DOUT	O	µ-Controller interface: control data output pin, DCLK determines the data rate, DOUT is high ‘Z’ if no data is transmitted from the SICOFI2/4-TE
33	RGEN	O	Ring generator output, provides a programmable (2 … 28 ms) output signal (synchronous to DCL)
16	CHCLK2	O	Chopper Clock output, provides a 256, or 512 or 16384 kHz signal, is synchronous to DCL
34	INT12	O	Interrupt output pin for channel 1 and 2, active high
Dedicated pins for PSB 2132			
61	V_{DDA}	I	+ 5 V Analog supply voltage [1)]
59,63	GNDA	I	Ground analog for unused analog I/O pins
1,2,13, 14	N.U.I	I	None usable input, tie directly to GNDD
3,4,5, 10,11, 12	N.U.I.O	I/O	None usable input/output, tie via a pull-down-resistor to GNDD.
6,7,8,9, 15,25, 28,58, 60,62, 64	N.U.		None usable, leave unconnected
Dedicated pins for PSB 2134			
61	V_{DDA34}	I	+ 5 V Analog supply voltage for channel 3 and 4[1)]
15	INT34	O	Interrupt output pin for channel 3 and 4, active high

Pin No.	Symbol	Input (I) Output (O)	Function
Specific Pins for Channel 1			
50	GNDA1	I	Ground Analog for channel 1, not internally connected to GNDD or GNDA2,3,4
49	V_{IN1}	I	Analog voice (voltage) input for channel 1, has to be connected to the SLIC by a 39 nF cap.
51	V_{OUT1}	O	Analog voice (voltage) output for channel 1, has to be connected to the SLIC via a cap. [2)]
36	SI1_0	I	Signaling input pin 0 for channel 1
35	SI1_1	I	Signaling input pin 1 for channel 1
41	SO1_0	O	Signaling output pin 0 for channel 1
40	SO1_1	O	Signaling output pin 1 for channel 1
39	SB1_0	I/O	Bi-directional signaling pin 0 for channel 1
38	SB1_1	I/O	Bi-directional signaling pin 1 for channel 1
37	SB1_2	I/O	Bi-directional signaling pin 2 for channel 1
Specific Pins for Channel 2			
54	GNDA2	I	Ground Analog for channel 2, not internally connected to GNDD or GNDA 1,3,4
55	V_{IN2}	I	Analog voice (voltage) input for channel 2, has to be connected to the SLIC by a 39 nF cap.
53	V_{OUT2}	O	Analog voice (voltage) output for channel 2, has to be connected to the SLIC via a cap. [2)]
47	SI2_0	I	Signaling input pin 0 for channel 2
48	SI2_1	I	Signaling input pin 1 for channel 2
42	SO2_0	O	Signaling output pin 0 for channel 2
43	SO2_1	O	Signaling output pin 1 for channel 2
44	SB2_0	I/O	Bi-directional signaling pin 0 for channel 2
45	SB2_1	I/O	Bi-directional signaling pin 1 for channel 2
46	SB2_2	I/O	Bi-directional signaling pin 2 for channel 2

Pin No.	Symbol	Input (I) Output (O)	Function
Specific Pins for Channel 3 (PSB 2134 only)			
59	GNDA3	I	Ground Analog for channel 3, not internally connected to GNDD or GNDA1,2,4
58	V_{IN3}	I	Analog voice (voltage) input for channel 3, has to be connected to the SLIC by a 39 nF cap.
60	V_{OUT3}	O	Analog voice (voltage) output for channel 3, has to be connected to the SLIC via a cap. [2)]
2	SI3_0	I	Signaling input pin 0 for channel 3
1	SI3_1	I	Signaling input pin 1 for channel 3
7	SO3_0	O	Signaling output pin 0 for channel 3
6	SO3_1	O	Signaling output pin 1 for channel 3
5	SB3_0	I/O	Bi-directional signaling pin 0 for channel 3
4	SB3_1	I/O	Bi-directional signaling pin 1 for channel 3
3	SB3_2	I/O	Bi-directional signaling pin 2 for channel 3

Pin No.	Symbol	Input (I) Output (O)	Function
Specific Pins for Channel 4 (PSB 2134 only)			
63	GNDA4	I	Ground Analog for channel 4, not internally connected to GNDD or GNDA1,2,3
64	V_{IN4}	I	Analog voice (voltage) input for channel 4, has to be connected to the SLIC by a 39 nF cap.
62	V_{OUT4}	O	Analog voice (voltage) output for channel 4, has to be connected to the SLIC via a cap. [2]
13	SI4_0	I	Signaling input pin 0 for channel 4
14	SI4_1	I	Signaling input pin 1 for channel 4
8	SO4_0	O	Signaling output pin 0 for channel 4
9	SO4_1	O	Signaling output pin 1 for channel 4
10	SB4_0	I/O	Bi-directional signaling pin 0 for channel 4
11	SB4_1	I/O	Bi-directional signaling pin 1 for channel 4
12	SB4_2	I/O	Bi-directional signaling pin 2 for channel 4

[1] A 100 nF cap. should be used for blocking these pins, see also on page 83

[2] The value for the capacitor needed, depends on the input impedance of the ‘SLIC’-circuitry. For choosing the appropriate values see figure on page 72.

2 Functional Description

2.1 System Integration

The SICOFI2/4-TE is connected to an IOM-2 compatible transceiver such as the PEB 8191 INTC-Q for U-interface or NT-applications or the PSB 2186 ISAC-S TE or PSB 2115 IPAC for S/T-interface applications. The FSC output is connected to the FSC input on the SICOFI2/4-TE. The DCL output of the transceiver is fed to the DCL input of the SICOFI2/4-TE which is used as master clock. For transferring PCM data, the bit clock signal of the transceiver (BCL, 768 kHz) is connected to the SICOFI2/4-TE.

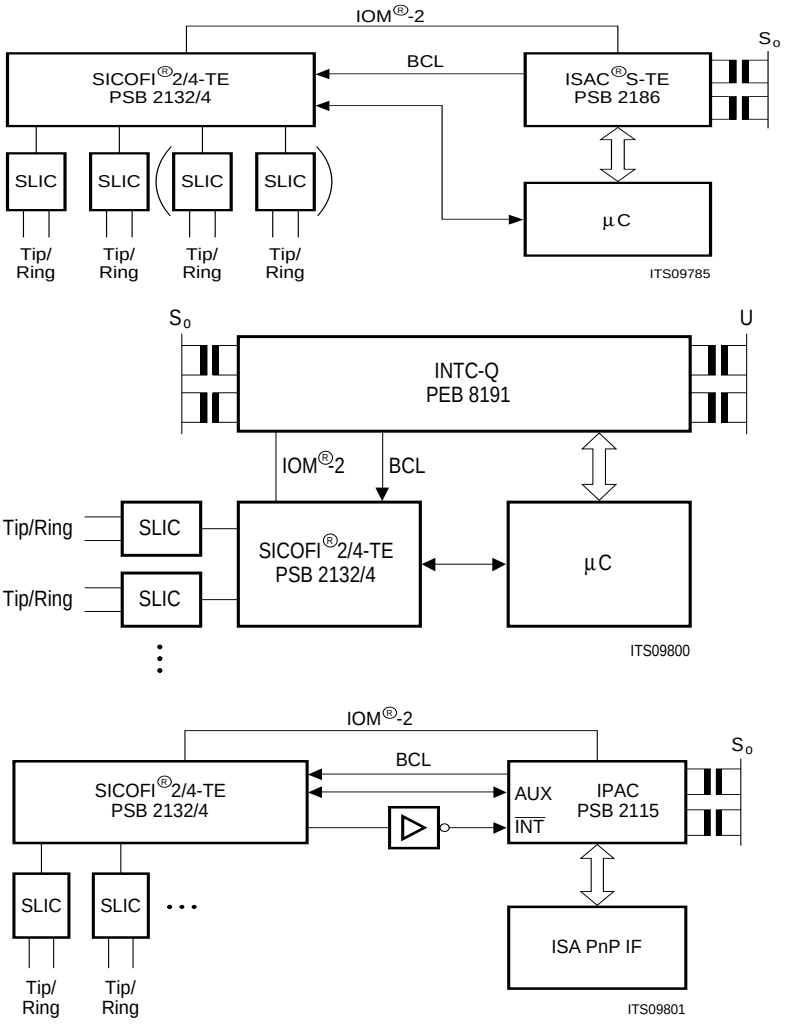


Figure 2

The microcontroller interface is connected to a microcontroller. Since the data transfer does not require duplex operation it can be connected both to SPI compatible microcontrollers (Siemens C5xx series, C161 series) as well as to Intel C51 based ones.

The SICOFI2/4-TE provides an high active interrupt output. The interrupts are caused by changes on the input lines of each channel. In order to operate it is necessary to keep DCL running all the time. If DCL is stopped in order to reduce the power consumption of the system, additional hardware is required. This hardware may be used to generate directly an interrupt to the microcontroller which may than request IOM-clocking.

Each channel serves seven I/O lines (2xO, 2xI, 3xI/O) which are used to control the inputs of the SLIC or to fed the outputs of a SLIC to the microcontroller.

The RGEN output can be used to generate the input signal of a ringing SLIC. Its frequency is programmable down to 35,7 Hz.

2.2 SICOFI®2/4-TE Principles

The SICOFI2/4-TE is designed for terminal adapters and Intelligent NT (NT1plus) applications.

It is designed to reduce the number of external components required for the integrated or discrete SLIC.

The SICOFI-2/4 TE bridges the gap between analog and digital voice signal transmission in modern telecommunication systems. High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) provide the conversion accuracy required. Analog antialiasing prefilters (PREFI) and smoothing postfilters (POFI) are included. The connection between the ADC and the DAC (with high sampling rate) and the DSP, is done by specific Hardware Filters, for filtering like interpolation and decimation. The dedicated Digital Signal Processor (DSP) handles all the algorithms necessary e.g. for PCM bandpass filtering, sample rate conversion and PCM companding. The PCM-interface handles digital voice transmission, a serial µC-interface handles SICOFI2/4-TE feature control and transparent access to the SICOFI2/4-TE command and indication pins. To program the filters, precalculated sets of coefficients are downloaded from the system to the on-chip Coefficient-RAM (CRAM).

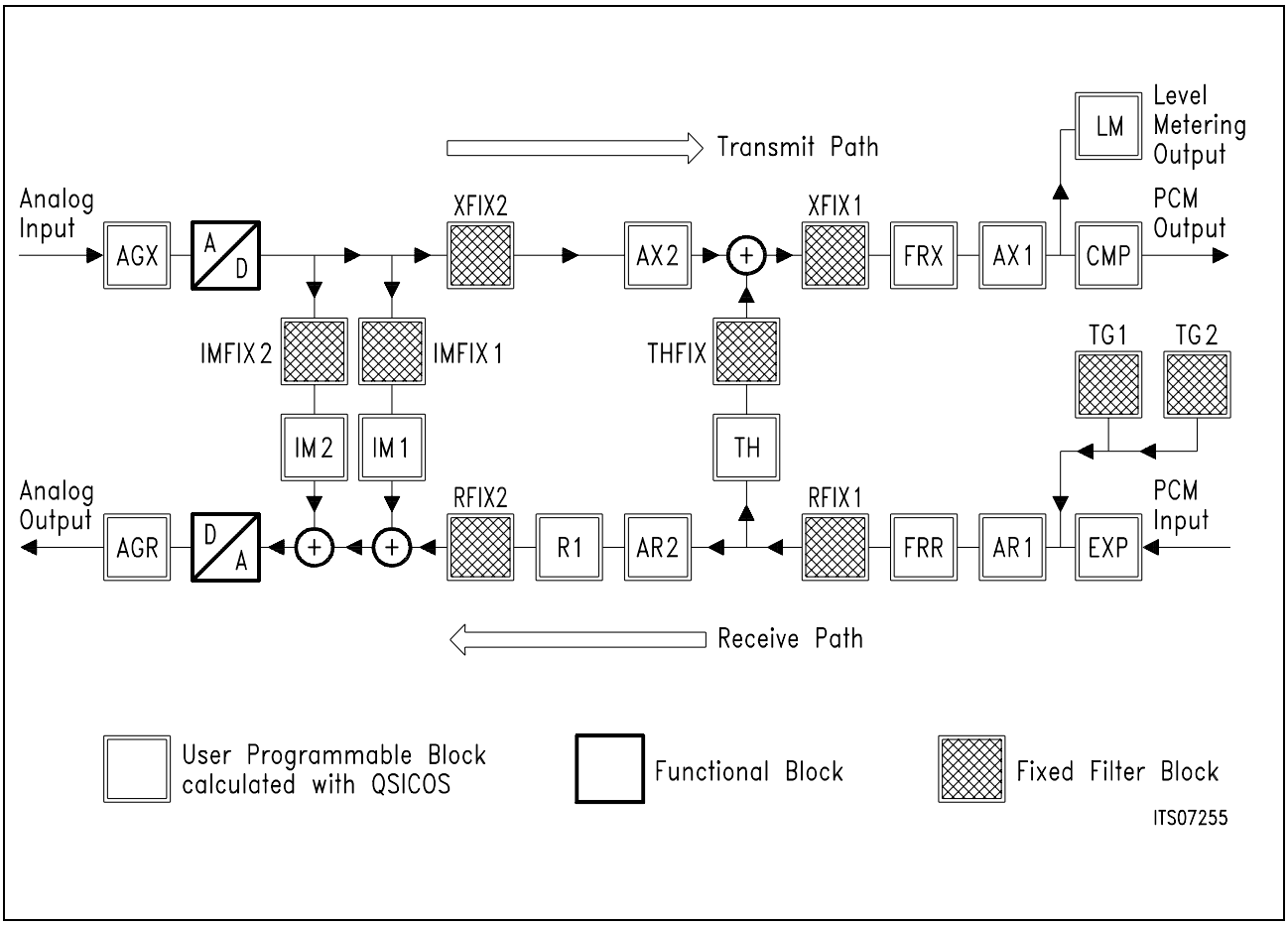


Figure 3
SICOFI®2/4-TE Signal Flow Graph (for any channel)

Transmit Path

The analog input signal has to be DC-free connected by an external capacitor because there is an internal virtual reference ground potential. After passing a simple antialiasing prefilter (PREFI) the voice signal is converted to a 1-bit digital data stream in the Sigma-Delta-converter. The first downsampling steps are done in fast running digital hardware filters. The following steps are implemented in the micro-code which has to be executed by the central Digital Signal Processor. This DSP-machine is able to handle the workload for all four channels. At the end the fully processed signal (flexibly programmed in many parameters) is transferred to the PCM- interface in a PCM-compressed signal representation.

Receive Path

The digital input signal is received via the PCM interface. Expansion, PCM-Law-pass-filtering, gain correction and frequency response correction are the next steps which are done by the DSP-machine. The upsampling interpolation steps are again processed by fast hardware structures to reduce the DSP-workload. The

upsampled 1-bit data stream is then converted to an analog equivalent which is smoothed by a POST-Filter (POFI). As the signal V_{OUT} is also referenced to an internal virtual ground potential, an external capacitor is required for DC-decoupling.

Loops

There are two loops implemented. The first is to generate the AC-input impedance (IM) and the second is to perform a proper hybrid balancing (TH). A simple extra path IM2 (from the transmit to the receive path) supports the impedance matching function.

Test Features

There are four analog and five digital test loops implemented in the SICOFI-2/4 TE. For special tests it is possible to cut off the receive and the transmit path at two different points. In addition, external test loops including the subscriber line measurement are possible using the level meatering feature.

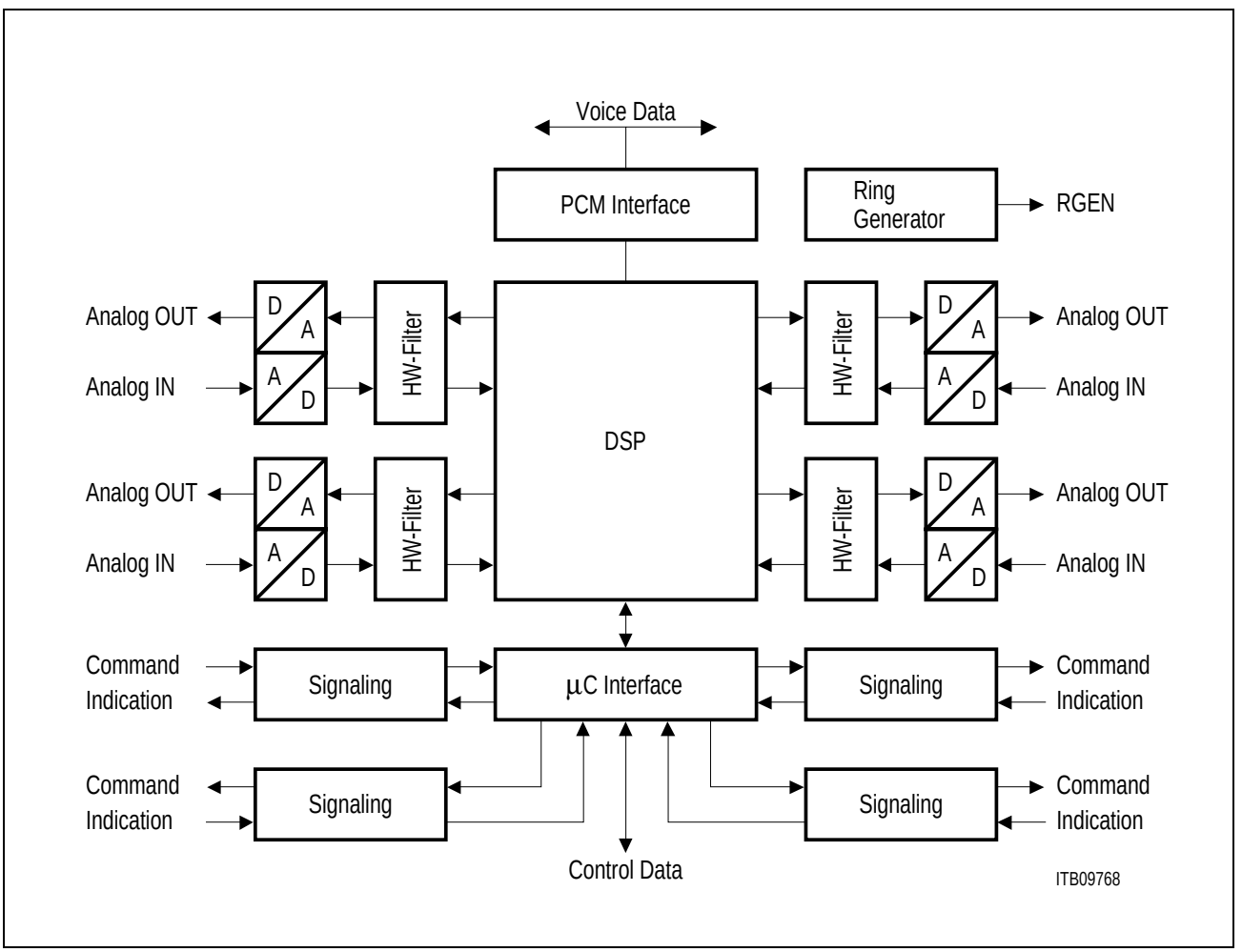


Figure 4
SICOFI2/4®-TE Block Diagram

2.3 The IOM-2 PCM-interface

One serial PCM-interface is used for transfer of A- or µ-law compressed voice data. The PCM-interface consists of 4 pins:

BCL: IOM-2 bit clock, 768 kHz

FSC: Frame Synchronization Clock, 8 kHz

DU: Data transmit or receive in data upstream direction

DD: Data receive or transmit in data downstream direction

The Frame Sync FSC pulse identifies the beginning of a receive and transmit frame for all of the two / four channels. The BCL clock is the signal to synchronize the data transfer on both lines DU and DD. Bytes in all channels are serialized to 8 bit width and MSB first. As a default setting, the rising edge indicates the start of the bit, while the falling edge is used to latch the contents of the received data.

The data rate of the interface is fixed to 768 kHz. A frame consists of 12 time slots of 8 bits each. In the Time Slot Configuration Registers CR5 and CR6 the user can select an individual time slot, and one of two data lines, for any of the voice channels. Receive and transmit time slots can also be programmed individually. An extra delay of up to 7 clocks, valid for all channels, as well as the sampling slope may be programmed (see XR6).

A typical example is shown below.

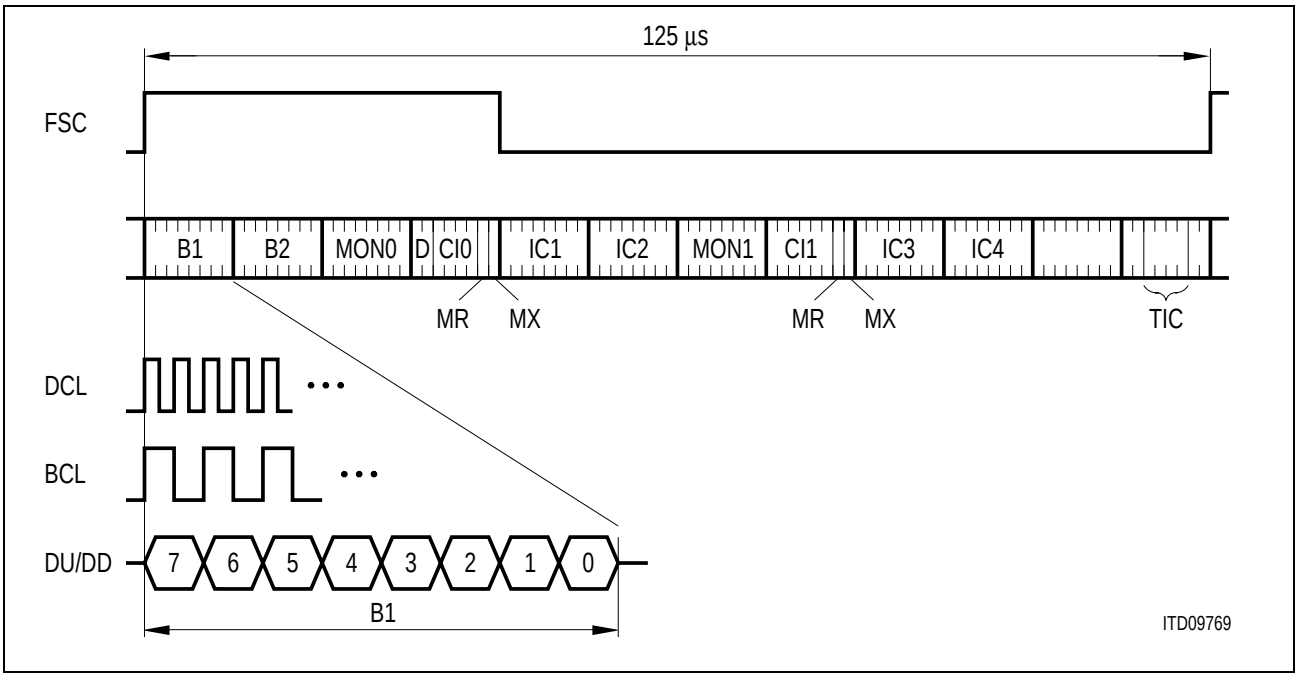


Figure 5
Example for IOM-2 Terminal Mode

2.4 The µ-Controller Interface

The internal configuration registers, the signaling interface, and the Coefficient-RAM (CRAM) of the SICOFI-2/4-TE are programmable via a serial µ-Controller interface.

The µ-Controller interface consists of four lines: $\overline{CS}$, DCLK, DIN and DOUT:

$\overline{CS}$ is used to start a serial access to the SICOFI-2/4-TE registers and Coefficient-RAM. Following a falling edge of CS, the first eight bits received on DIN specify the command. Subsequent data bytes (number depends on command) are stored in the selected configuration registers or the selected part of the Coefficient-RAM.

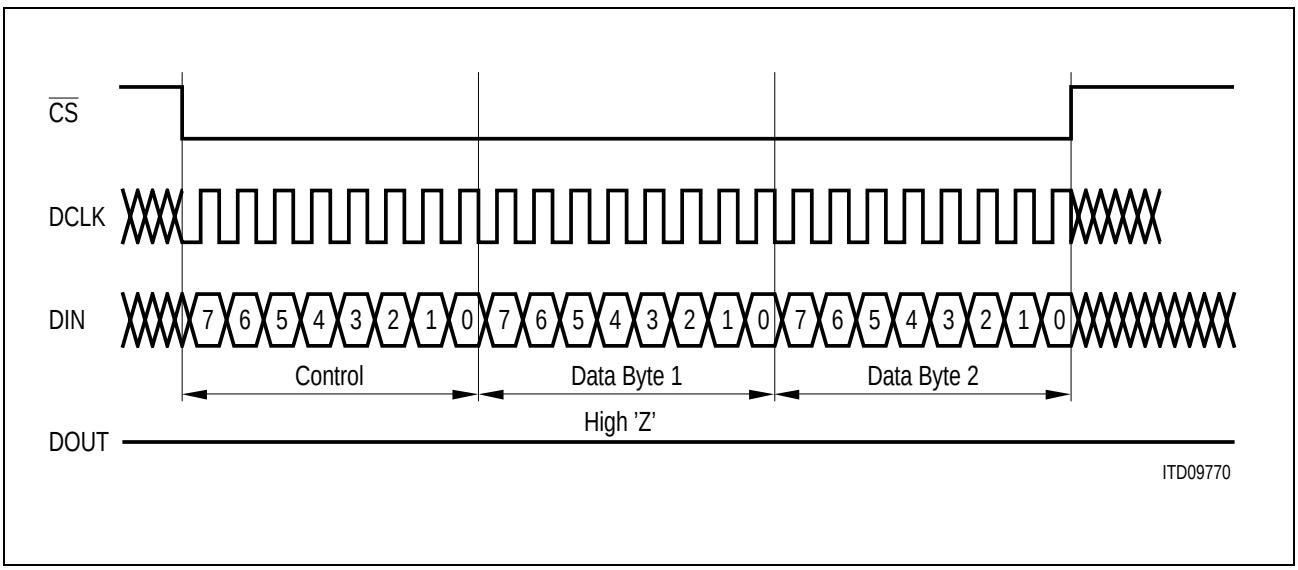


Figure 6
Example for a Write Access, with Two Data Bytes Transferred

If the first eight bits received via DIN specify a read-command, the SICOFI-2/4 TE will start a response via DOUT with its specific address byte (81_H). After transmitting this identification, the specified n data bytes (contents of configuration registers, or contents of the CRAM) will follow on DOUT.

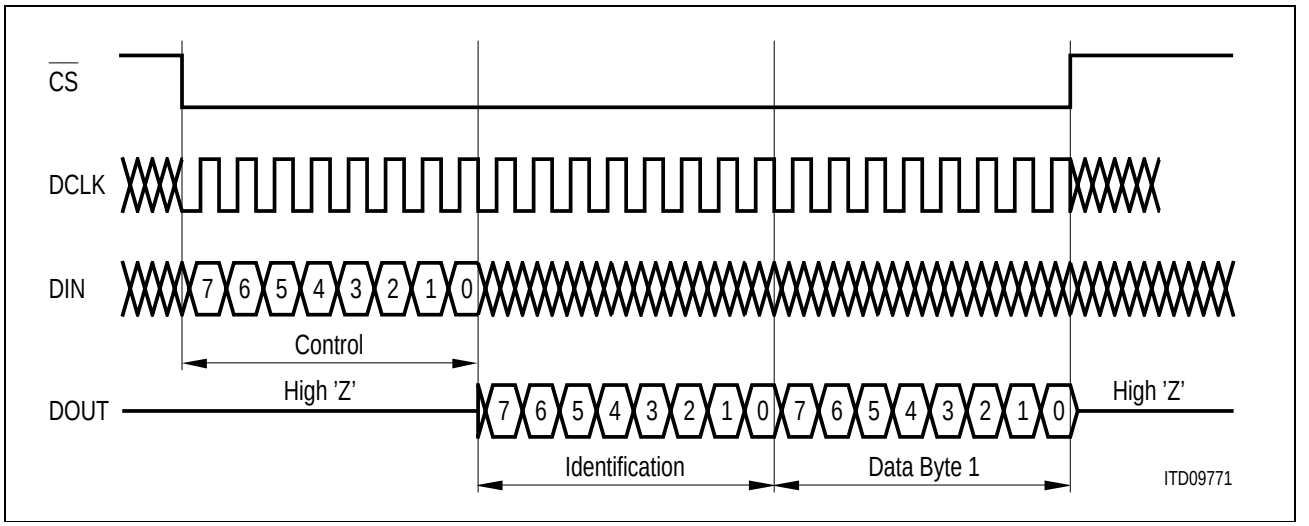


Figure 7
Example for a Read Access, with One Data Byte Transferred via DOUT

The data transfer is synchronized by the DCLK input. The contents of DIN is latched at the rising edge of DCLK, while DOUT changes with the falling edge of DCLK. During execution of commands that are followed by output data (read commands), the device will not accept any new command via DIN. The data transfer sequence is completed by setting $\overline{CS}$ to high.

To reduce the number of connections to the µP DIN and DOUT may be strapped together, and form a bi-directional data-'pin'.

For special applications a byte by byte transfer is needed. This can be done by prolonging the high time of DCLK for a user defined 'waiting time' after transferring any byte.

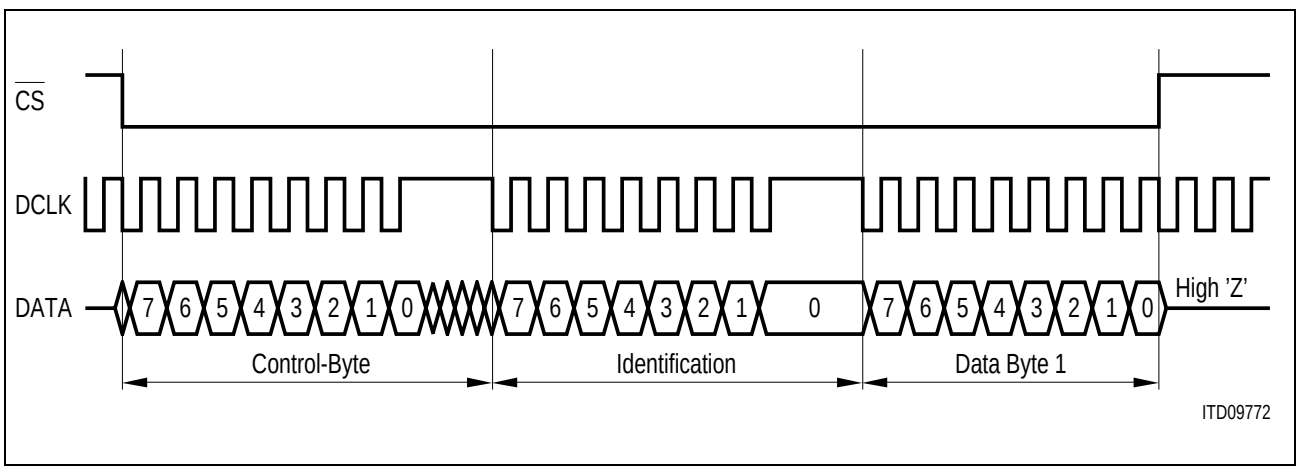


Figure 8
Example for a Write/Read Access, with a Byte by Byte Transfer, and DIN and DOUT Strapped Together

The Identification Byte is "81_H" for the PSB 2132/34.

2.5 The Signaling Interface

The SICOFI-2/4 TE signaling interface is made up of 2 input pins (SIx_0, SIx_1), two output pins (SOx_0, SOx_1) and three bi-directional programmable pins (SBx_0, SBx_1, SBx_2) per channel.

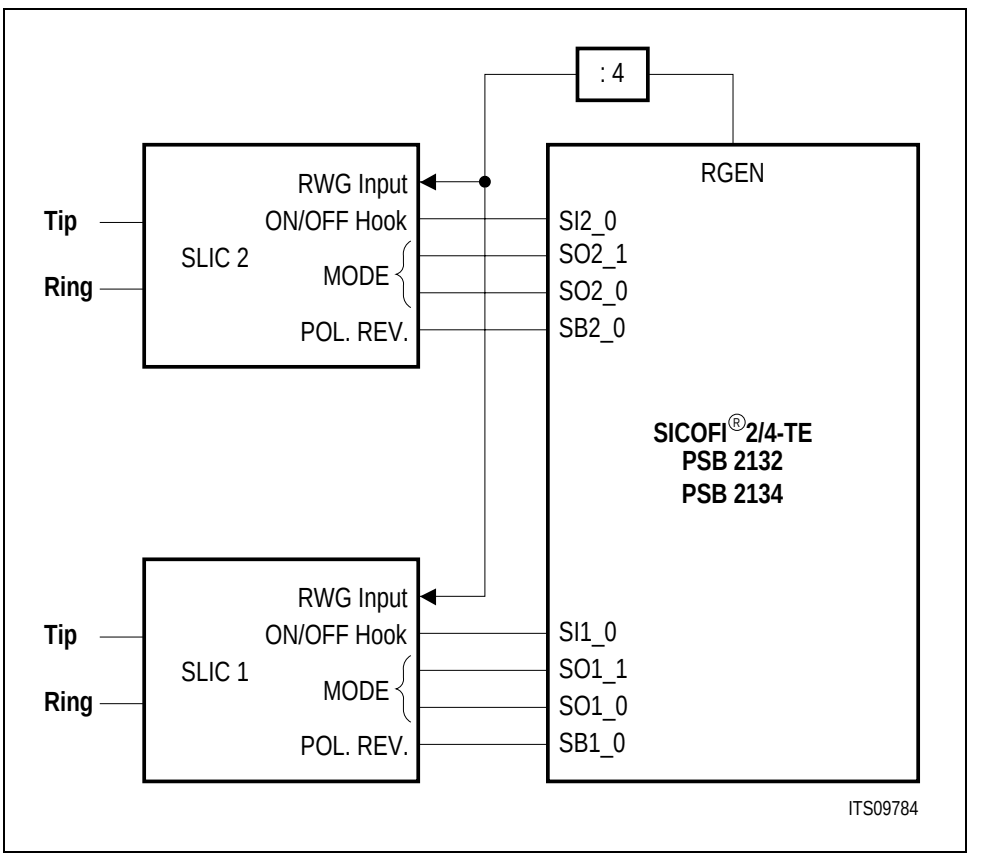


Figure 9

The purpose of these pins is to control the SLIC functions without additional ports on the host or microcontroller.

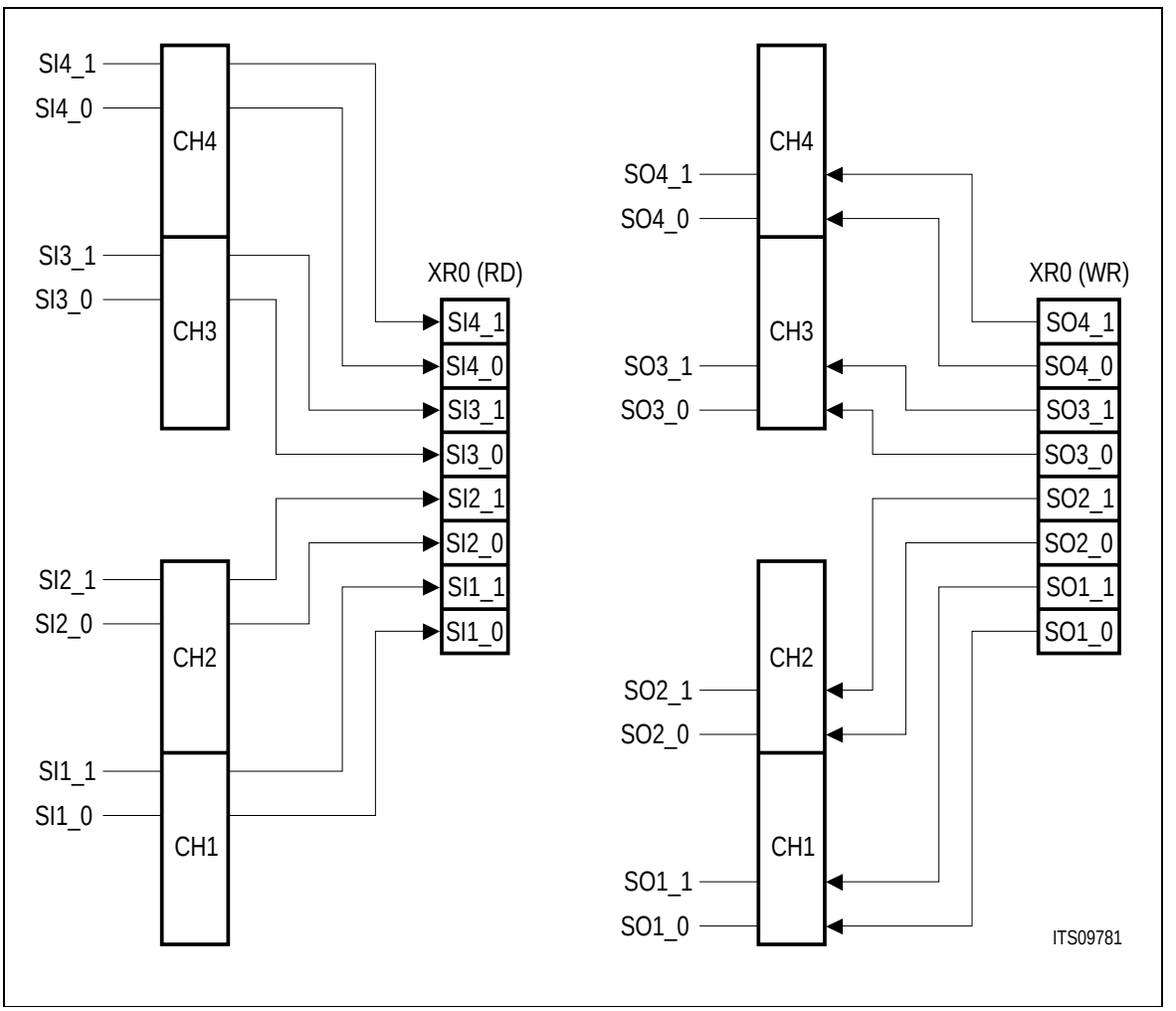


Figure 10

The status bits of all SIx_0 and SIx_1 inputs are stored in the XR0 register (RD). Similar the control bits of SOx_0 and SOx_1 are stored in the XR0 register (WR).

The bidirection status bits are arranged such that all SBx_1 and SBx_0 bits are controlled / read via the XR1 register. The correspondig direction register is the XR2 register. The third bidirectional status bit of each channel is accessed via the four most significant bits of the XR3 register while the least significant four bits specify the corresponding direction.

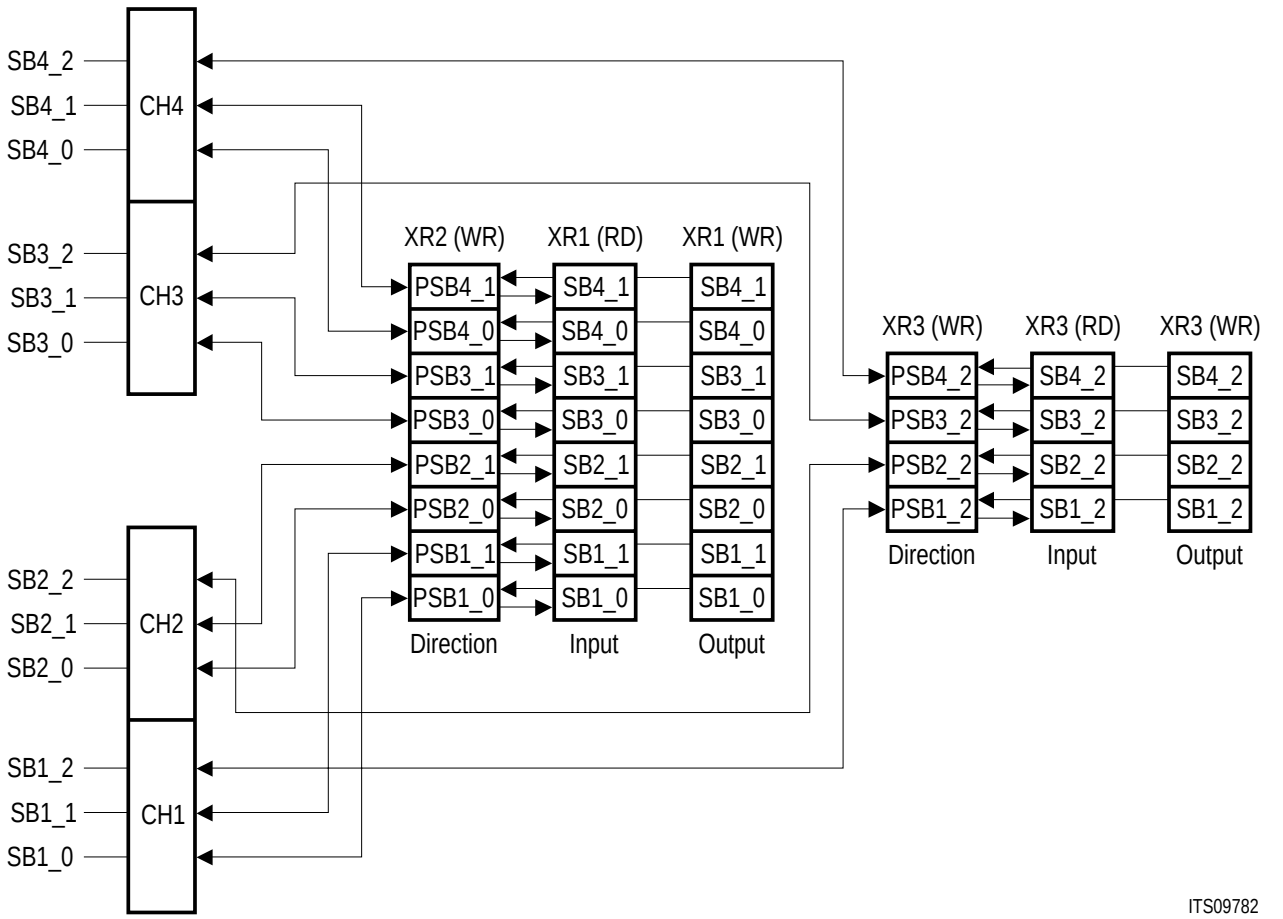


Figure 11

Depending on the application, the lines can be group individually to support the best software interface. E.g. if a DTMF receiver is connected to the SICOFI2/4-TE, the pins SB2_1, SB2_0,SB1_1,SB1_0 may be used for the data bus. This simplifies the software since the value can be read directly from the register.

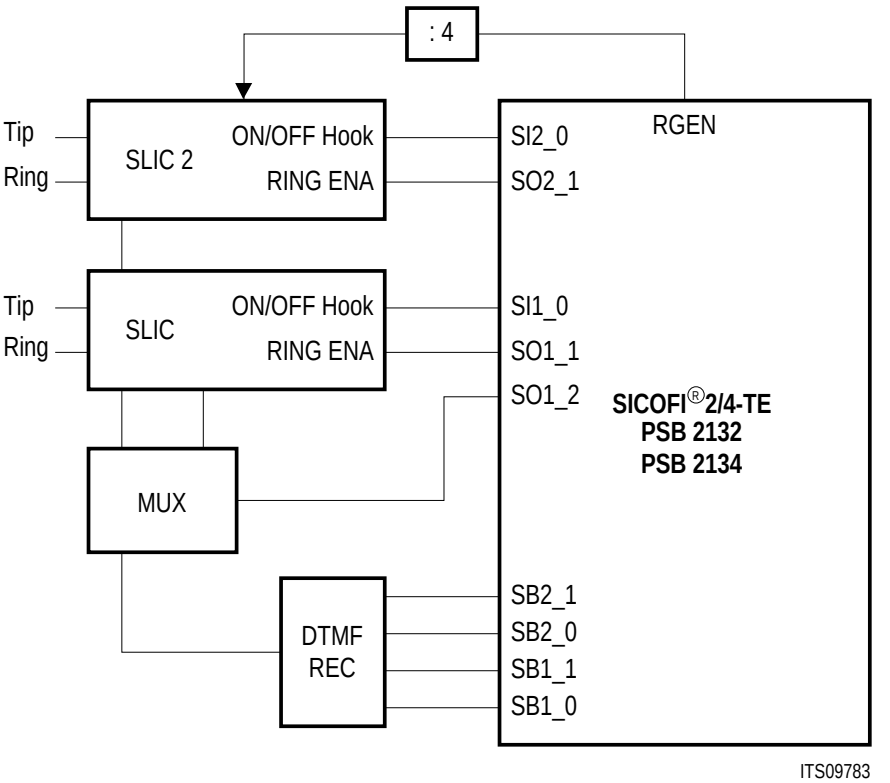


Figure 12

Additional two interrupt pins (INT12, INT34) are provided. If one of the input pins for channel 1 or 2, or one of the bi-directional pins for channel 1 and 2 (if programmed as inputs) changes, and being stable for the debounce time specified in Register XR4, INT12 will go from ‘0’ to ‘1’. This interrupt is cleared if the appropriate registers (XR0, XR1 and XR3) are read via the serial µC-interface. Pin INT34 provides the same functionality for channel 3 and 4.

2.6 Ring Generator and Special Purpose Pin

For special purposes two additional output signals are provided by the SICOFI-2/4 TE.

RGEN (see also register XR4) will provide a programmable ring generator output of 2 to 28 ms. The output of RGEN diveded by four can be used to drive the ring input of a ringin SLIC. RGEN delivers a square-wave signal (duty cycle 1:1).

CHCLK will provide 3 different frequencies (256 kHz, 512 kHz or 16384 kHz). Both signals are only available if a valid signal is applied to the DCL-pin.

3 Programming the SICOFI®-2/4-TE

With the appropriate commands, the SICOFI2/4-TE can be programmed and verified very flexibly via the µ-Controller interface.

With the first byte received via DIN, one of 3 different types of commands (SOP, XOP and COP) is selected. Each of those can be used as a write or read command. Due to the extended SICOFI2/4-TE feature control facilities, SOP, COP and XOP commands contain additional information (e.g. number of subsequent bytes) for programming (write) and verifying (read) the SICOFI2/4-TE status.

A write command is followed by up to 8 bytes of data. The SICOFI2/4-TE responds to a read command with its specific identification and the requested information, that is up to 8 bytes of data.

3.1 Types of Command and Data Bytes

The 8-bit bytes have to be interpreted as either commands or status information stored in Configuration Registers or the Coefficient-RAM. There are three different types of SICOFI -2/4-TE commands which are selected by bit 3 and 4 as shown below.

SOP **STATUS OPERATION:** SICOFI2/4-TE status setting/monitoring

Bit	7							0
	AD2	AD1		1	0			

XOP **EXTENDED OPERATION:** C/I[1)] channel configuration/evaluation

Bit	7							0
		0		1	1			

COP **COEFFICIENT OPERATION:** filter coefficient setting/monitoring

Bit	7							0
	AD2	AD1		0				

Note: [1)] Command/Indication (signaling) channel.

Storage of Programming Information

6 configuration registers per channel:	CR0, CR1, CR2, CR3, CR4 and CR5 accessed by SOP commands
8 common configuration registers:	XR0 .. XR7 accessed by XOP commands, valid for all 4 channels
1 Coefficient-RAM per channel:	CRAM accessed by COP commands

3.2 Examples for SICOFI®2/4-TE Commands

SOP - Write Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Write 1 Byte			0	1	0	0	0	0		Idle								
CR0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Write 2 Bytes			0	1	0	0	0	1		Idle								
CR1	Data									Idle								
CR0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Write 3 Bytes			0	1	0	0	1	0		Idle								
CR2	Data									Idle								
CR1	Data									Idle								
CR0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Write 4 Bytes			0	1	0	0	1	1		Idle								
CR3	Data									Idle								
CR2	Data									Idle								
CR1	Data									Idle								
CR0	Data									Idle								

XOP - Write Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Write 2 Bytes			0	1	1	0	0	1		Idle								
XR1	Data									Idle								
XR0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Write 3 Bytes			0	1	1	0	1	0		Idle								
XR2	Data									Idle								
XR1	Data									Idle								
XR0	Data									Idle								

COP - Write Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
COP-Write 4 Bytes			0	0						Idle								
Coeff. 3	Data									Idle								
Coeff. 2	Data									Idle								
Coeff. 1	Data									Idle								
Coeff. 0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
COP-Write 8 Bytes			0	0						Idle								
Coeff. 7	Data									Idle								
Coeff. 6	Data									Idle								
Coeff. 5	Data									Idle								
Coeff. 4	Data									Idle								
Coeff. 3	Data									Idle								
Coeff. 2	Data									Idle								
Coeff. 1	Data									Idle								
Coeff. 0	Data									Idle								

SOP - Read Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Read 1 Byte			1	1	0	0	0	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								CR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Read 2 Bytes			1	1	0	0	0	1		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								CR1
	Idle									Data								CR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Read 3 Bytes			1	1	0	0	1	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								CR2
	Idle									Data								CR1
	Idle									Data								CR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Read 4 Bytes			1	1	0	0	1	1		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								CR3
	Idle									Data								CR2
	Idle									Data								CR1
	Idle									Data								CR0

XOP-Read Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Read 1 Byte			1	1	1	0	0	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								XR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Read 2 Bytes			1	1	1	0	0	1		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								XR1
	Idle									Data								XR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Read 3 Bytes			1	1	1	0	1	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								XR2
	Idle									Data								XR1
	Idle									Data								XR0

COP-Read Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
COP-Read 4 Bytes			1	0	1					Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								Coeff. 3
	Idle									Data								Coeff. 2
	Idle									Data								Coeff. 1
	Idle									Data								Coeff. 0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
COP-Read 8 Bytes			1	0	0					Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								Coeff. 8
	Idle									Data								Coeff. 7
	Idle									Data								Coeff. 6
	Idle									Data								Coeff. 5
	Idle									Data								Coeff. 4
	Idle									Data								Coeff. 3
	Idle									Data								Coeff. 2
	Idle									Data								Coeff. 1

Example of a Mixed Command

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Write 4 Bytes			0	1	0	0	1	1		Idle								
CR3	Data									Idle								
CR2	Data									Idle								
CR1	Data									Idle								
CR0	Data									Idle								
XOP-Write 2 Bytes			0	1	1	0	0	1		Idle								
XR1	Data									Idle								
XR0	Data									Idle								
COP-Write 4 Bytes			0	0	1					Idle								
Coeff. 3	Data									Idle								
Coeff. 2	Data									Idle								
Coeff. 1	Data									Idle								
Coeff. 0	Data									Idle								
SOP-Read 3 Bytes			1	1	0	0	1	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								CR2
	Idle									Data								CR1
	Idle									Data								CR0
COP-Read 4 Bytes			1	0	1					Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								Coeff. 3
	Idle									Data								Coeff. 2
	Idle									Data								Coeff. 1
	Idle									Data								Coeff. 0
XOP-Read 1 Byte			1	1	1	0	0	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								XR0

3.3 SOP Command

To modify or evaluate the SICOFI2/4-TE status, the contents of up to 6 configuration registers CR0 .. CR5 may be transferred to or from the SICOFI2/4-TE. This is started by a SOP-Command (status operation command).

Bit 7 0

AD2	AD1	RW	1	0	LSEL2	LSEL1	LSEL0

AD Address Information

AD = 00 SICOFI2/4-TE - channel 1 is addressed with this command

AD = 01 SICOFI2/4-TE - channel 2 is addressed with this command

AD = 10 SICOFI2/4-TE - channel 3 is addressed with this command (PSB 2134 only)

AD = 11 SICOFI2/4-TE - channel 4 is addressed with this command (PSB 2134 only)

RW Read/Write Information: Enables reading from the SICOFI2/4-TE or writing information to the SICOFI2/4-TE

RW = 0 Write to SICOFI2/4-TE

RW = 1 Read from SICOFI2/4-TE

LSEL Length select information (see also programming procedure)
This field identifies the number of subsequent data bytes

LSEL = 000 1 byte of data is following (CR0)

LSEL = 001 2 bytes of data are following (CR1, CR2)

LSEL = 010 3 bytes of data are following (CR2, CR1, CR0)

LSEL = 011 4 bytes of data are following (CR3, CR2, CR1, CR0)

LSEL = 100 5 bytes of data are following (CR4, CR3, CR2, CR1, CR0)

LSEL = 101 6 bytes of data are following (CR5, CR4, CR3, CR2, CR1, CR0)

All other codes are reserved for future use !

Note: If only one configuration register requires modification, for example CR5, this can be accomplished by setting LSEL = 101 and releasing pin CS after CR5 is written.

3.3.1 CR0 Configuration Register 0

Configuration register CR0 defines the basic SICOFI2/4-TE settings, which are: enabling/disabling the programmable digital filters.

Bit	7						0
	TH	IM/R1	FRX	FRR	AX	AR	TH-SEL

TH Enable TH- (Trans Hybrid Balancing) Filter

TH = 0: TH-filter disabled

TH = 1: TH-filter enabled

IM/R1 Enable IM-(Impedance Matching) Filter and R1-Filter

IM/R1 = 0: IM-filter and R1-filter disabled

IM/R1 = 1: IM-filter and R1-filter enabled

FRX Enable FRX (Frequency Response Transmit)-Filter

FRX = 0: FRX-filter disabled

FRX = 1: FRX-filter enabled

FRR Enable FRR (Frequency Response Receive)-Filter

FRR = 0: FRR-filter disabled

FRR = 1: FRR-filter enabled

AX Enable AX-(Amplification/Attenuation Transmit) Filter

AX = 0: AX-filter disabled

AX = 1: AX-filter enabled

AR Enable AR-(Amplification/Attenuation Receive) Filter

AR = 0: AX-filter disabled

AR = 1: AX-filter enabled

TH-SEL 2 bit field to select one of two/four programmed TH-filter coefficient sets

TH-Sel = 0 0: TH-filter coefficient set 1 is selected

TH-Sel = 0 1: TH-filter coefficient set 2 is selected

TH-Sel = 1 0: TH-filter coefficient set 3 is selected (PSB 2134 only)

TH-Sel = 1 1: TH-filter coefficient set 4 is selected (PSB 2134 only)

3.3.2 CR1 Configuration Register 1

Configuration register CR1 selects tone generator modes and other operation modes.

Bit 7 … 0

ETG2	ETG1	PTG2	PTG1	LAW	0	0	PU

ETG2 Enable programmable tone generator 2 [1)]

ETG2 = 0: Programmable tone generator 2 is disabled

ETG2 = 1: Programmable tone generator 2 is enabled

ETG1 Enable programmable tone generator 1

ETG1 = 0: Programmable tone generator 1 is disabled

ETG1 = 1: Programmable tone generator 1 is enabled

PTG2 User programmed frequency or fixed frequency is selected

PTG2 = 0: Fixed frequency for tone generator 2 is selected (1 kHz)

PTG2 = 1: Programmed frequency for tone generator 2 is selected

PTG1 User programmed frequency or fixed frequency is selected

PTG1 = 0: Fixed frequency for tone generator 1 is selected (1 kHz)

PTG1 = 1: Programmed frequency for tone generator 1 is selected

LAW PCM - law selection

LAW = 0: A-Law is selected

LAW = 1: µ-Law (µ255 PCM) is selected

PU Power UP, sets the addressed channel to Power Up / Down

PU = 0: The addressed channel is set to Power Down (standby)

PU = 1: The addressed channel is set to Power Up (operating)

[1)] Tone generator 2 is not available if Level Metering Function is enabled!

3.3.3 CR2 Configuration Register 2

Bit 7 … 0

COT/R	0	IDR	LM	LMR	V+T

COT/R Selection of Cut off Transmit/Receive Paths

0 0 0:	Normal Operation	
0 0 1:	COT16	Cut Off Transmit Path at 16 kHz (input of TH-Filter)
0 1 0:	COT8	Cut Off Transmit Path at 8 kHz (input of compression, output is zero for µ-law, 1 LSB for A-law)
1 0 1:	COR4M	Cut Off Receive Path at 4 MHz (POFI-output)
1 1 0:	COR64	Cut Off Receive Path at 64 kHz (IM-filter input)

IDR Initialize Data RAM

IDR = 0: Normal operation is selected

IDR = 1: Contents of Data RAM is set to 0 (used for production test purposes)

LM Level Metering function [1)]

LM = 0: Level metering function is disabled

LM = 1: Level metering function is enabled

LMR Result of Level Metering function (this bit can not be written)

LMR = 0: Level detected was lower than the reference

LMR = 1: Level detected was higher than the reference

V+T Add Voice signal and Tone Generator signal

V+T = 0: Voice or Tone Generator is fed to the DAC

V+T = 1: Voice and Tone Generator Signals are added, and fed to the Digital to Analog Converter

1) Explanation of the level metering function:
A signal fed to A/µ-Law compression via AX- and HPX-filters (from a digital loop, or externally via VIN), is rectified, and the power is measured. If the power exceeds a certain value, loaded to XR7, bit LMR is set to '1'. The power of the incoming signal can be adjusted by AX-filters.

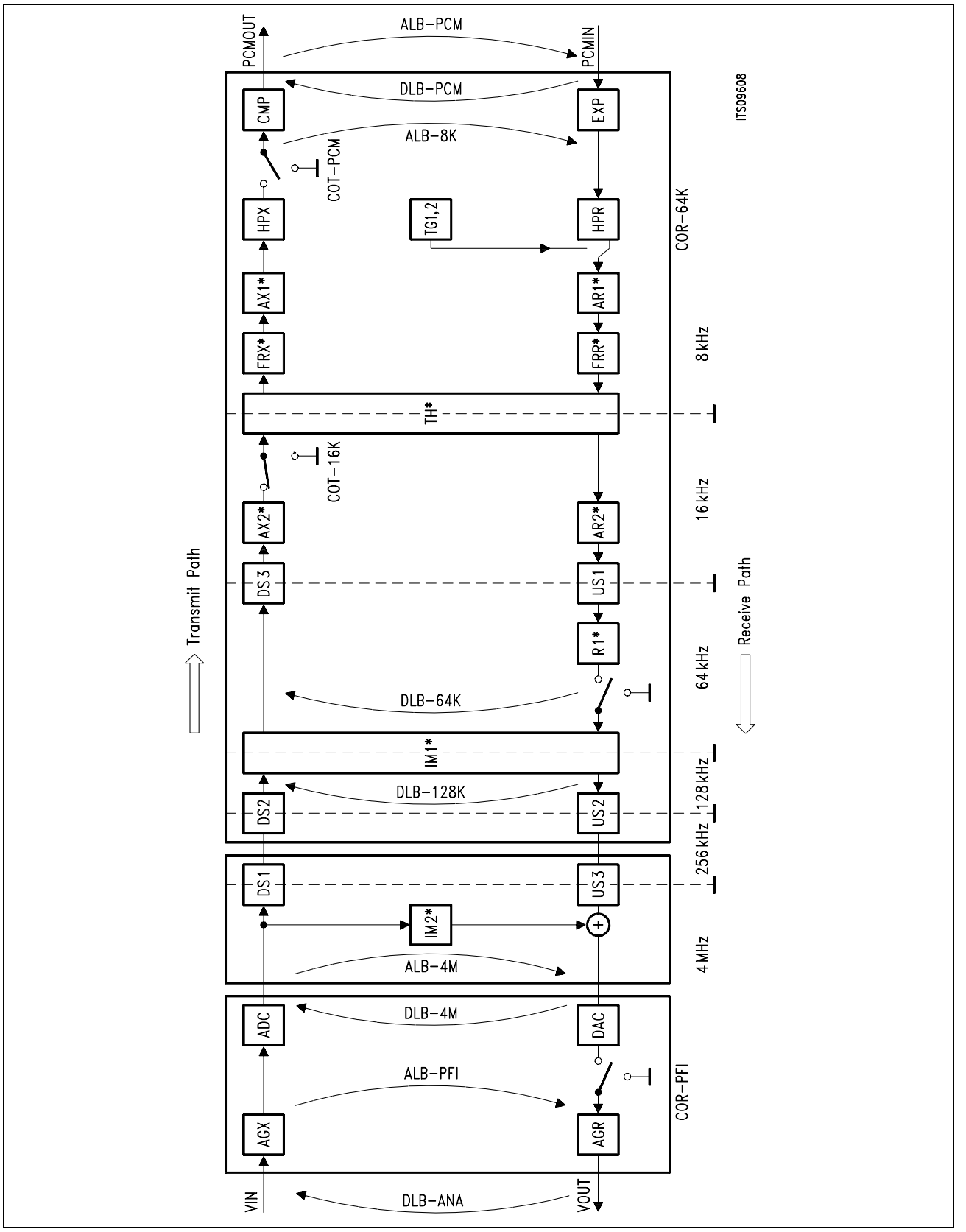


Figure 13
'CUT OFF's' and Loops

3.3.4 CR3 Configuration Register 3

Bit 7				0
Test-Loops	**AGX**	**AGR**	**D-HPX**	**D-HPR**

Test-Loops 4 bit field for selection of Analog and Digital Loop Backs

0 0 0 0:		No loop back is selected (normal operation)
0 0 0 1:	ALB-PFI	Analog loop back via PREFI-POFI is selected
0 0 1 1:	ALB-4M	Analog loop back via 4 MHz is selected
0 1 0 0:	ALB-PCM	Analog loop back via 8 kHz (PCM) is selected (attention: special settings necessary)
0 1 0 1:	ALB-8K	Analog loop back via 8 kHz (linear) is selected
1 0 0 0:	DLB-ANA	Digital loop back via analog port is selected
1 0 0 1:	DLB-4M	Digital loop back via 4 MHz is selected
1 1 0 0:	DLB-128K	Digital loop back via 128 kHz is selected
1 1 0 1:	DLB-64K	Digital loop back via 64 kHz is selected
1 1 1 1:	DLB-PCM	Digital loop back via PCM-registers is selected

AGX Analog gain in transmit direction

AGX = 0: Analog gain is disabled

AGX = 1: Analog gain is enabled (6.02 dB amplification)

AGR Analog gain in receive direction

AGR = 0: Analog gain is disabled

AGR = 1: Analog gain is enabled (6.02 dB attenuation)

D-HPX Disable highpass in transmit direction

D-HPX = 0: Transmit high pass is enabled

D-HPX = 1: Transmit high pass is disabled[1)]

D-HPR Disable highpass in receive direction

D-HPR = 0: Receive high pass is enabled

D-HPR = 1: Receive high pass is disabled[2)]

1) In this case the transmit-path signal is attenuated 0.06 dB

2) In this case the receive-path signal is attenuated 0.12 dB

3.3.5 CR4 Configuration Register 4

Configuration register CR4, sets the receiving time slot and the receiving PCM-highway.

Bit 7 0

RLINE	0	0	0	RS3	RS2	RS1	RS0

RLINE Selects the data line for the receiving of PCM-data

RLINE = 0: DD is selected

RLINE = 1: DU is selected

RS[3:0] Selects the time slot (0 to 11) used for receiving the PCM-data

The time slot-number is binary coded.

0 0 0 0: Time slot 0 is selected

0 0 0 1: Time slot 1 is selected

....

1 0 1 0: Time slot 10 is selected

1 0 1 1: Time slot 11 is selected

3.3.6 CR5 Configuration Register 5

Configuration register CR5, sets the transmit time slot and the transmit PCM-highway.

Bit 7 0

XLINE	0	0	0	XS3	XS2	XS1	XS0

XLINE Selects the data line for transmitting PCM-data

XLINE = 0: DU is selected

XLINE = 1: DD is selected

XS[3:0] Selects the time slot (0 to 11) used for transmitting the PCM-data

The time slot-number is binary coded.

0 0 0 0: Time slot 0 is selected

0 0 0 1: Time slot 1 is selected

....

1 01 0: Time slot 10 is selected

1 01 1: Time slot 11 is selected

3.4 COP Command

With a COP command coefficients for the programmable filters can be written to the SICOFI-2/4-TE coefficient-RAM or read from the Coefficient-RAM via the µ-Controller interface for verification

Bit 7 … 0

AD2	AD1	RW	0	CODE3	CODE2	CODE1	CODE0

AD2-1 Address

AD2-1 = 0 0	SICOFI2/4-TE- channel 1 is addressed
AD2-1 = 0 1	SICOFI2/4-TE- channel 2 is addressed
AD2-1 = 1 0	SICOFI2/4-TE- channel 3 is addressed (PSB 2134 only)
AD2-1 = 1 1	SICOFI2/4-TE- channel 4 is addressed (PSB 2134 only)

RW Read/Write

RW = 0	Subsequent data is written to the SICOFI2/4-TE
RW = 1	Read data from SICOFI2/4-TE

CODE 3-0 Includes number of following bytes and filter-address

0	0	0	0	TH-Filter coefficients (part 1)	(followed by 8 bytes of data)
0	0	0	1	TH-Filter coefficients (part 2)	(followed by 8 bytes of data)
0	0	1	0	TH-Filter coefficients (part 3)	(followed by 8 bytes of data)
0	1	0	0	IM/R1-Filter coefficients (part 1)	(followed by 8 bytes of data)
0	1	0	1	IM/R1-Filter coefficients (part 2)	(followed by 8 bytes of data)
0	1	1	0	FRX-Filter coefficients	(followed by 8 bytes of data)
0	1	1	1	FRR-Filter coefficients	(followed by 8 bytes of data)
1	0	0	0	AX-Filter coefficients	(followed by 4 bytes of data)
1	0	0	1	AR-Filter coefficients	(followed by 4 bytes of data)
1	1	0	0	TG 1- coefficients	(followed by 4 bytes of data)
1	1	0	1	TG 2- coefficients	(followed by 4 bytes of data)

How to Program the Filter Coefficients

TH-Filter: Two (Four) sets of TH-filter coefficients can be loaded to the SICOFI2 (/4)-TE. Each sets can be selected for any of the two / four SICOFI2/4-TE channels, by setting the value of TH-Sel in configuration register CR0. Coefficient set 1 is loaded to the SICOFI2/4-TE via channel 1, set 2 is loaded via channel 2 and so on. For the SICOFI2-TE, only set 1 and 2 are available.

AX, AR, IM/R1, FRX, FRR-Filter, Tone-Generators:

An individual coefficient set is available for each of the two / four channels.

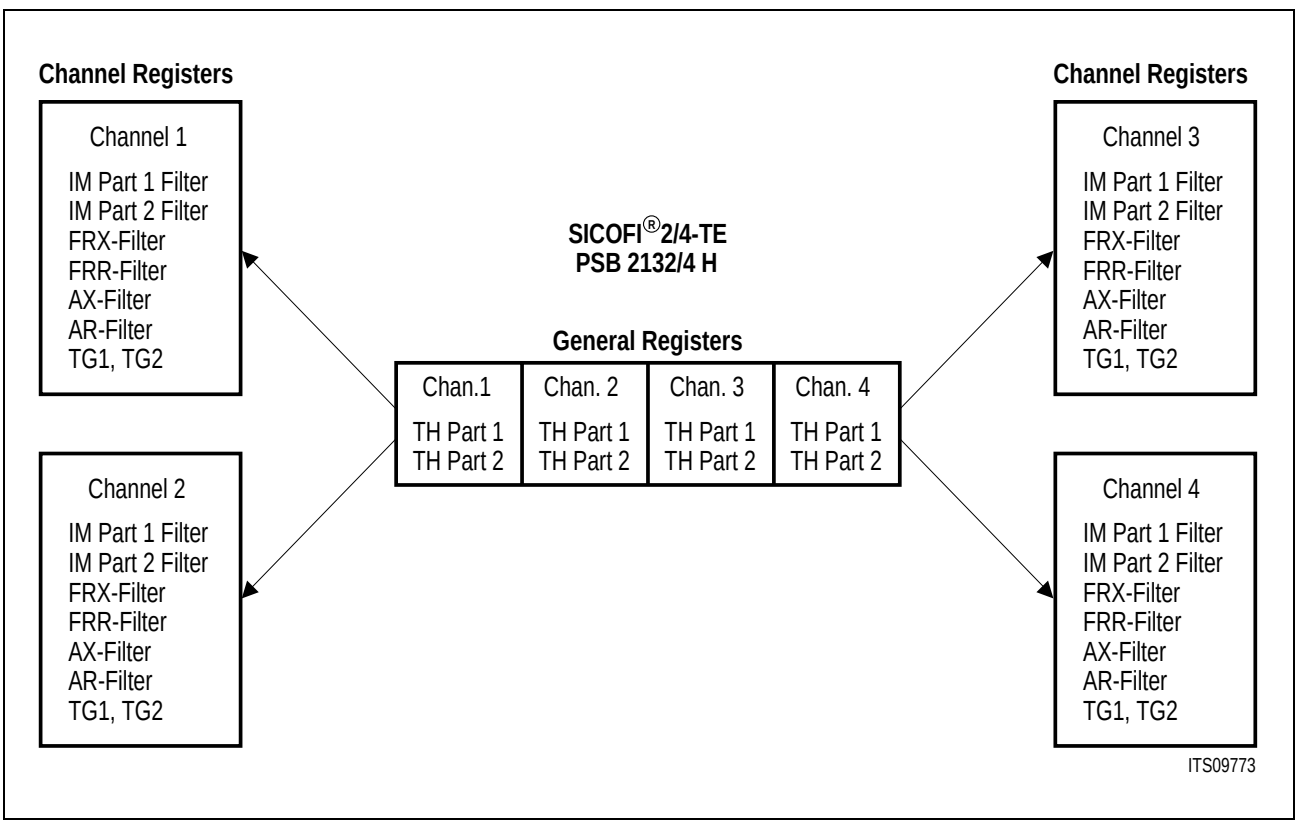


Figure 14

3.5 XOP Command

With the XOP command the SICOFI2/4-TE digital command/indication interface to a SLIC is configured and evaluated. Also other common functions are assigned with this command.

Bit 7 … 0

RST	0	RW	1	1	LSEL2	LSEL1	LSEL0

RST Software Reset

(same as RESET-pin, valid for all 2/4 channels)

RST = 1: Reset

RST = 0: No operation

RW Read / Write Information: Enables reading from the SICOFI-2/4-TE or writing information to the SICOFI2/4-TE

RW = 0: Write to SICOFI2/4-TE

RW = 1: Read from SICOFI2/4-TE

LSEL Length select information, for setting the number of subsequent data bytes

LSEL = 000: 1 byte of data is following (XR0)

LSEL = 001: 2 bytes of data are following (XR1, XR0)

:

LSEL = 111: 8 bytes of data are following (XR7, XR6, XR5, XR4, XR3, XR2, XR1, XR0)

Note: All other codes are reserved for future use!
If only one configuration register requires modification, for example XR5, this can be accomplished by setting LSEL =101 and releasing pin CS after XR5 is written.

3.5.1 XR0 Extended Register 0

The signaling connection between SICOFI2/4-TE and a SLIC is performed by master device the SICOFI2/4-TE signaling input and output pins and Configuration Register XR0... XR4. Data received from the upstream master device are transferred to signaling output pins (SO, SB). Data at the signaling input pins are transferred to the upstream controller.

In Connection with XOP-Read Commands

Bit 7 0

0	**0**	**0**	**0**	**SI2_1**	**SI2_0**	**SI1_1**	**SI1_0**
SI4_1	**SI4_0**	**SI3_1**	**SI3_0**	**SI2_1**	**SI2_0**	**SI1_1**	**SI1_0**

PSB 2134 only

SI4_1 Status of pin SI4_1 is transferred to the upstream master device

SI4_0 Status of pin SI4_0 is transferred to the upstream master device

SI3_1 Status of pin SI3_1 is transferred to the upstream master device

SI3_0 Status of pin SI3_0 is transferred to the upstream master device

Common

SI2_1 Status of pin SI2_1 is transferred to the upstream master device

SI2_0 Status of pin SI2_0 is transferred to the upstream master device

SI1_1 Status of pin SI1_1 is transferred to the upstream master device

SI1_0 Status of pin SI1_0 is transferred to the upstream master device

In Connection with XOP-Write Commands

Bit 7 0

0	**0**	**0**	**0**	**SO2_1**	**SO2_0**	**SO1_1**	**SO1_0**
SO4_1	**SO4_0**	**SO3_1**	**SO3_0**	**SO2_1**	**SO2_0**	**SO1_1**	**SO1_0**

PSB 2134 only

SO4_1 Pin SO4_1 is set to the assigned value

SO4_0 Pin SO4_0 is set to the assigned value

SO3_1 Pin SO3_1 is set to the assigned value

SO3_0 Pin SO3_0 is set to the assigned value

Common

SO2_1	Pin SO2_1 is set to the assigned value
SO2_0	Pin SO2_0 is set to the assigned value
SO1_1	Pin SO1_1 is set to the assigned value
SO1_0	Pin SO1_0 is set to the assigned value

3.5.2 XR1 Extended Register 1

This register transfers information to or from the programmable signaling pins.

Bit 7 0

0	**0**	**0**	**0**	**SB2_1**	**SB2_0**	**SB1_1**	**SB1_0**
SB4_1	**SB4_0**	**SB3_1**	**SB3_0**	**SB2_1**	**SB2_0**	**SB1_1**	**SB1_0**

In Connection with a XOP-Read Command

PSB 2134 only

SB4_1 If input: status of pin SB4_1 is transferred upstream

SB4_0 If input: status of pin SB4_0 is transferred upstream

SB3_1 If input: status of pin SB3_1 is transferred upstream

SB3_0 If input: status of pin SB3_0 is transferred upstream

Common

SB2_1 If input: status of pin SB2_1 is transferred upstream

SB2_0 If input: status of pin SB2_0 is transferred upstream

SB1_1 If input: status of pin SB1_1 is transferred upstream

SB1_0 If input: status of pin SB1_0 is transferred upstream

In Connection with a XOP-Write Command

PSB 2134 only

SB4_1 If output: pin SB4_1 is set to the assigned value

SB4_0 If output: pin SB4_0 is set to the assigned value

SB3_1 If output: pin SB3_1 is set to the assigned value

SB3_0 If output: pin SB3_0 is set to the assigned value

Common

SB2_1 If output: pin SB2_1 is set to the assigned value

SB2_0 If output: pin SB2_0 is set to the assigned value

SB1_1 If output: pin SB1_1 is set to the assigned value

SB1_0 If output: pin SB1_0 is set to the assigned value

Note: After a ‘Reset’ of the device, all programmable pins are input pins!

3.5.3 XR2 Extended Register 2

This register controls the direction of the programmable signaling pins.

Bit 7 0

0	**0**	**0**	**0**	**PSB2_1**	**PSB2_0**	**PSB1_1**	**PSB1_0**
PSB4_1	**PSB4_0**	**PSB3_1**	**PSB3_0**	**PSB2_1**	**PSB2_0**	**PSB1_1**	**PSB1_0**

PSB 2134 only

PSB4_1 Programmable bi-directional signaling pin SB4_1 is programmed
PSB4_1 = 0: Pin SB4_1 is indication input
PSB4_1 = 1: Pin SB4_1 is command output

PSB4_0 Programmable bi-directional signaling pin SB4_0 is programmed
PSB4_0 = 0: pin SB4_0 is indication input
PSB4_0 = 1: Pin SB4_0 is command output

PSB3_1 Programmable bi-directional signaling pin SB3_1 is programmed
PSB3_1 = 0: Pin SB3_1 is indication input
PSB3_1 = 1: Pin SB3_1 is command output

PSB3_0 Programmable bi-directional signaling pin SB3_0 is programmed
PSB3_0 = 0: Pin SB3_0 is indication input
PSB3_0 = 1: Pin SB3_0 is command output

Common

PSB2_1 Programmable bi-directional signaling pin SB2_1 is programmed
PSB2_1 = 0: Pin SB2_1 is indication input
PSB2_1 = 1: Pin SB2_1 is command output

PSB2_0 Programmable bi-directional signaling pin SB2_0 is programmed
PSB2_0 = 0: Pin SB2_0 is indication input
PSB2_0 = 1: Pin SB2_0 is command output

PSB1_1 Programmable bi-directional signaling pin SB1_1 is programmed
PSB1_1 = 0: Pin SB1_1 is indication input
PSB1_1 = 1: Pin SB1_1 is command output

PSB1_0 Programmable bi-directional signaling pin SB1_0 is programmed

PSB1_0 = 0: Pin SB1_0 is indication input

PSB1_0 = 1: Pin SB1_0 is command output

Note: After a 'Reset' of the device, all programmable pins are input pins!

3.5.4 XR3 Extended Register 3

This register transfers information to or from the programmable signaling pins and configures these pins.

Bit 7 0

0	**0**	**SB2_2**	**SB1_2**	**0**	**0**	**PSB2_2**	**PSB1_2**
SB4_2	**SB3_2**	**SB2_2**	**SB1_2**	**PSB4_2**	**PSB3_2**	**PSB2_2**	**PSB1_2**

In Connection with a XOP-Read Command

PSB 2134 only

SB4_2 If input: status of pin SB4_2 is transferred upstream

SB3_2 If input: status of pin SB3_2 is transferred upstream

Common

SB2_2 If input: status of pin SB2_2 is transferred upstream

SB1_2 If input: status of pin SB1_2 is transferred upstream

In Connection with a XOP-Write Command

PSB 2134 only

SB4_2 If output: pin SB4_2 is set to the assigned value

SB3_2 If output: pin SB3_2 is set to the assigned value

Common

SB2_2 If output: pin SB2_2 is set to the assigned value

SB1_2 If output: pin SB1_2 is set to the assigned value

PSB 2134 only

PSB4_2 Programmable bi-directional signaling pin SB4_2 is programmed

PSB4_2 = 0: Pin SB4_2 is indication input

PSB4_2 = 1: Pin SB4_2 is command output

PSB3_2 Programmable bi-directional signaling pin SB3_2 is programmed

PSB3_2 = 0: Pin SB3_2 is indication input

PSB3_2 = 1: Pin SB3_2 is command output

Common

PSB2_2 Programmable bi-directional signaling pin SB2_2 is programmed

PSB2_2 = 0: Pin SB2_2 is indication input

PSB2_2 = 1: Pin SB2_2 is command output

PSB1_2 Programmable bi-directional signaling pin SB1_2 is programmed

PSB1_2 = 0: Pin SB1_2 is indication input

PSB1_2 = 1: Pin SB1_2 is command output

Note: After a 'Reset' of the device, all programmable pins are input pins!

3.5.5 XR4 Extended Register 4

Register XR4 provides two optional functions: debouncing of signaling input changes, and the configuration of the programmable ring generator output pin RGEN.

Bit 7 0

N	T

Signaling Debounce Interval N

To restrict the rate of changes on signaling input pins transferred, deglitching of the status information from the SLIC may be applied. New status information will be read into registers XR0, XR1, XR2 and XR3, and an interrupt on pin INT12 (INT34) will be generated, after it has been stable for N milliseconds. N is programmable in the range of 2 to 26ms in steps of 2 ms, with N = 0 the debouncing is disabled. The last two bit combinations are reserved for future use.

Field N				Debounce Interval Time
0	0	0	0	Debounce and interrupt generation is disabled
0	0	0	1	Debounce period 2 ms
0	0	1	0	Debounce period 4 ms
.	.	.	.	.
1	1	0	1	Debounce period 26 ms
1	1	1	0	reserved
1	1	1	1	reserved

Configuration of RGEN

Field T				Frequency applied to Pin RGEN
0	0	0	0	RGEN is set to 1 permanently
0	0	0	1	T is 2ms
0	0	1	0	T is 4ms
.	.	.	.	.
.	.	.	.	.
1	1	1	0	T is 28 ms
1	1	1	1	RGEN is set to 0 permanently

3.5.6 XR5 Extended Register 5

This register contains additional configuration items valid for all 2/4 channels

Bit 7 0

0	0	CR_DU	CR_DD	CHCLK	Version

CR_DU Crash[1] on DU (read only)

0: No crash detected

1: Crash detected (bad programming in CR5-registers)

CR_DD

Crash on DD (read only)

0: No crash detected

1: Crash detected (bad programming in CR5-registers)

CHCLK Enables Chopper Clock Output to pin CHCLK

0 0: pin CHCLK is set to 1

0 1: A 512 kHz signal is fed to pin CHCLK

1 0: A 256 kHz signal is fed to pin CHCLK

1 1: A 16384 kHz signal (internal masterclock) is fed to pin CHCLK

(at least one of the two / four channels has to be set to 'POWER UP' and DCL must be provided)

VERSION This two bit field identifies the actual chip version,

is '01' for Version 1.2

[1] A crash occurs, if 2 or more channels are programed to transmit (talk) in the same time slot on the same line. In this case the crash-bit will be set, and transmission will be disabled for all affected channels.

3.5.7 XR6 Extended Register 6

This register configures the operation of the PCM-interface

Bit 7 0

0	X-S	R-S	DRV_0	0	PCM-OFFSET

X-S Transmit Slope

	X-S = 0:	Transmission starts with rising edge of BCL
	X-S = 1:	Transmission starts with falling edge of BCL
R-S	Receive Slope	
	R-S= 0:	Data is sampled with falling edge of BCL
	R-S= 1:	Data is sampled with rising edge of BCL
DRV_0	Driving Mode for Bit 0	
	DRV_0 = 0:	Bit 0 is driven the whole BCL-period
	DRV_0 = 1:	Bit 0 is driven during the first half of the BCL-period only
PCM-OFFSET	Offset in number of data-clock periods added to Time slot	
	0 0 0:	No offset is added
	0 0 1:	One data clock period is added
	...	
	1 1 1	Seven data clock periods are added

3.5.8 XR7 Extended Register 7

This register contains the 8-bit offset value for the level metering function

Bit 7 0

OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0

3.5.9 Setting of Slopes in Register XR6

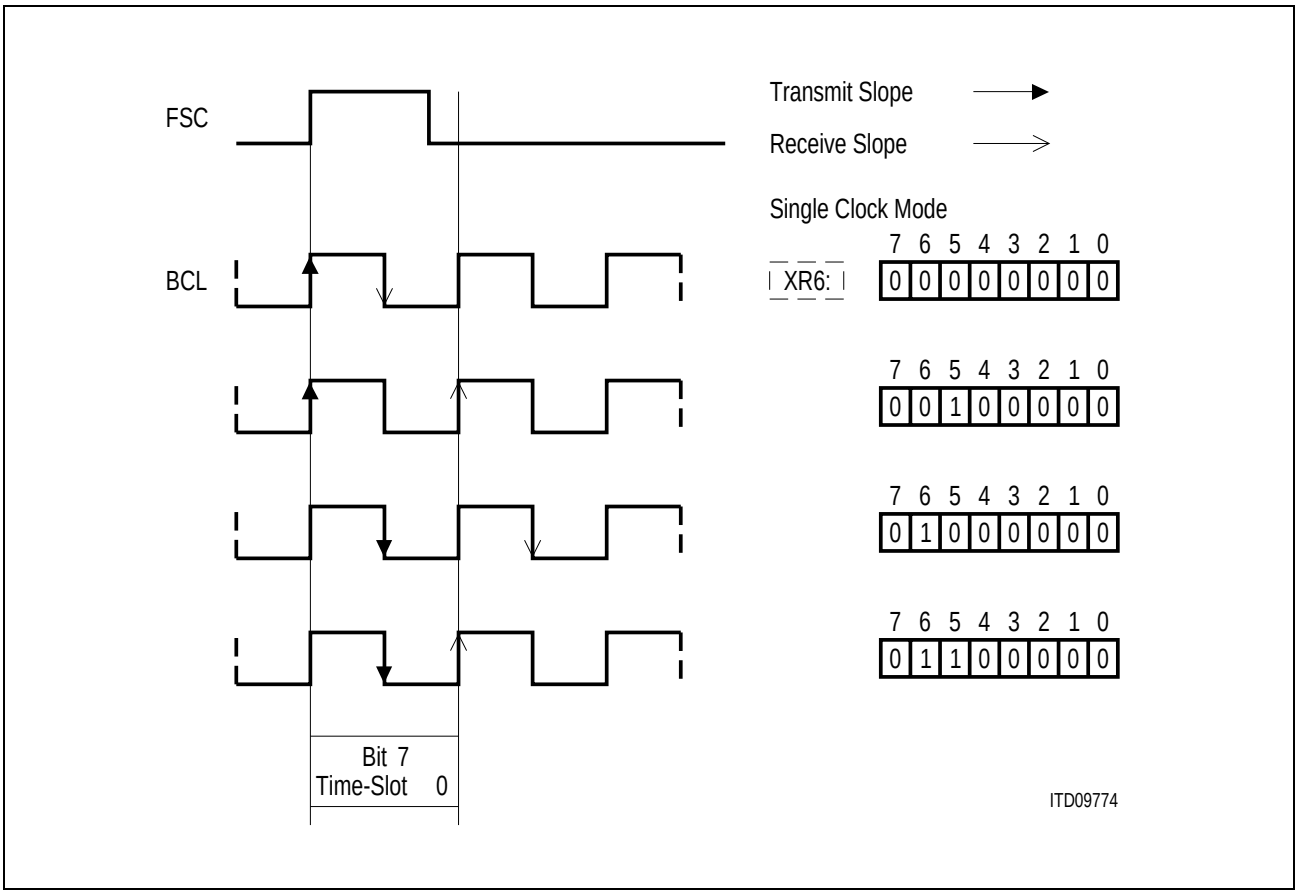


Figure 15

3.6 Operating Modes

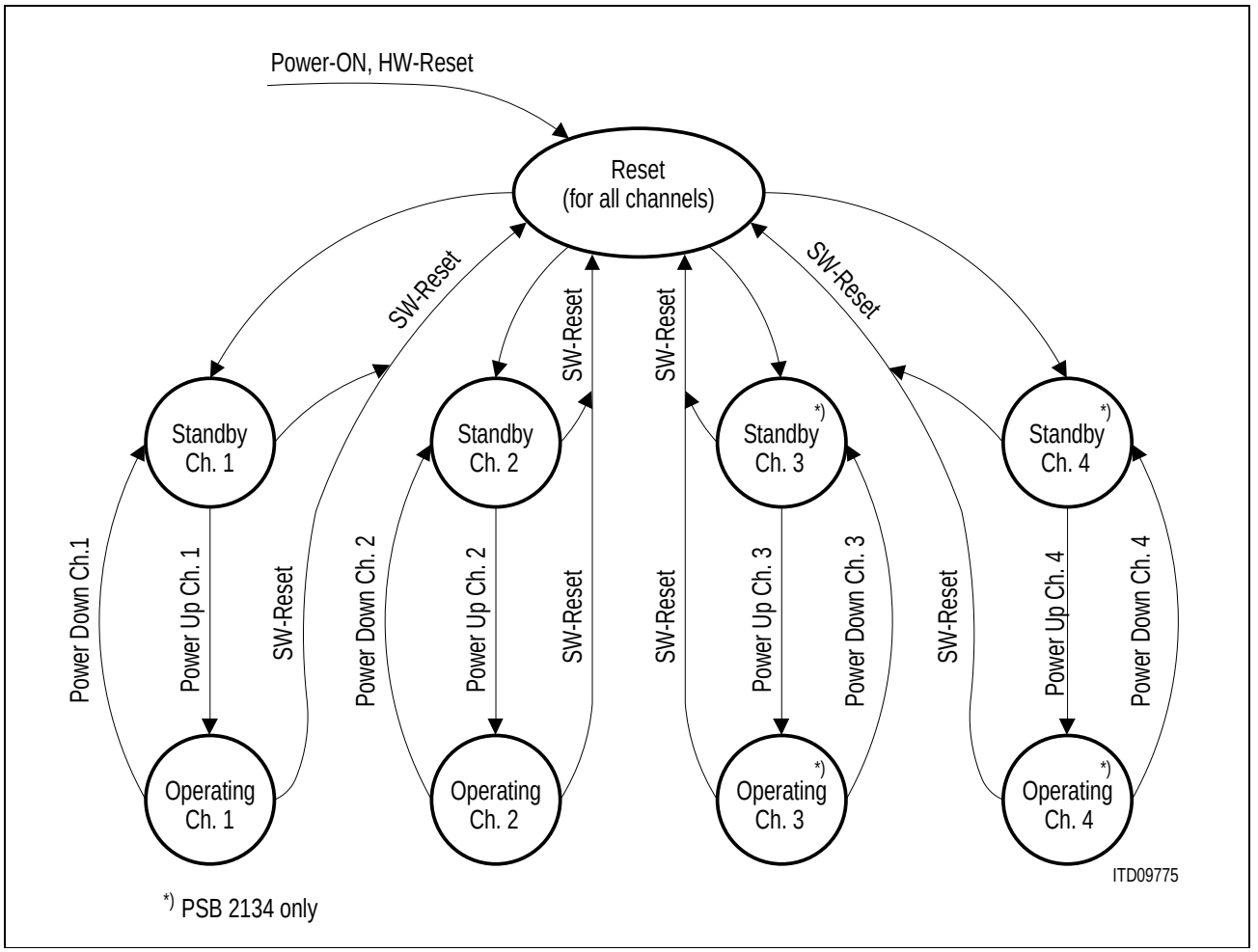


Figure 16

3.6.1 RESET (Basic Setting Mode)

Upon initial application of V_{DD} or resetting pin RESET to '0' during operation, or by software-reset (see XOP command), the SICOFI2/4-TE enters a basic setting mode. Basic setting means, that the SICOFI2/4-TE configuration registers CR0... CR6 and XR0... XR7 are initialized to '0' for all channels.

All programmable filters are disabled, all programmable command/indication pins are inputs. The two tone generators as well as any testmodes are disabled. There is no persistence checking. Receive signaling registers are cleared. DOUT-pin is in high impedance state, the analog outputs and the signaling outputs are forced to ground.

CR0.. CR6	00_H
XR0.. XR7	00_H
Coefficient-RAM	Old value

Command Stack	Cleared
DIN-input	Ignored
DOUT-output	High impedance
VOUT1,2 or 1,2,3,4	GNDA1,2 or 1,2,3,4
SBx_y	Input
SOx_y	GNDD

If any voltage is applied to any input-pin before initial application of V_{DD}, the SICOFI2/4-TE may not enter the basic setting mode. In this case it is necessary to reset the SICOFI2/4-TE or to initialize the SICOFI2/4-TE configuration registers to '0'.

The SICOFI2/4-TE leaves this mode automatically after the RESET-pin is released.

3.6.2 Standby Mode

After releasing the RESET-pin, (RESET-state), the SICOFI2/4-TE will enter the Standby mode. The SICOFI2/4-TE is forced to standby mode with the PU-bit set to '0' in the CR1-register (POWERDOWN). All 2/4 channels must be programmed separately. During standby mode the serial SICOFI2/4-TE µ-Controller interface is ready to receive and transmit commands and data. Received voice data on DU, DD-pin will be ignored. SICOFI2/4-TE configuration registers and Coefficient-RAM can be loaded and read back in this mode. Data on signaling input pins can be read via the µ-Controller interface.

DU, DD	High 'Z'
VOUT1, 2, 3, 4	GNDA1, 2, 3, 4

3.6.3 Active Mode (Power Up)

The operating mode for any of the four channels is entered upon recognition of a PU-bit set to '1' in a CR1-register for the specific channel.

3.6.4 Programmable Filters

Based on an advanced digital filter concept, the SICOFI-2/4 TE provides excellent transmission performance and high flexibility. The new filter concept leads to a maximum independence between the different filter blocks.

Impedance Matching Filter

- Realization by 3 different loops
  - 4 MHz: Multiplication by a constant (12 bit)
  - 128 kHz: Wave Digital Filter (IIR) (60 bit)
    Improves low frequency response
  - 64 kHz: FIR-Filter (48 bit)
    For fine-tuning
- Improved stability behavior of feedback loops
- Real part of termination impedance positive under all conditions
- Improved overflow performance for transients
- Return loss better 30 dB

Transhybrid Balancing (TH) Filter

- New concept: 2 loops at 16 kHz
- Flexible realization allows optimization of wide impedance range
- Consists of a fixed and a programmable part
  - 2nd order Wave Digital Filter (IIR) (106 bit)
    Improves low frequency response
  - 7-TAP FIR-Filter (84 bit)
    For fine-tuning
- Trans-Hybrid-Loss better 30 dB (typically better 40 dB, device only)
- Adaptation to different lines by:
  - Easy selection between four different downloaded coefficient sets

Filters for Frequency Response Correction

- For line equalization and compensation of attenuation distortion
- Improvement of Group-Delay-Distortion by using minimum phase filters (instead of linear phase filters)
- FRR filter for correction of receive path distortion
  – 5 TAP programmable FIR filter operating at 8 kHz (60 bit)
- FRX filter for correction of transmit path distortion
  – 5 TAP programmable FIR filter operating at 8 kHz (60 bit)
- Frequency response better 0.1 dB

Amplification/Attenuation -Filters AX1, AX2, AR1, AR2

- Improved level adjustment for transmit and receive
- Two separate filters at each direction for
  – Improved trans-hybrid balancing
  – Optimal adjustment of digital dynamic range
  – Gain adjustments independent of TH-filter

Amplification/Attenuation Receive (AR1, AR2)-Filter

Step size for AR-Filter	range 3 .. – 14 dB:	step size 0.02 .. 0.05 dB
	range – 14 .. – 24	step size 0.5 dB

Amplification/Attenuation Transmit (AX1, AX2)-Filter

Step size for AX-Filter	range – 3 .. 14 dB:	step size 0.02 .. 0.05 dB
	range 14 .. 24 dB:	step size 0.5 dB

3.6.5 QSICOS Software

The QSICOS-software has been developed to help to obtain an optimized set of coefficients both quickly and easily. The QSICOS program runs on any PC with at least 575 Kbytes of memory. This also requires MS-DOS Version 5.0 or higher, as well as extended memory.

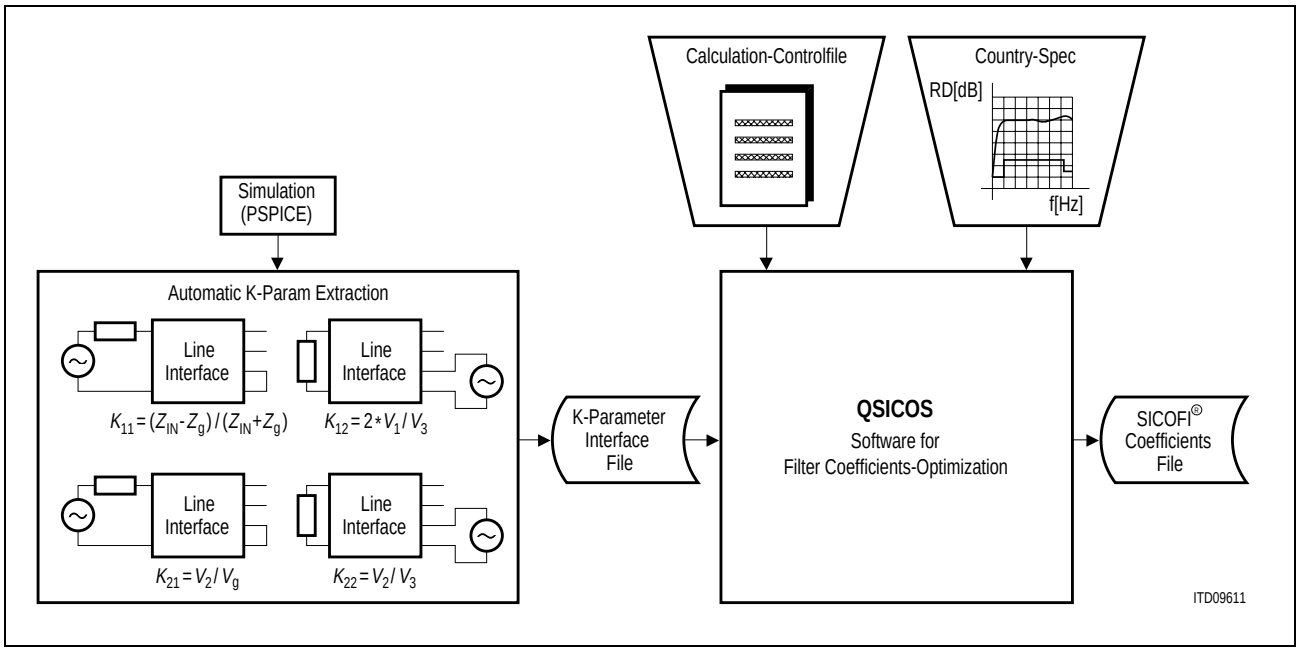


Figure 17

QSICOS Supports:

- **Calculation of Coefficients for the SICOFI2/4-TE**
  - Impedance Filter (IM) for return loss calculation (please note that the IM filter coefficients are different for the SICOFI2/4-TE and for the PEB 2465. QSICOS calculates the programming bytes for the SICOFI-4 IOM version PEB 2465. These bytes have to be converted with an additional tool to get the required SICOFI-2/4 TE programming bytes. The conversion tool QSUCCONV.EXE is part of the QSICOS software package.)
  - FRR and FRX-filters for frequency response in receive and transmit path
  - AR1, AR2 and AX1, AX2-filter for level adjustment in receive and transmit path
  - Transhybrid Balancing Filter (TH) and
  - Two programmable tone generators (TG 1 and TG 2)
- **Simulation of the SICOFI-2/4 TE and SLIC System** with fixed filter coefficients allows simulations of tolerances which may be caused e.g. by discrete external components.
- **Graphical Output of Transfer Functions to the Screen** for
  - Return Loss
  - Frequency responses in receive and transmit path
  - Transhybrid Loss
- **Calculation of the SICOFI-2/4 TE and SLIC system Stability**. The IM-filter of the SICOFI-2/4 TE adjust the total system impedance by making a feedback loop. Because the line is also a part of the total system, a very robust method has to used to avoid oscillations and to ensure system stability. The input impedance of the

SICOFI-2/4 TE and SLIC combination is calculated. If the real part of the system input impedance is positive, the total system stability can be guaranteed.

In addition to the individual calculation of coefficient sets Siemens will provide ready to use coefficient sets for selected SLICs.

Please contact your Siemens office for available information.

4 Transmission Characteristics

The figures in this specification are based on the subscriber-line board requirements. The proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) requires a complete knowledge of the SICOFI-2/4 TE's analog environment. Unless otherwise stated, the transmission characteristics are guaranteed within the test conditions.

Test Conditions

T_A = 0 °C to 70 °C; V_{DD} = 5 V ± 5%; GNDA1..4 = GNDD = 0 V
R_L [1] > 300 Ω; C_L < 50 pF; H(IM) = H(TH) = 0; H(R1) = H(FRX) = H(FRR) = 1;
HPR and HPX enabled;
AR[2]= 0 to – 8 dB
AX[3]= 0 to 8 dB for A-Law, 0 to 6 dB for µ-Law
f = 1014 Hz; 0 dBm0; A-Law or µ-Law;

AGX = 0 dB, 6.02 dB, AGR = 0 dB, – 6.02dB;

A-Law

A 0 dBm0 signal is equivalent to 1.095 Vrms. A + 3.14 dBm0 signal is equivalent to 1.57 Vrms which corresponds to the overload point of 2.223 V.

When the gain in the receive path is set at 0 dB, an 1014 Hz PCM sinewave input with a level 0 dBm0 will correspond to a voltage of 1.095 Vrms at the analog output.

When the gain in the transmit path is set at 0 dB, an 1014 Hz sine wave signal with a voltage of 1.095Vrms A-Law will correspond to a level of 0 dBm0 at the PCM output.

µ-Law

In transmit direction for µ-law an additional gain of 1.94 dB is implemented automatically, in the companding block (CMP). This additional gain has to be considered at all gain calculations, and reduces possible AX-gain from 8 dB (with A-Law) to 6 dB (with µ-Law)

A 0 dBm0[4] signal is equivalent to 1.0906 Vrms. A + 3.17 dBm0 signal is equivalent to 1.57 Vrms which corresponds to the overload point of 2.223 V.

When the gain in the receive path is set at 0 dB, an 1014 Hz PCM sinewave input with a level 0 dBm0 will correspond to a voltage of 1.0906 Vrms at the analog output.

When the gain in the transmit path is set at 0 dB, an 1014 Hz sine wave signal with a voltage of 1.0906 Vrms will correspond to a level of 1.94 dBm0 at the PCM output.

---

1) R_L, C_L forms the load on VOUT
2) Consider, in a complete system, AR = AR1 + AR2 + FRR + R1
3) Consider, in a complete system, AX = AX1 + AX2 + FRX
4) The absolute power level in decibels referred to (a point of zero relative level) the PCM interface levels.

Transmission Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Gain absolute (AGX = AGR = 0) T_A= 25 °C; V_{DD} = 5 V T_A = 0 – 70 °C; V_{DD} = 5 V ± 5%	G	 – 0.80 – 0.90	 ± 0.10	 + 0.80 + 0.90	 dB dB
Gain absolute (AGX = 6.02 dB, AGR = – 6.02 dB) T_A = 25°C; V_{DD} = 5 V T_A = 0-70°C; V_{DD} = 5 V ± 5%	G	 – 0.85 – 0.95	 ± 0.10	 + 0.85 + 0.95	 dB dB
Harmonic distortion, 0 dBm0; f = 1000 Hz; 2nd, 3rd order	HD		– 44		dB
Intermodulation[1)] R_2 R_3	IMD IMD		– 46 – 56		dB dB
Crosstalk 0 dBm0; f = 200 Hz to 3400 Hz any combination of direction and channel	CT		– 80	– 75	dB
Idle channel noise, Transmit, A-law, psophometric (V_{IN} = 0 V) Transmit, µ-law, C-message (V_{IN} = 0V) Receive, A-law, psophometric (idle code + 0) Receive, µ-law, C-message (idle code + 0)	 N_{TP} N_{TC} N_{RP} N_{RC}		 – 85 5	 – 66.0 19.0 – 77.0 13.0	 dBm0p dBrnc0 dBm0p dBrnc0

1) Using equal-level, 4-tone method (EIA) at a composite level of – 13 dBm0 with frequencies in the range between 300 Hz and 3400 Hz.

4.1 Frequency Response

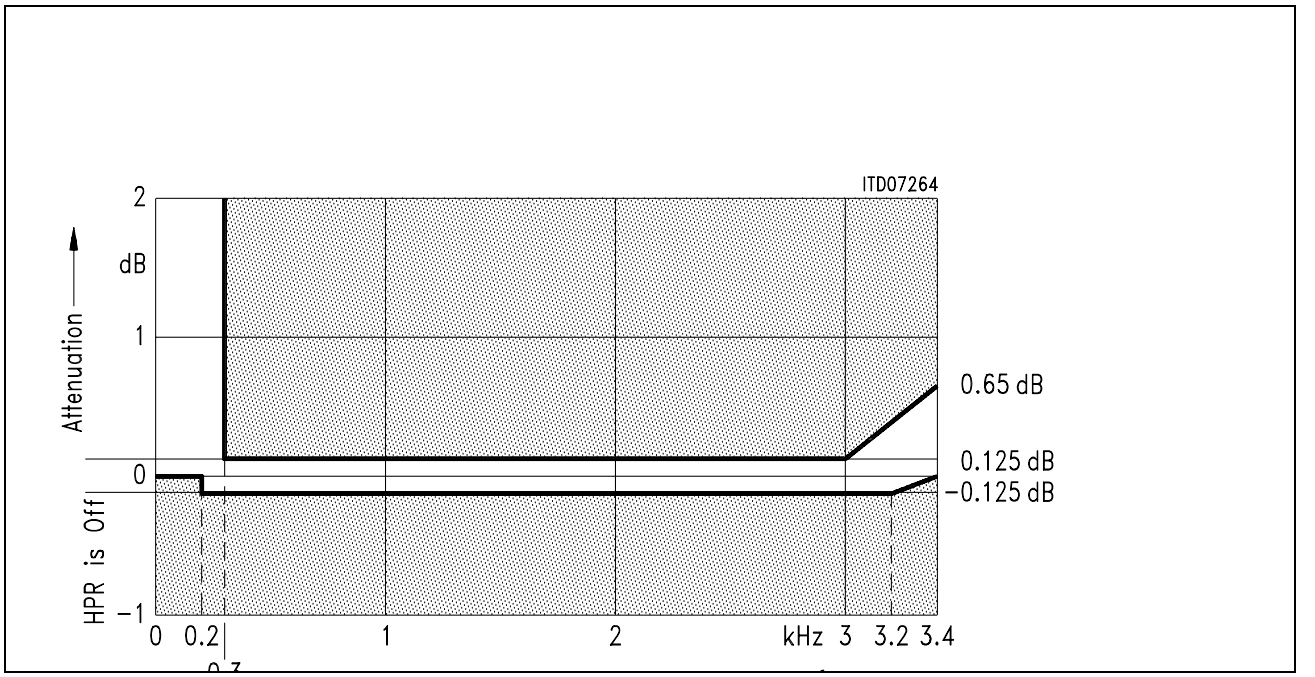


Figure 18
Receive: Reference Frequency 1014 Hz, Input Signal Level 0 dBm0

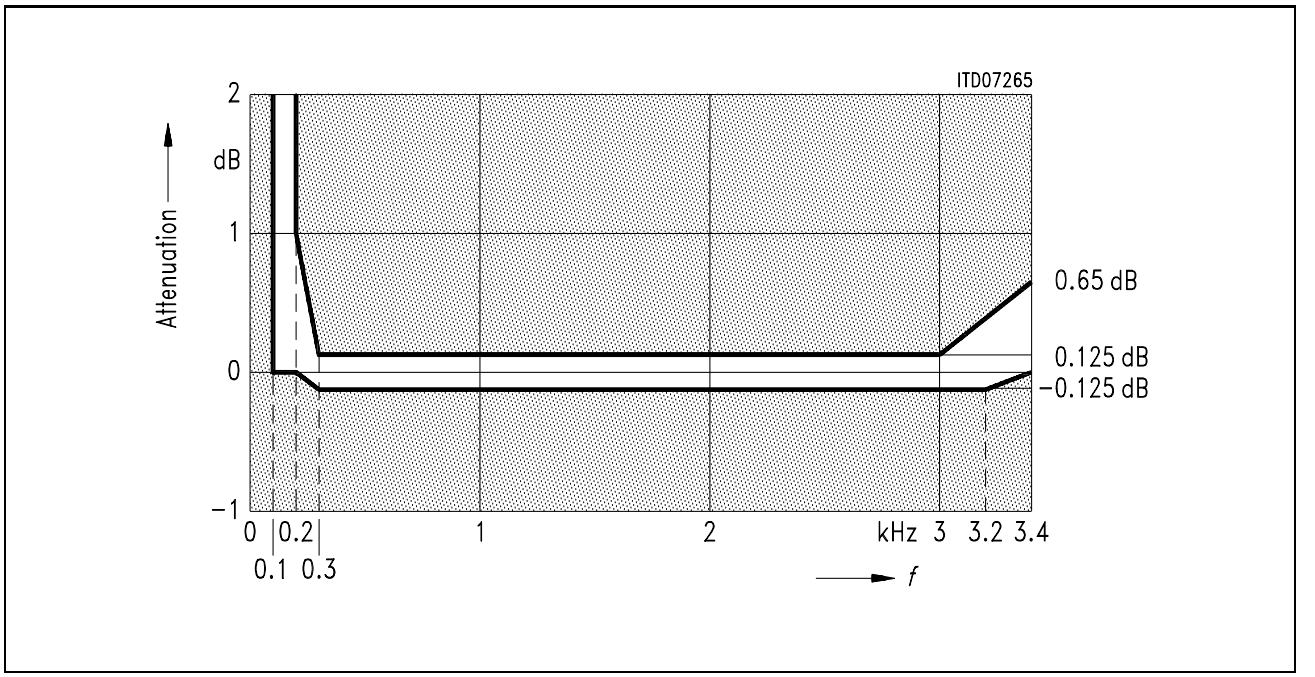


Figure 19
Transmit: Reference Frequency 1014 Hz, Input Signal Level 0 dBm0

4.2 Group Delay

Maximum delays when the SICOFI2/4-TE is operating with H(TH) = H(IM) = 0 and H(FRR) = H(FRX) = 1 including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

Group delay deviations stay within the limits in the figures below.

Group Delay Absolute Values: Input signal level 0 dBm0

Parameter	Symbol	Limit Values			Unit	Reference
		min.	typ.	max.		
Transmit delay	D_{XA}			300.	µs	
Receive delay	D_{RA}			250	µs	

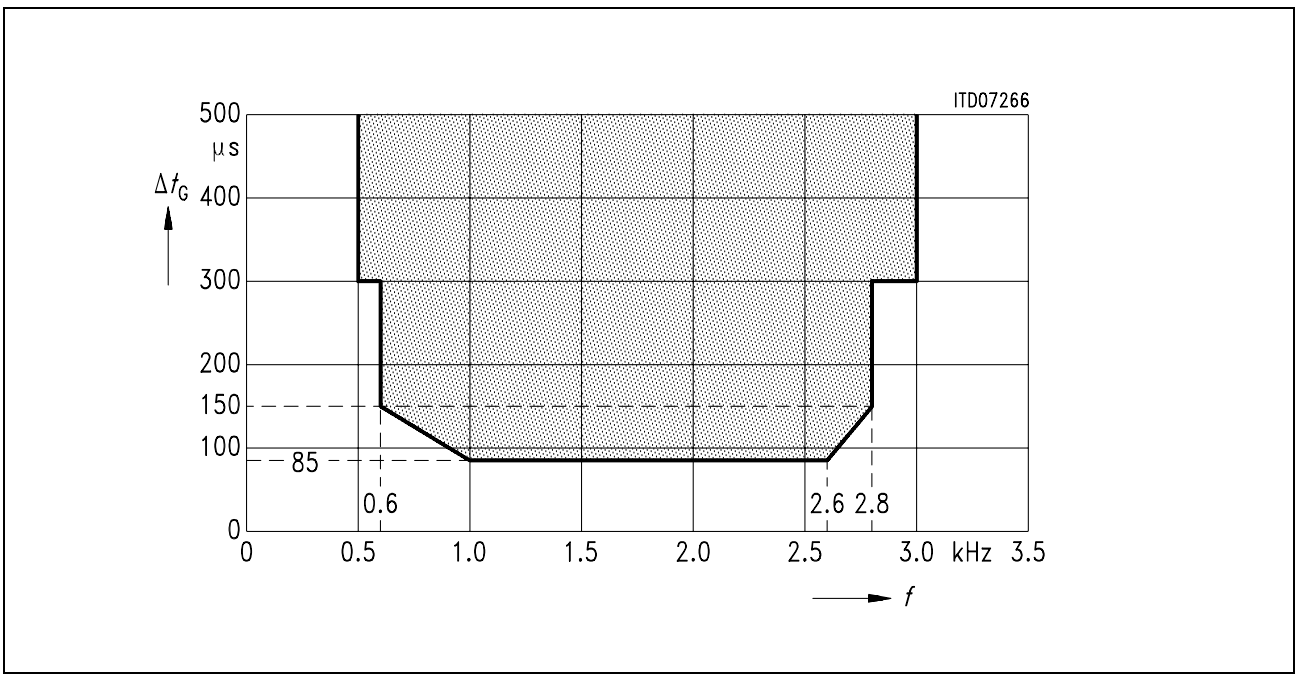


Figure 20
Group Delay Distortion Transmit: Input Signal Level 0 dBm0

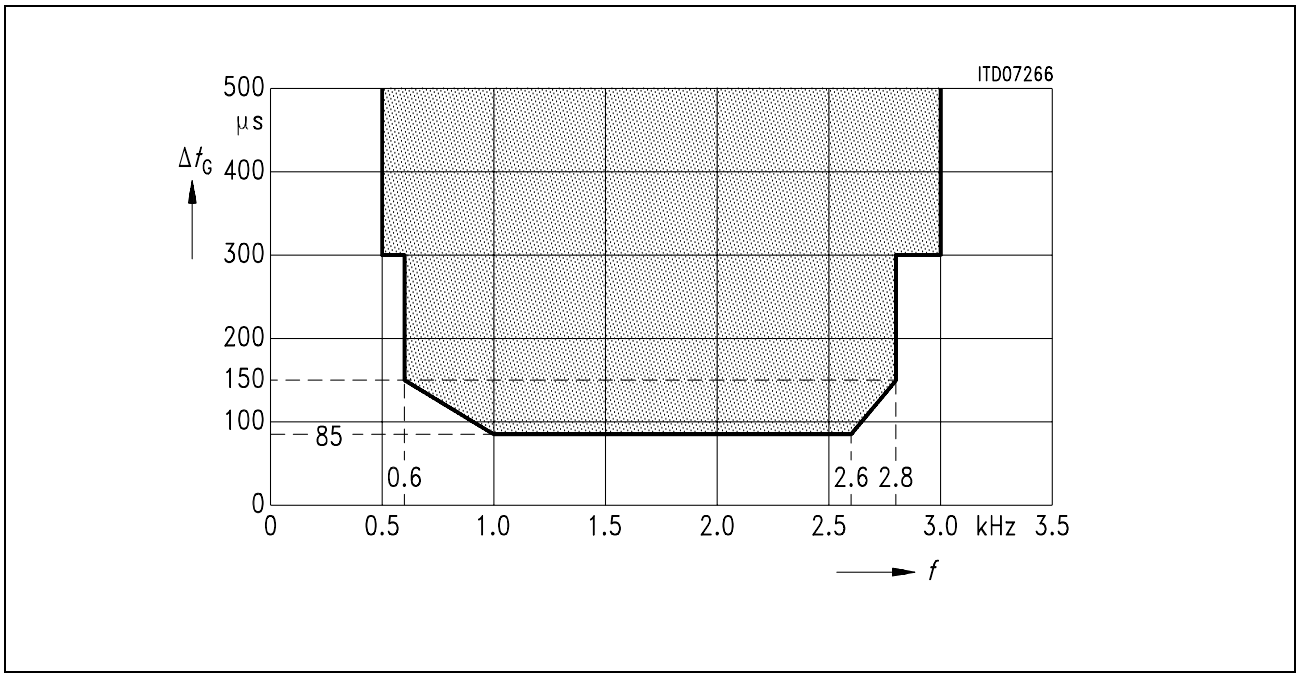
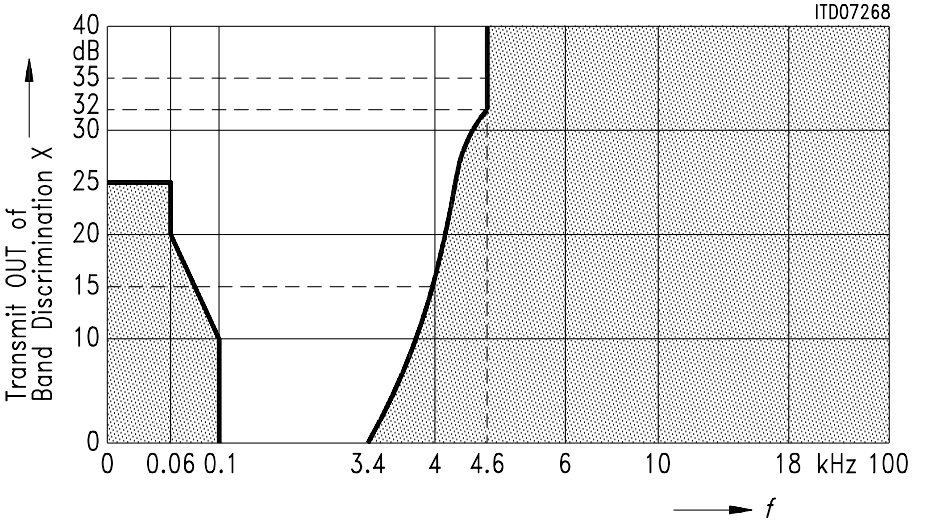


Figure 21
Group Delay Distortion Receive: Input Signal Level 0 dBm0 [1)]

[1)] HPR is switched on: reference point is at t_{Gmin}
HPR is switched off: reference is at 1.5 kHz

4.3 Out-of-Band Signals at Analog Input

With an 0 dBm0 out-of-band sine wave signal with frequency f (<<100 Hz or 3.4 kHz to 100 kHz) applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog input.[1)]



$$3.4 \ldots 4.0 \text{ kHz: } X = -14 \left(\sin \left(\pi \frac{4000 - f}{1200} \right) - 1 \right)$$

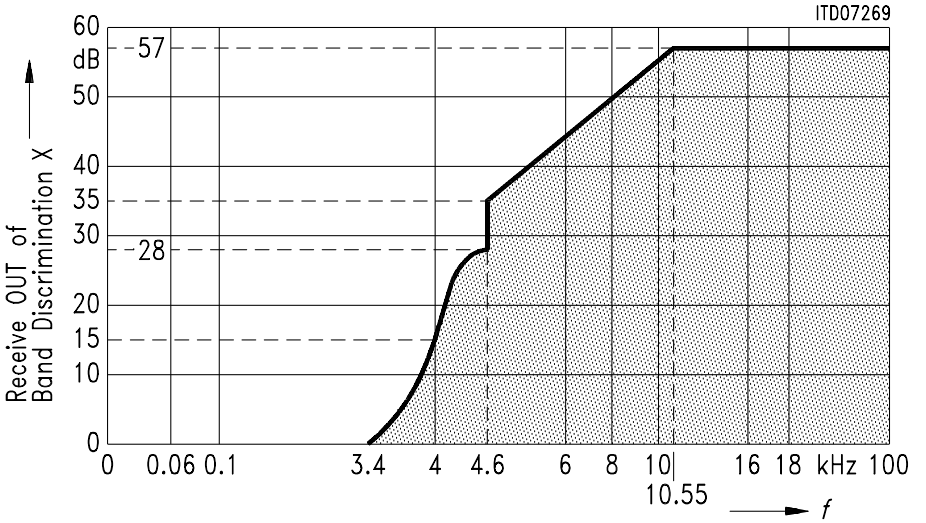
$$4{,}0 \ldots 4.\dot{6} \text{ kHz: } X = -18 \left(\sin \left(\pi \frac{4000 - f}{1200} \right) - \frac{7}{9} \right)$$

Figure 22

1) Poles at 12 kHz ± 150 Hz and 16 kHz ± 150 Hz are provided

4.4 Out-of-Band Signals at Analog Output

With a 0 dBm0 sine wave with frequency f (300 Hz to 3.99 kHz) applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.



$$3.4 \ldots 4.6 \text{ kHz: } X = -14 \left(\sin \left(\pi \frac{4000 - f}{1200} \right) - 1 \right)$$

Figure 23

4.5 Out of Band Idle Channel Noise at Analog Output

With an idle code applied to the digital input, the level of any resulting out-of-band power spectral density (measured with 3 kHz bandwidth) at the analog output, will be not greater than the limit curve shown in the figure below.

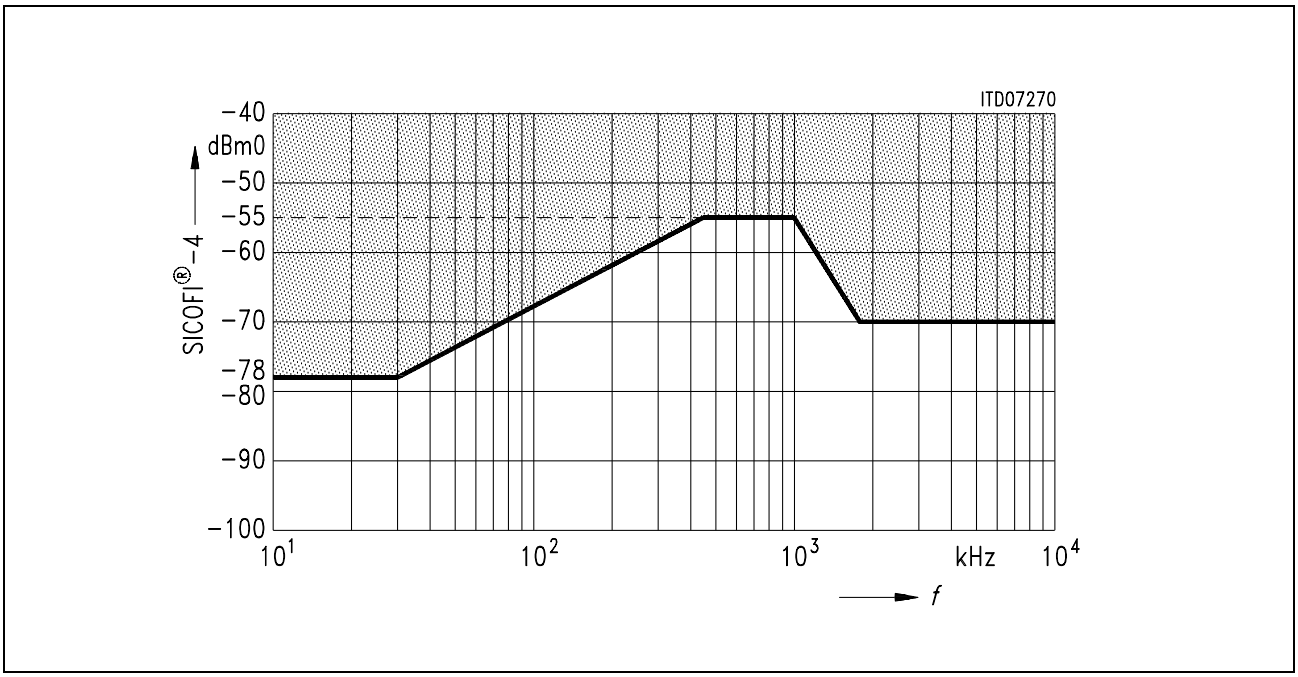


Figure 24

4.6 Overload Compression

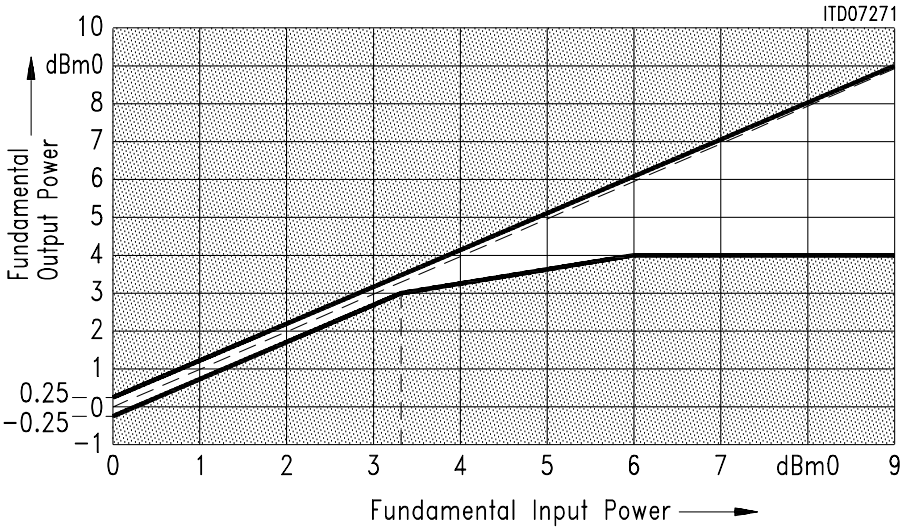


Figure 25
μ-Law, Transmit: measured with sine wave f = 1014 Hz.

4.7 Gain Tracking (receive or transmit)

The gain deviations stay within the limits in the figures below.

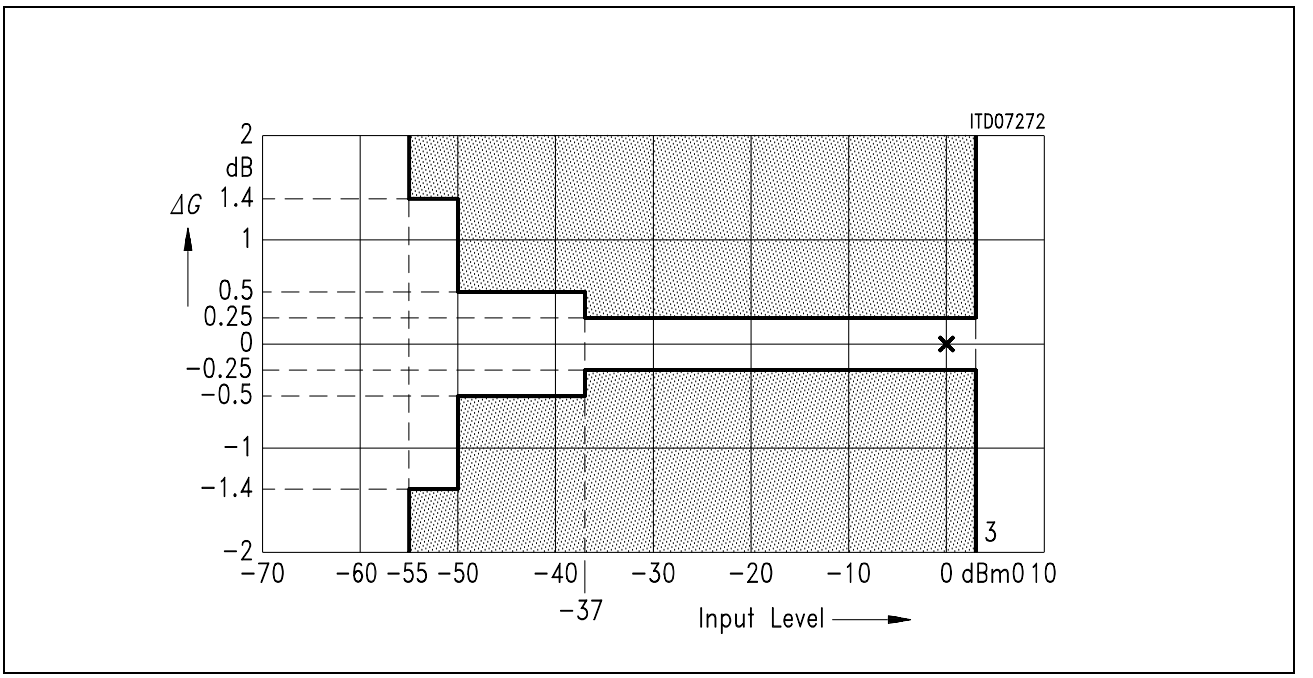


Figure 26
Gain Tracking: (measured with sine wave f = 1014 Hz, reference level is 0 dBm0)

4.8 Total Distortion

The signal to distortion ratio exceeds the limits in the following figure (measured with sine wave).

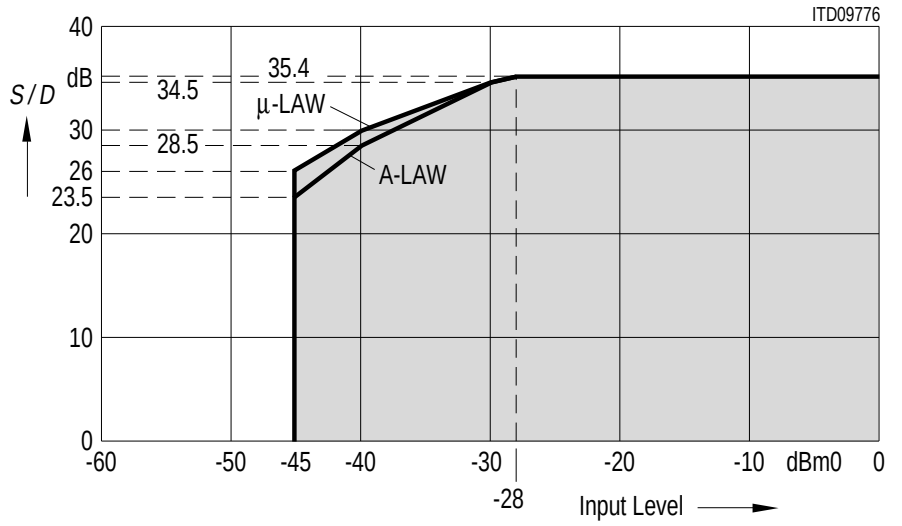


Figure 27
Receive or Transmit: measured with sine wave f = 1014 Hz. (C-message weighted for μ-law, psophometricaly weighted for A-law)

4.9 Single Frequency Distortion

An input signal with its frequency swept between 0.3 to 3 kHz for the receive path, or 0 to 12 kHz for the transmit path, any generated output signal with other frequency than the input frequency will stay 28 dB below the maximum input level of 0 dBM0.

Receive		Transmit	
Frequency	**Max Input Level**	**Frequency**	**Max. Input Level**
300 Hz to 3.4 kHz	0 dBm0	0 to 12 kHz	0 dBm0

4.10 Transhybrid Loss

The quality of Transhybrid-Balancing is very sensitive to deviations in gain and group delay - deviations inherent to the SICOFI-2/4 TE A/D- and D/A-converters as well as to all external components used on a line card (SLIC, OP's etc.)

Measurement of SICOFI-2/4 TE Transhybrid-Loss: A 0 dBm0 sine wave signal and a frequency in the range between 300-3400 Hz is applied to the digital input. The resulting analog output signal at pin V_{OUT} is directly connected to V_{IN}, e.g. with the SICOFI-2/4 TE

testmode “Digital Loop Back via Analog Port”. The programmable filters FRR, AR, FRX, AX and IM are disabled, the balancing filter TH is enabled with coefficients optimized for this configuration (V_{OUT} = V_{IN}).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the table below. (Filter coefficients will be provided)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	typ.		
Transhybrid Loss at 300 Hz	THL_{300}	19	40	dB	T_A = 25 °C; V_{DD} = 5 V;
Transhybrid Loss at 500 Hz	THL_{500}	25	45	dB	T_A = 25 °C; V_{DD} = 5 V;
Transhybrid Loss at 2500 Hz	THL_{2500}	21	40	dB	T_A = 25 °C; V_{DD} = 5V;
Transhybrid Loss at 3000 Hz	THL_{3000}	19	35	dB	T_A = 25 °C; V_{DD} = 5V;
Transhybrid Loss at 3400 Hz	THL_{3400}	19	35	dB	T_A = 25 °C; V_{DD} = 5 V

The listed values for THL correspond to a typical variation of the signal amplitude and delay in the analog blocks.

Δamplitude = typ. $\pm$ 0.15 dB
Δdelay = typ $\pm$ 0.5 µs

5 Proposed Test Circuit

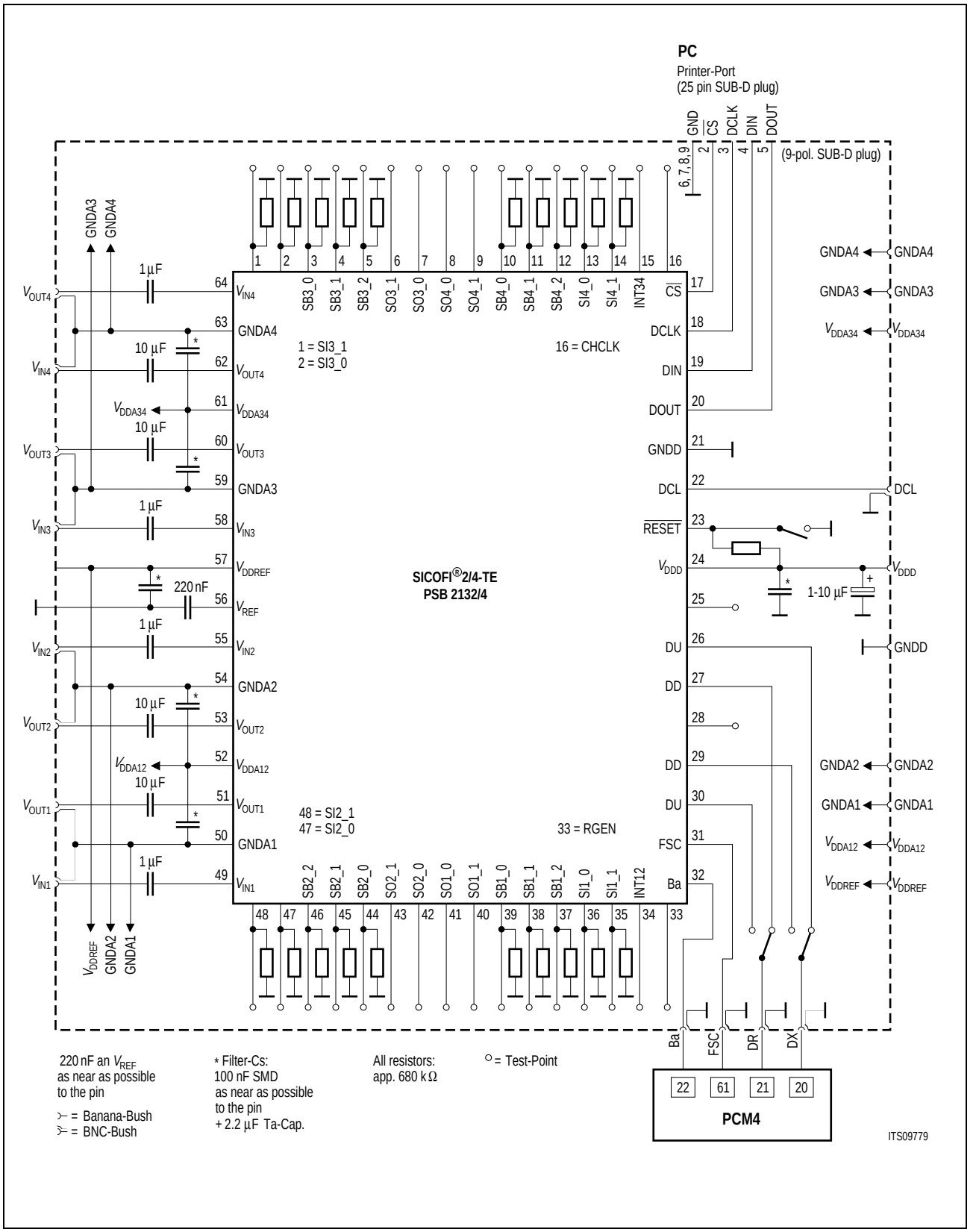


Figure 28

6 Guidelines for Board-Design

6.1 Board Layout Recommendation

Keep in mind that inside the SICOFI-2/4 TE all the different V_{DD}-supplies are connected via the substrate of the chip, and the areas connected to different grounds are separated on chip.

a) Separate all digital supply lines from analog supply lines as much as possible.
b) Use a separate GND-connection for the capacitor which is filtering the reference voltage (220 nF ceramic-capacitor at V_{REF}).
c) Don't use a common ground-plane under the SICOFI-2/4-TE.
d) Use a large ground-plane (distant from the SICOFI-2/4-TE) and use three single ground lines for connecting the SICOFI-2/4-TE: one common analog ground, one digital ground, and a third for the 220 nF capacitor connected to V_{REF}.

6.2 Filter Capacitors

a) To achieve a good filtering for the high frequency band, place SMD ceramic-capacitors with 100 nF from V_{DDA12}, V_{DDA32} and V_{DDREF} to GNDA.
b) One 100 nF SMD ceramic-capacitor is needed to filter the digital supply (V_{DDD} to GNDD).
c) Place all filter capacitors as close as possible to the SICOFI-2/4-TE (most important!!!).
d) Use one central Tantalum-capacitor with about 1 µF to 10 µF to block V_{DD} to GND.

6.3 Example of a SICOFI-2/4-TE-board

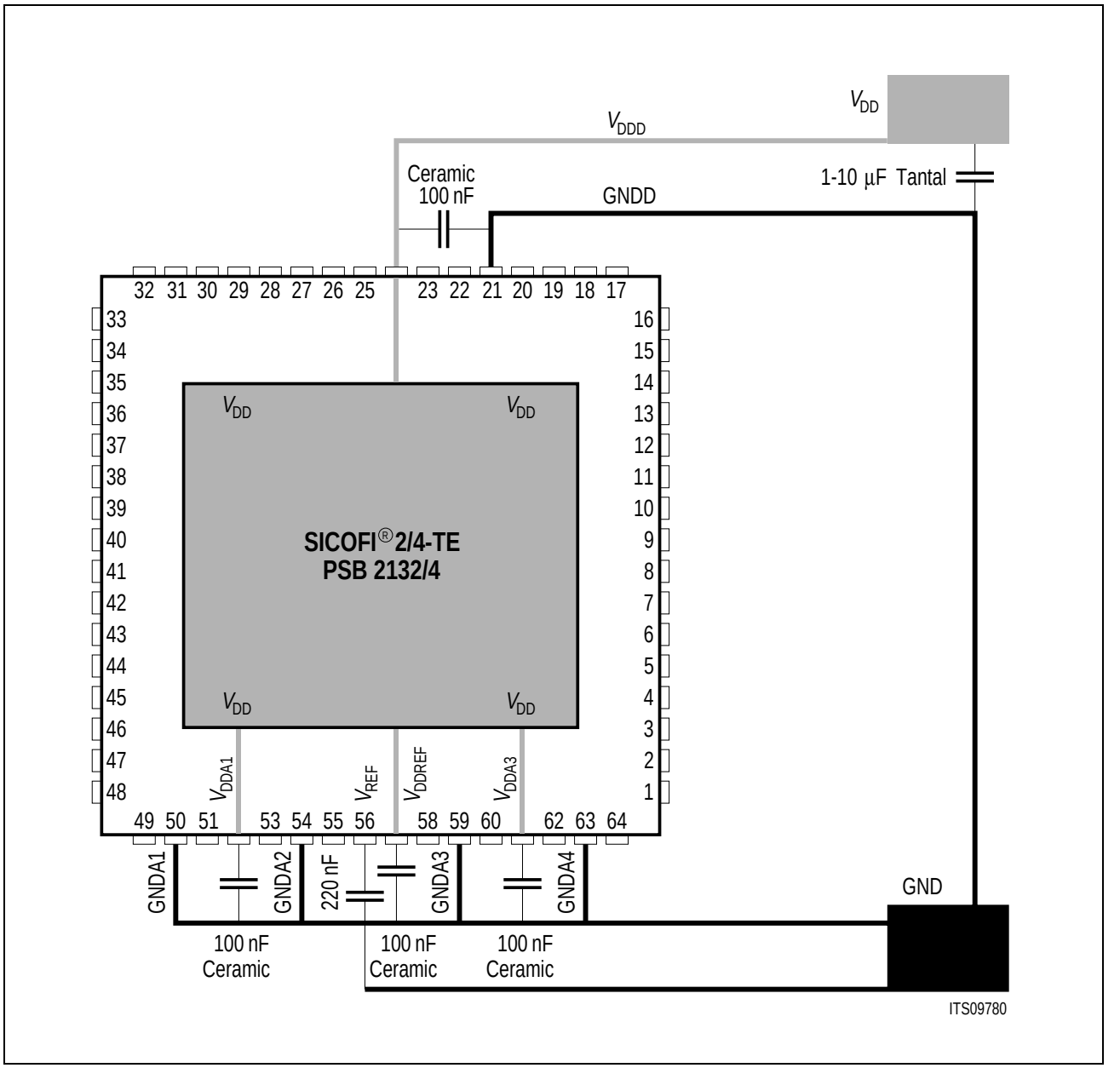


Figure 29

7 Programming the SICOFI2/4-TE Tone Generators

Two independent tone generators are available per channel. Switching on/off the tone generators is done by a SOP-Command for CR1-register. The frequencies are programmed via a COP-Command, followed by the appropriate byte-sequence.

When one or both tone generators are switched on, the voice signal is switched off, if V+T=0 (CR2) for the selected voice channel. To make the generated signal sufficient for DTMF, a programmable bandpass-filter is included. The default frequency for both tone

generators is 1000 Hz. The QSICOS-program contains a program for generating coefficients for variable frequencies.

The following table shows sequences for programming both the tone generators and the bandpass-filters to select common used frequencies:

Table 1

Frequency	Tone Freq.	Command	Byte 1	Byte 2	Byte 3	Byte 4
350 Hz	343,8 Hz	0C/0D [1)]	0C	33	59	23
400 Hz	406,3 Hz	0C/0D [1)]	0B	AB	59	2B
425 Hz	421,9 Hz	0C/0D [1)]	0B	B6	59	33
440 Hz	439,5 Hz	0C/0D [1)]	0B	CC	59	3C
445 Hz	445,3 Hz	0C/0D [1)]	0B	D7	59	3C
880 Hz	879,9 Hz	0C/0D [1)]	14	23	5B	D3
950 Hz	949,2	0C/0D [1)]	1C	F0	5C	C0
1000 Hz	984,4 Hz	0C/0D [1)]	1B	3B	50	87
1400 Hz	1406,3 Hz	0C/0D [1)]	BA	AC	51	AB
1800 Hz	1812,5 Hz	0C/0D [1)]	91	B2	50	AB

[1)] 0C is used for programming Tone Generator 1, in channel 1
0D is used for programming Tone Generator 2, in channel 1

The resulting signal amplitude can be set by transmitting the AR1 and AR2 filters. By switching a ‘digital loop’ the generated sine-wave signal can be fed to the transmit path.

8 Application Note: Level Metering

8.1 Introduction

The purpose of this application note is to describe the handling of the Level Metering Function and the facts that should be taken into account when using it.

The Level Metering Function is a feature which allows a self test of the chip and also a test of the connected circuitry i.e. SLIC, subscriber line and analog telephone. No external components are needed for this function.

8.2 Level Metering Block

Figure 33 shows the location of the Level Metering Function in the signal flow graph of one channel.

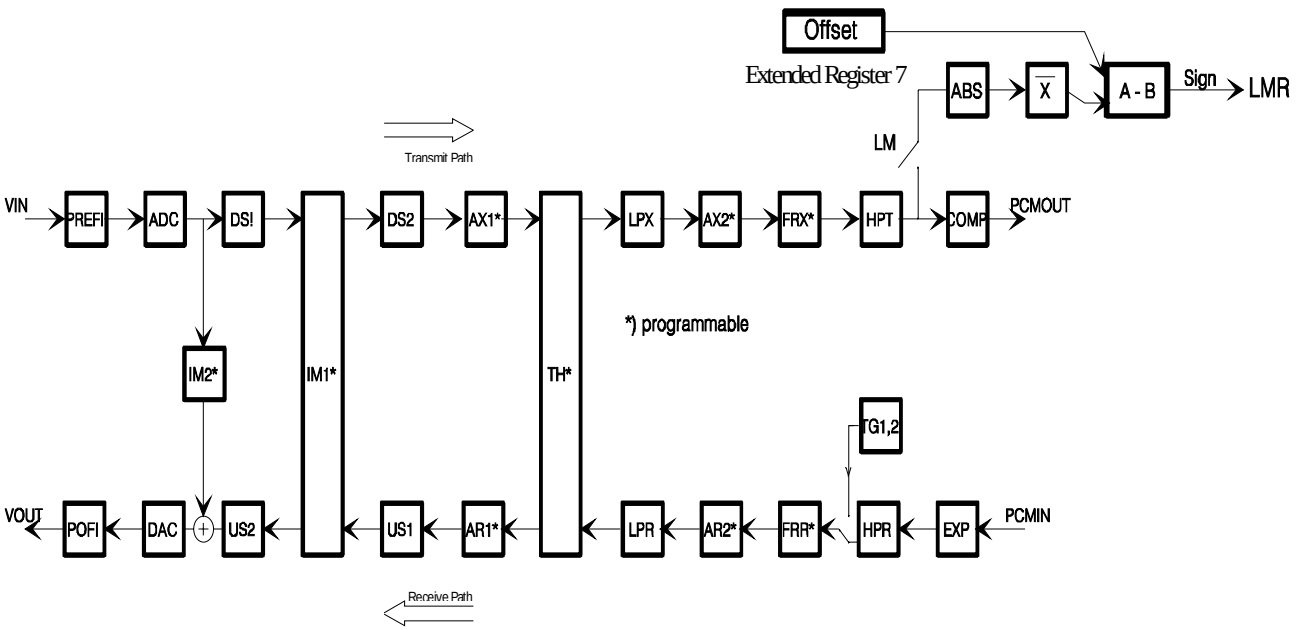


Figure 30
Block diagram of one SICOFI2/4-TE channel

The level metering function is always used together with a bandpass filter. The programming of this bandpass filter has to be done by programming the tone generator coefficients of the tone generator TG2. Due to of the bandpass filter only the power of a certain test signal is measured and disturbences originated from other signals are avoided.
After passing the bandpass filter of the Level Metering Function the test signal in the transmit path is rectified and the power of this signal is compared to the programmable offset value of the Level Metering Function. The reading of the CR2-bit LMR shows if the measured level of the test signal was higher or lower than the programmed offset value.

There is a single 8-bit offset register available for all 4 channels. This offset register can be accessed as XR7 with a XOP command. With the QSICOS utility program 'Calculate Level Metering Function' the programming byte for the register XR7 can be calculated. Another way is to use the table of appendix A.
By using the Level Metering Function in channel 2 (or 4) the channel 1 (or 3) has to be in operating mode.

8.3 Measuring a Level via the Level Metering Function

To find the value of an unknown level as fast as possible, the offset register should be programmed with the byte in the middle of the measuring range. The reading of the configuration register 2 bit LMR shows if the measured level is higher or lower than the programmed level.
If the measured level is higher than the reference, the offset register should be programmed with the byte in the middle between the highest valid byte and the previous used byte. Otherwise the byte in the middle between the lowest valid byte and the previous used byte should be programmed in the offset register.
Figure 2 shows the last three steps of such a procedure.

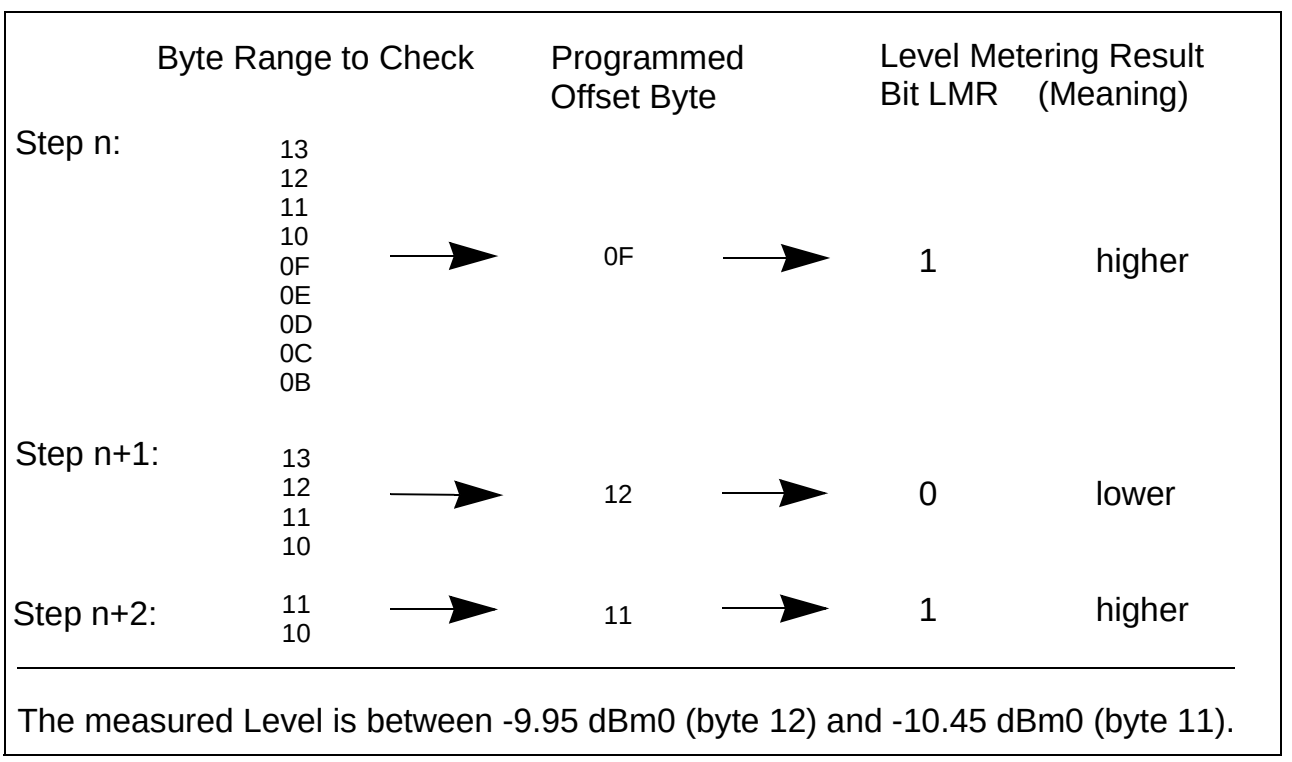


Figure 31
Procedure to find an unknown level with the Level Metering Function

By repeating the interpolation again and again two consecutive bytes will be found where bit LMR is high for the lower and low for the higher byte. The value of the unknown level is between the levels assigned to these two consecutive bytes.
Appendix B shows the programming file LMch1a.SUC with this procedure.

The procedure to find an unknown level is predesigned to be carried out by software. The first valid LMR-bit is available 4 ms after enabling the level metering via setting bit LM. Then the LMR-bit is updated every 4 ms corresponding to the topical test signal and the stored offset byte. During the measurement time of 4ms the test signal has to be stable. That means for the above mentioned procedure to find an unknown level:
1. After programming the offset register and enabling the Level Metering Function, the software has to wait for at least 4 ms before accessing the first valid LMR-bit.
2. After programming the offset register again the software has to wait for at least 4 ms before accessing bit LMR.
3 After a change of the test level the software has to wait for at least 8 ms before accessing bit LMR.

8.4 Relative Measuring Precision

The bytes for the offset register are assigned to voltage values with a distance of about 0,02 Vrms. Since a level is measured by determining the bytes below and above, the distance between two consecutive bytes defines the relative measuring precision.
The maximum relative measuring error is about 0.02 Vrms.
The absolute measuring precision is depending on the gain tracking and described in the SICOFI2/4-TE data sheet.

8.5 Generating Tests Signals

In order to perform a measurement, an appropriate test signal is necessary.
There are 3 different ways to create a test signal: built-in tone generators, test equipment PCM4 by Wandel and Goltermann or an external analog test source.

8.6 Tone Generators

Only tone generator 1 is available for level metering. By setting the LM bit in CR2 tone generator 2 is automatically switched off. But it is necessary to program both bandpass filters with the same coefficients because the coefficients of tone generator 2 determine also the bandpass filter for the Level Metering Function. Only with identically adjusted bandpass filters a precise level metering is possible.
A very simplified block diagram is shown in figure 35.

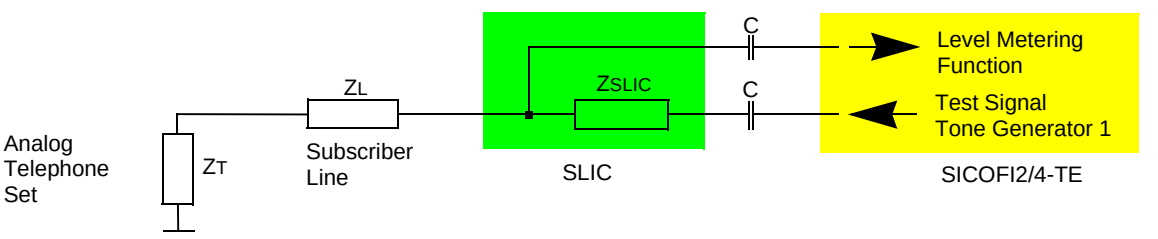


Figure 32
Test signal generated by tone generator 1

The attenuation and amplification filters of the SICOFI2/4-TE can be used to amplify or attenuate the level of the tone generator 1. With disabled filters the tone generator 1 sends a level of -4.5 dBm0.
In order to avoid test signal attenuation by the balancing filter TH, it has to be disabled. It is necesarry to switch off the voice in the respective channel during level metering with V+T bit of CR2.
No external components are required to use the Level Metering Function with the built-in tone generators. This can be very helpful in digital exchange systems. It is a task of the exchange software to switch from time to time the tone generators on and to measure the level via the Level Metering Function. So the actual state of all SICOFI2/4-TE channels and connected circuitry can be supervised very comfortably.

8.7 PCM4

For development of a new application the PCM4 by Wandel and Goltermann can also be very helpful to send and receive test signals. Please make sure that the configuration of the PCM4 corresponds to the SICOFI2/4-TE configuration, for instance that the same companding law is used.
Figure 36 shows a test configuration with a PCM4 device.

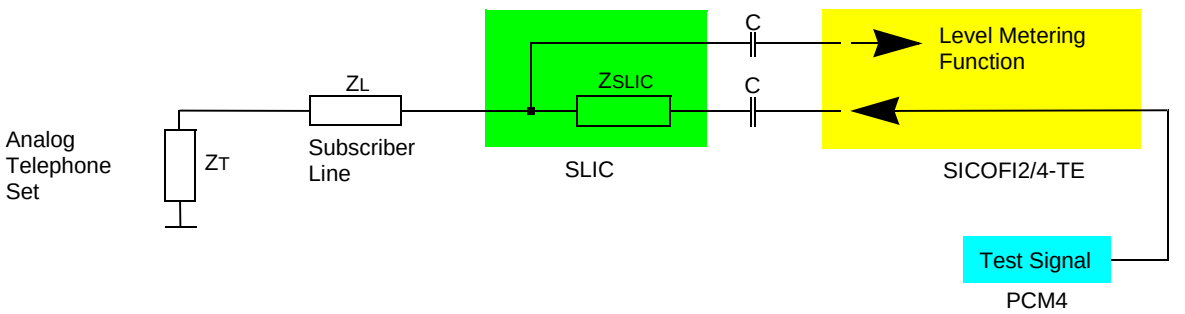


Figure 33
Test signal for level metering provided by PCM4

For a digital exchange system it is possible to use a PCM4 as a test signal generator as well as a test signal receiver. To do this, the PCM4 has to be connected to a PCM highway and the exchange has to switch the test information from the PCM4 to the respective SICOFI2/4-TE and back.
By using a PCM4 the expenditure for level metering measurement, level evaluating and preparation for software processing is higher and already done in the level metering block of the SICOFI2/4-TE. That is why the Level Metering Function is more helpful in digital exchange systems than a PCM4.

8.8 Analog Test Source

For test purposes an analog test signal can be applied to the SICOFI2/4-TE analog input. Figure 37 shows such a configuration.

To calculate the applied analog level, the gain settings of the SICOFI2/4-TE filters together with the 0 dBm0 reference voltage have to be taken into consideration.

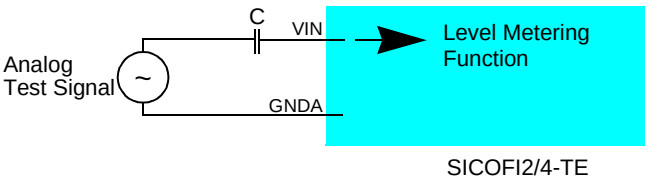


Figure 34
Measurement of an unknown level

8.9 Loops

If the test signal is fed via tone generator 1 or via PCM4 in the receive path of the SICOFI2/4-TE a loop is necessary to feed the test signal back to the transmit path.
Digital loops are implemented in the SICOFI2/4-TE and can be activated by writing register CR4. After switching an internal loop the measured level is a representation of the internal attenuation and amplification via the filter blocks. Such self tests show whether the SICOFI2/4-TE is working or not and how it is adjusted.
In a line card application a SLIC is connected to each channel of the SICOFI2/4-TE. The SLIC together with a connected analog telephone creates a loop from the receive-path to the transmit path. SLIC, subscriber line and telephone have a special impedance according to their specification. If only one of them changes the value, the returned test signal will be changed und will indicate a change in the corresponding system condition. Therefore, changes of the telephone state, the subscriber line length or the SLIC can be supervised.

8.10 Application Examples

8.10.1 Supervision the State of a Subscriber Line

The configuration of an application example is shown in figure 38.

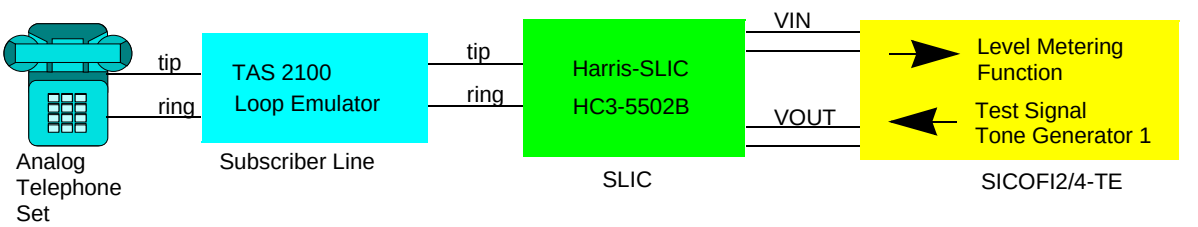


Figure 35
Test configuration

The TAS 2100 emulates subscriber line lengths from 0 to 6 kft in 1 kft increments. 1 kft is equivalent to 0.3 km.
The SICOFI2/4-TE is programmed with the file TEST.SUC for operation with the Harris-SLIC HC 5502 and the specification for Germany. The file TEST.SUC is a component part of the QSICOS software.
After that the SICOFI2/4-TE is programmed with the file LMch1b.SUC of appendix C. The task of this file is to program the bandpass filters at 1516 Hz and to increase the amplification by programming the AR and AX filters. With the second part of the file LMch1b.SUC the Level Metering Function is activated and the offset register is loaded. The read command reads out CR2 with bit LMR. Bit LMR shows if the level detected is higher or lower than the reference stored in the offset register.
By changing the line length with the Loop Emulator the levels of appendix D are measured by using the procedure described in paragraph 2.1. The values of the metered levels are depending on the line lengths.
That means, that it is possible to determine the state of a connected telephone as well as the subscriber line length very comfortably due to the help of the Level Metering Function and the built-in tone generators.

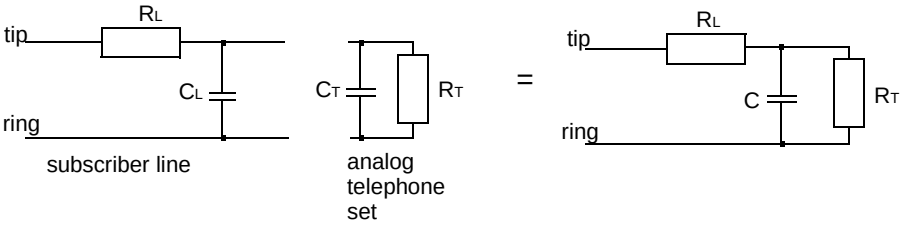
8.10.2 Improvement of Transhybrid Balancing

The Level Metering Function can also be used for an improvement of transhybrid balancing. This can be very useful after calculating the filter coefficients via QSICOS software and getting a too low transhybrid loss because of too long (or too short) subscriber lines. With the knowledge of the subscriber line impedance and the telephone impedance an optimization of the transhybrid loss is possible.
For it a configuration like in figure 38 is used. The transhybrid filter is enabled with bit TH=1 of configuration register 0.
The tone generator 1 is programmed for sending a test frequency in the range between 300 and 3400 Hz, e.g. 300 Hz. The via Level Metering Function measured level (dBm0) minus the send level (dBm0), minus the value RLR (dB) and plus the value RLX (dB) is equivalent to the negative transhybrid loss.

Transhybrid loss/dB = send level/dBm0 + RLR/dB + RLX/dB - measured level/dBm0

In order to get information about the transhybrid loss over the whole frequency band measurements at some other frequencies are necessary. In appendix E is a list of some frequencies and assigned tone generator coefficients.
If the transhybrid loss measurement results are to low, another coefficient set has to be used for the respective channel. Either a transhybrid filter set of another channel can be used or a new coefficient set can be written to the coefficient RAM.
For calculating a transhybrid filter coefficient set via QSICOS producing a high transhybrid loss the value of the subscriber line impedance und the telephone

impedance has to be known. Figure 39 shows a simplified model of a subscriber line with an analog telephone set.



$C=C_L+C_T$

SPEC-File of QSICOS software:

ZL = 1 (circuit 1)
ZLR1 = RL
ZLR2 = RT
ZLC = C

Figure 36
A simplified model of a subscriber line and an analog telephone set

The subscriber line resistance and the subscriber line capacitance are depending on the cable type. Appendix F shows cable parameters of some cable types at 1 kHz. The cable parameters multiplied with the line length form the line resistance (R_L) and the line capacitance (C_L).
The input impedance of the telephone can be measured with an impedance analyzer. With parallel measuring mode the telephone resistance (R_T) and the telephone capacitance (C_T) in the off-hook state can be determined.
The sum of the telephone capacitance and the line capacitance forms the capacitance ZLC and is an input for QSICOS. The other inputs for QSICOS are R_L (ZLR1) and R_T (ZLR2). With these values QSICOS can calculate coefficients for a high transhybrid loss. Often the SICOFI2/4-TE is used with the same type of SLIC on all four channels. Therefore all four coefficient sets can be the same. But for different subscriber line lengths different transhybrid filter coefficients are necessary. For getting a high transhybrid loss it is useful to calculate TH-filter coefficient sets for 4 different subscriber line lengths and to store them in the coefficient RAM. With the help of the Level Metering Function the best coefficient set with the highest transhybrid loss can be selected for each channel.
So an improving of the transhybrid balancing by measuring the transhybrid loss and loading or selecting another coefficient set is possible. No external measuring devices are necessary.

8.11 Appendix

Appendix A: Assignment of measured level and byte for offset register XR7

Level / dBm0	Hex-Code	Level / dBm0	Hex-Code
3.11	51	-3.02	28
3.00	50	-3.24	27
2.89	4F	-3.46	26
2.78	4E	-3.69	25
2.67	4D	-3.93	24
2.56	4C	-4.18	23
2.44	4B	-4.43	22
2.33	4A	-4.69	21
2.21	49	-4.96	20
2.09	48	-5.23	1F
1.97	47	-5.52	1E
1.84	46	-5.81	1D
1.72	45	-6.11	1C
1.59	44	-6.43	1B
1.46	43	-6.76	1A
1.33	42	-7.10	19
1.20	41	-7.45	18
1.07	40	-7.82	17
0.93	3F	-8.21	16
0.79	3E	-8.61	15
0.65	3D	-9.04	14
0.50	3C	-9.48	13
0.36	3B	-9.95	12
0.21	3A	-10.45	11
0.06	39	-10.98	10
-0.09	38	-11.54	0F
-0.25	37	-12.14	0E
-0.41	36	-12.78	0D
-0.57	35	-13.47	0C
-0.74	34	-14.23	0B
-0.91	33	-15.06	0A
-1.08	32	-15.97	09
-1.25	31	-17.00	08
-1.43	30	-18.16	07
-1.62	2F	-19.50	06
-1.80	2E	-21.08	05
-1.99	2D	-23.02	04
-2.19	2C	-25.52	03
-2.39	2B	-29.04	02
-2.59	2A	-35.06	01

Level / dBm0	Hex-Code	Level / dBm0	Hex-Code
-2.80	29		

Appendix B: File LMch1a.SUC

```
;SICOFI2/4-TE LEVEL METERING in channel 1, Version 1.0 by R.Kitze, January 1997
;Configuration: SICOFI4-µC Board V1.1 STUT 2466, EVC50X Board, Harris SLIC-Board STUS
;5502 V2.0.
;Please run the file TEST.SUC (QSICOS package) first to configure the SICOFI2/4-TE.
;-----------------------------------------------------------------------------------------------------------------
;Programming of the tone generators 1 and 2, bandpass is set to 1516 Hz
W 0 0C A5 53 61 56
W 0 0D A5 53 61 56
;-----------------------------------------------------------------------------------------------------------------
W 0 13 00 04 71 7C ; power up channel 1, TH is disabled and level metering is enabled
;The test level is -10.2 dBm0.
;-----------------------------------------------------------------------------------------------------------------
;STEP 1:
W 0 1F 28 E0 80 0F FF FF FF FF ; LM offset byte = 28 (middle of the measuring range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=04 indicates that the measured level is lower than the reference
;-----------------------------------------------------------------------------------------------------------------
;STEP 2:
W 0 1F 14 E0 80 0F FF FF FF FF ; LM offset byte = 14 (middle of the target range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=04 indicates that the measured level is lower than the reference
;-----------------------------------------------------------------------------------------------------------------
;STEP 3:
W 0 1F 0A E0 80 0F FF FF FF FF ; LM offset byte = 0A (middle of the target range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=06 indicates that the measured level is higher than the reference
;-----------------------------------------------------------------------------------------------------------------
;STEP n:
W 0 1F 0F E0 80 0F FF FF FF FF ; LM offset byte = 0F (middle of the target range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=06 indicates that the measured level is higher than the reference
;-----------------------------------------------------------------------------------------------------------------
;STEP n+1:
W 0 1F 12 E0 80 0F FF FF FF FF ; LM offset byte = 12 (middle of the target range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=04 indicates that the measured level is lower than the reference
;-----------------------------------------------------------------------------------------------------------------
;STEP n+2:
W 0 1F 11 E0 80 0F FF FF FF FF ; LM offset byte = 11
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=06 indicates that the measured level is higher than the reference
```

```
;-----------------------------------------------------------------------------------------------------------------------
;Result: The measured level is between the levels -9.95 dBm0 (byte 12) and -10.45 dBm0 (byte 11).
```

Appendix C: File LMch1b.SUC

```
;Supervision the state of a subscriber line via LEVEL METERING in channel 1
;Version 1.0 by R.Kitze, January 1997
;Configuration: SICOFI4-µC Board V1.1 STUT 2466, EVC50X Board, Harris SLIC-Board STUS
;5502 V2.0.
;Please run the file TEST.SUC (QSICOS package) first to configure the SICOFI4-µC.
;-----------------------------------------------------------------------------------------------------------------------
;programming of the tone generators 1 and 2, bandpass is set to 1516 Hz
W 0 0C A5 53 61 56
W 0 0D A5 53 61 56
;programming the amplification/attenuation filters to 2.3 dBm0 at PCM output (test level)
W 0 08 4B 53 2A 56
W 0 09 DD B7 02 3A
;-----------------------------------------------------------------------------------------------------------------------
W 0 13 00 04 71 7C ; power up channel 1, TH is disabled and level metering is enabled
;-----------------------------------------------------------------------------------------------------------------------
;STEP 1: The Loop Emulator is set to 0 kft. The telephone is in the off-hook state.
;-----------------------------------------------------------------------------------------------------------------------
;STEP 1.1:
W 0 1F 28 E0 80 0F FF FF FF FF ; LM offset byte = 28 (middle of the measuring range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=06 indicates that the measured level is higher than the reference
;-----------------------------------------------------------------------------------------------------------------------
;STEP 1.2:
W 0 1F 3C E0 80 0F FF FF FF FF ; LM offset byte = 3C (middle of the target range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=06 indicates that the measured level is higher than the reference
;-----------------------------------------------------------------------------------------------------------------------
;STEP 1.3:
W 0 1F 46 E0 80 0F FF FF FF FF ; LM offset byte = 46 (middle of the target range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=06 indicates that the measured level is higher than the reference
;-----------------------------------------------------------------------------------------------------------------------
;STEP 1.4:
W 0 1F 4B E0 80 0F FF FF FF FF ; LM offset byte = 4B (middle of the target range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=06 indicates that the measured level is higher than the reference
;-----------------------------------------------------------------------------------------------------------------------
;STEP 1.5:
W 0 1F 4E E0 80 0F FF FF FF FF ; LM offset byte = 4E (middle of the target range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=06 indicates that the measured level is higher than the reference
```

```
;-----------------------------------------------------------------------------------------------------------------------
;STEP 1.6:
W 0 1F 4F E0 80 0F FF FF FF FF ; LM offset byte = 4F
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=04 indicates that the measured level is lower than the reference
;Result: The measured level is between the levels 2.89 dBm0 (byte 4F) and 2.78 dBm0 (byte 4E).
;-----------------------------------------------------------------------------------------------------------------------
;STEP 2: The Loop Emulator is set to 1 kft
;-----------------------------------------------------------------------------------------------------------------------
;STEP 2.1:
W 0 1F 28 E0 80 0F FF FF FF FF ; LM offset byte = 28 (middle of the measuring range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=06 indicates that the measured level is higher than the reference
;-----------------------------------------------------------------------------------------------------------------------
;STEP 2.2:
W 0 1F 3C E0 80 0F FF FF FF FF ; LM offset byte = 3C (middle of the target range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=06 indicates that the measured level is higher than the reference
;-----------------------------------------------------------------------------------------------------------------------
;STEP 2.3:
W 0 1F 46 E0 80 0F FF FF FF FF ; LM offset byte = 46 (middle of the target range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=06 indicates that the measured level is higher than the reference
;-----------------------------------------------------------------------------------------------------------------------
;STEP 2.4:
W 0 1F 4B E0 80 0F FF FF FF FF ; LM offset byte = 4B (middle of the target range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=04 indicates that the measured level is lower than the reference
;-----------------------------------------------------------------------------------------------------------------------
;STEP 2.5:
W 0 1F 49 E0 80 0F FF FF FF FF ; LM offset byte = 49 (middle of the target range)
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=06 indicates that the measured level is higher than the reference
;-----------------------------------------------------------------------------------------------------------------------
;STEP 2.6:
W 0 1F 4A E0 80 0F FF FF FF FF ; LM offset byte = 4A
R 0 32 (5) ; Read CR2, CR1, CR0
;CR2=04 indicates that the measured level is lower than the reference
;-----------------------------------------------------------------------------------------------------------------------
;Result: The measured level is between the levels 2.33 dBm0 (byte 4A) and 2.21 dBm0 (byte 49).
;-----------------------------------------------------------------------------------------------------------------------
;STEP 3: The Loop Emulator is set to 2 kft
;-----------------------------------------------------------------------------------------------------------------------
;STEP 3.1:
W 0 1F 28 E0 80 0F FF FF FF FF ; LM offset byte = 28 (middle of the measuring range)
.
```

.
.

Appendix D: Measured levels for different line lengths

Subscriber Line: Cable configuration 0.4 mm = 26 AWG

Subscriber Line in kft	Measured Level in dBm0, off-hook	Measured Level in dBm0, on-hook
0	2.89/2.78	- 7.45/ - 7.82
1	2.33/2.21	- 6.76/ - 7.10
2	1.59/1.46	- 4.96/ - 5.23
3	1.20/1.07	- 3.02/ - 3.24
4	0.79/0.65	- 1.62/ - 1.80
5	0.65/0.50	- 0.57/ - 0.74
6	0.50/0.36	0.21/0.06

The measured level is between the lower/higher level.

Appendix E: Tone generator coefficients (bandpass Q-factor = 2)

Frequency / Hz	Bytes
300	0C D3 19 30
600	0A B4 19 C0
900	14 A4 1B C0
1200	2A 27 12 C0
1500	AC E3 11 09
1900	8A AC 11 20
2200	82 40 10 40
2500	80 AD 10 98
2800	80 3C 10 20
3100	80 15 10 04
3400	80 0C 10 10

Appendix F: Cable parameters at 1 kHz

Cable type	Distributed capacitance C'	Resistance per unit length R'
0.32 mm PVC	120 nF/km	420 Ω/km
0.40 mm PVC	120 nF/km	270 Ω/km
0.40 mm PE	45 nF/km	270 Ω/km
0.50 mm PE	25 nF/km	172 Ω/km
0.60 mm PE	56 nF/km	120 Ω/km
0.63 mm PVC	120 nF/km	110 Ω/km
0.80 mm PE	38 nF/km	68 Ω/km

9 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
V_{DD} referred to GNDD		– 0.3	7.0	V	
GNDA to GNDD		– 0.6	0.6	V	
Analog input and output voltage Referred to V_{DD} = 5 V; Referred to GNDA = 0 V		 – 5.3 – 0.3	 0.3 5.3	 V V	
All digital input voltages Referred to GNDD = 0 V; (V_{DD} = 5V) Referred to V_{DD} = 5 V; (GNDD = 0 V)		 – 0.3 – 5.3	 5.3 0.3	 V V	
DC input and output current at any input or output pin (free from latch-up)			10	mA	
Storage temperature	T_{STG}	– 60	125	°C	
Ambient temperature under bias	T_A	– 10	80	°C	
Power dissipation (package)	P_D		1	W	

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{DD} supply current standby	I_{DIN}		0.5	1.0	mA	FSC,DCL,BCL active no loads
V_{DD} supply current Operating (1 channel) Operating (2 channels) PSB 2134 only: Operating (3 channels) Operating (4 channels)	I_{DIN}		 14 18 22 26	 30 40	 mA mA mA mA	FSC,DCL,BCL active no loads, PCM idle code.
Power supply rejection Of either supply/direction Receive V_{DD} target value	$PSRR$	 30 14			 dB dB	Ripple: 0 to 150 kHz, 70 mVrms Measured: 300 Hz to 3.4 kHz Measured: at f: = 3.4 to 150 kHz

Note: In the operating range the functions given in the circuit description are fulfilled.

Digital Interface

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Low-input voltage	V_{IL}	– 0.3	0.8	V	
High-input voltage	V_{IH}	2.0		V	
Low-output voltage	V_{OL}		0.45	V	I_0 = – 5mA
High-output voltage	V_{OH}	4.4		V	I_0 = 5 mA
Input leakage current	V_{IL}		± 1	µA	$-0.3 \le V_{IN} \le V_{DD}$

Analog Interface

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Analog input resistance	R_i	160	270	380	kΩ	
Analog output resistance	R_O			0.25	Ω	
Analog output load	R_L C_L	300		 50	Ω pF	
Input leakage current	I_{IL}		± 0.1	± 1.0	µA	$0 \le V_{IN} \le V_{DD}$
Input offset voltage	V_{IO}			± 50	mV	
Output offset voltage	V_{OO}			± 50	mV	
Input voltage range (AC)	V_{IN}			± 2.223	V	

9.1 Coupling Capacitors at the Analog Interface

In Transmit direction, a 39 nF capacitor has to be connected to V_{IN}-pins. To fulfil the frequency response requirement in Receive direction, the value of the coupling capacitor (C_{ext1}) needed, depends on the input resistance of the SLIC-circuitry (equals the Analog-Output-Load: R_{Load}).

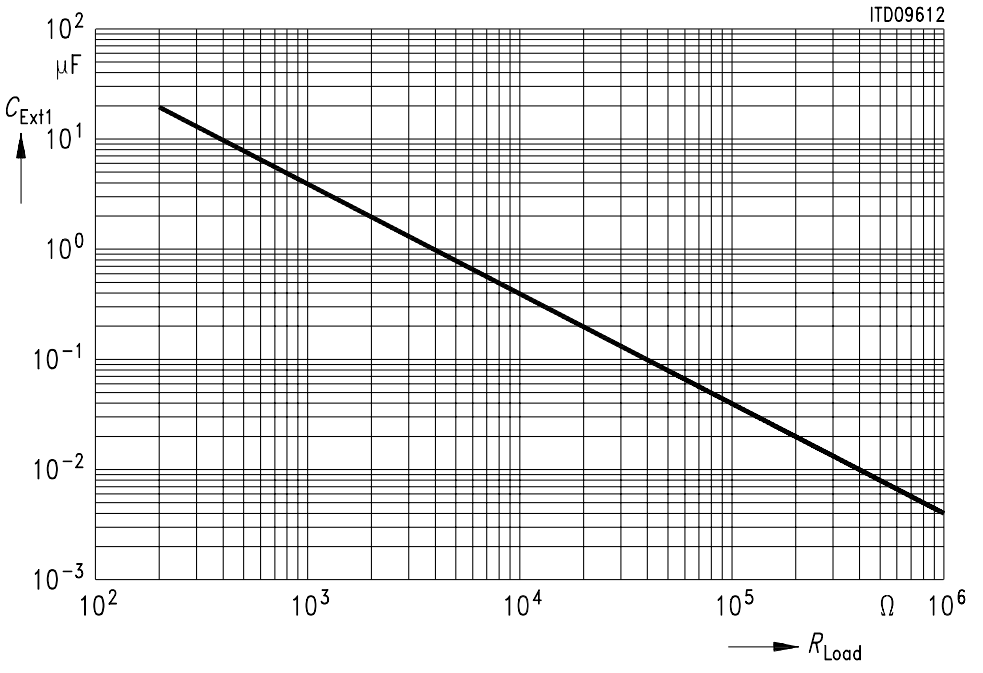


Figure 37

9.2 Reset Timing

To reset the SICOFI-2/4 TE to basic setting mode, negative pulses applied to pin $\overline{\text{RESET}}$ have to be lower than 1.2 V (TTL-Schmitt-Trigger Input) and have to be longer than 3 µs. Spikes shorter than 1 µs will be ignored.

9.3 PCM-Interface Timing

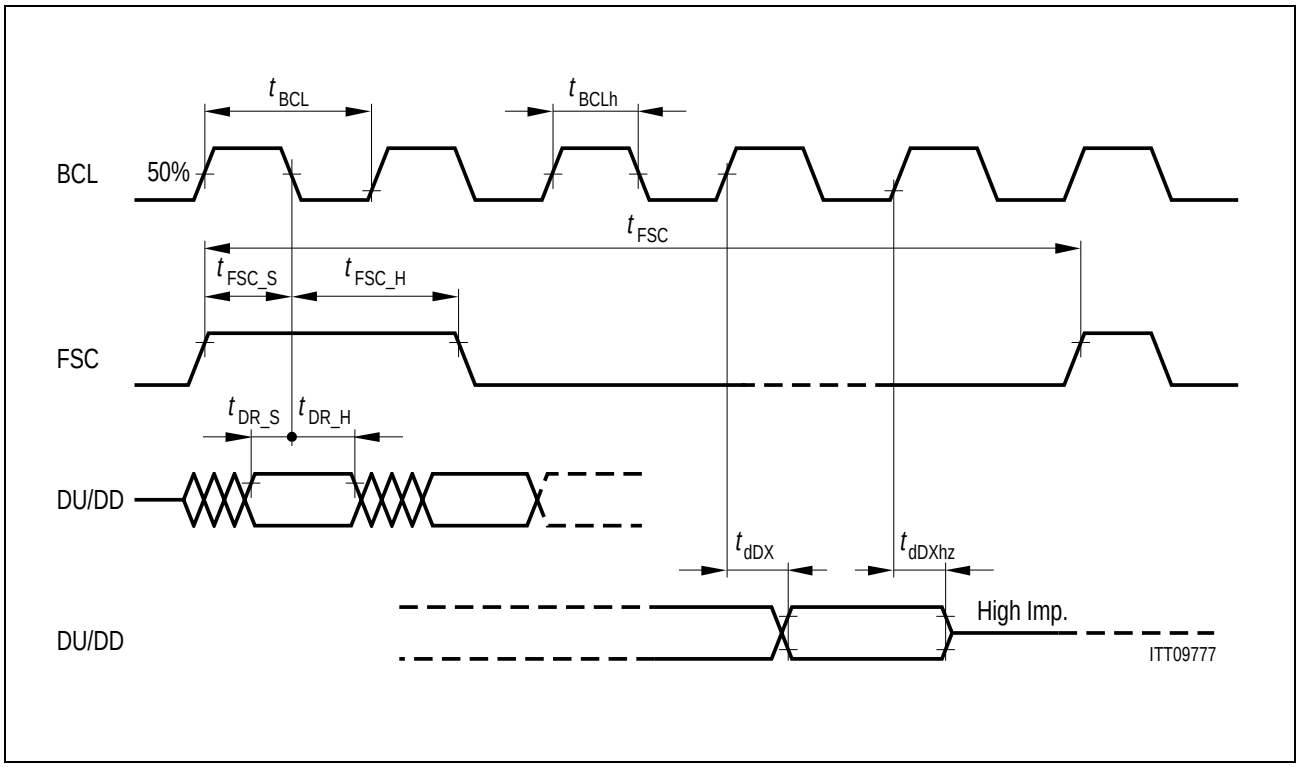


Figure 38
Single Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period of BCL	t_{BCL}		1/768000		µs
BCL high time	t_{BCLh}		$t_{BCL/2}$		µs
Period FSC	t_{FSC}		125		µs
FSC setup time	t_{FSC_s}	10	50		ns
FSC hold time	t_{FSC_h}	(t_{BCL} - t_{BCLh}) + 10	(t_{BCL} - t_{BCLh}) + 50		ns
DU/DD setup time	t_{DR_s}	10	50		ns
DU/DD hold time	t_{DR_h}	10	50		ns
DU/DD delay time [1)]	t_{dDX}	25	50 (@ 200 pF)		ns
DU/DD delay time to high Z	t_{dDXhz}	25	50		ns

[1)] All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C-load)

9.4 µ-Controller Interface Timing

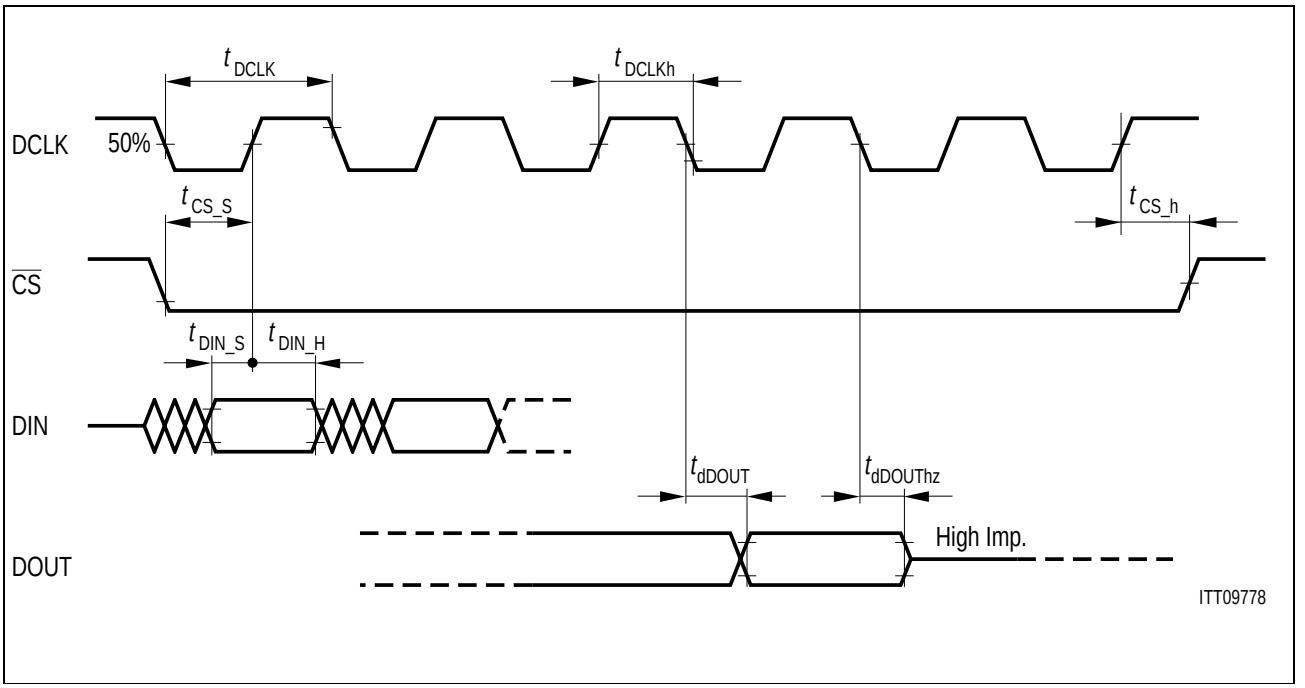


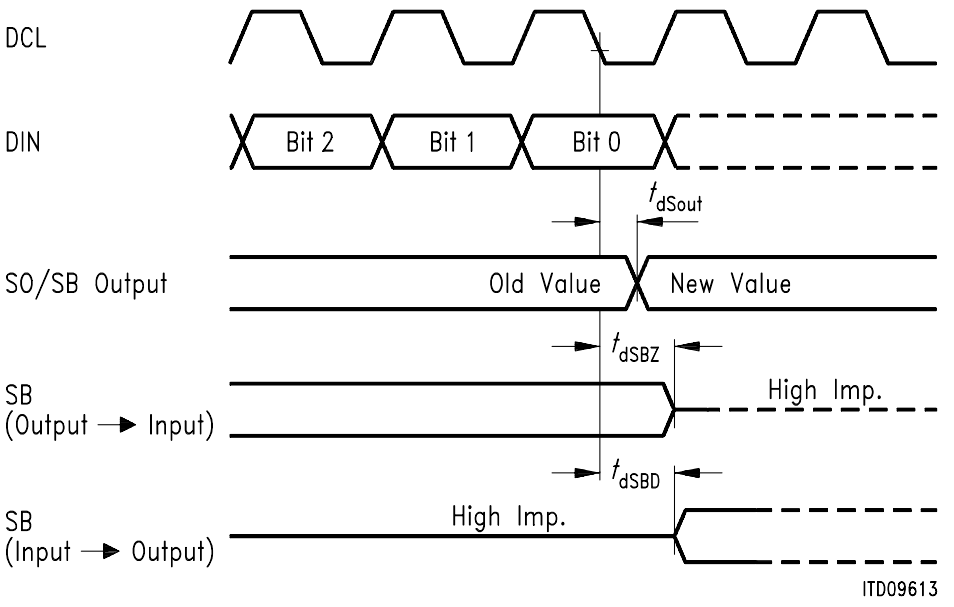
Figure 39

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period of DCLK	t_{DCLK}	1/8192			ms
DCLK high time	t_{DCLKh}		$t_{DCLK/2}$		µs
CS setup time	t_{CS_s}	10	50		ns
CS hold time	t_{CS_h}	30	50		ns
DIN setup time	t_{DIN_s}	10	50		ns
DIN hold time	t_{DIN_h}	10	50		ns
DOUT delay time [1)]	t_{dDOUT}	30	100		ns
DOUT delay time to high Z	$t_{dDOUThz}$	30	100		ns

1) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C-load)

9.5 Signaling Interface

9.5.1 From the µC-interface to the SO/SB-pins (data downstream)



Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
SO/SB delay time [1]	t_{dSout}	30	100		ns
SB to 'Z' - time	t_{dSBZ}	40	100		ns
SB to 'drive'-time	t_{dSBD}	40	100		ns

[1] All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C-load)

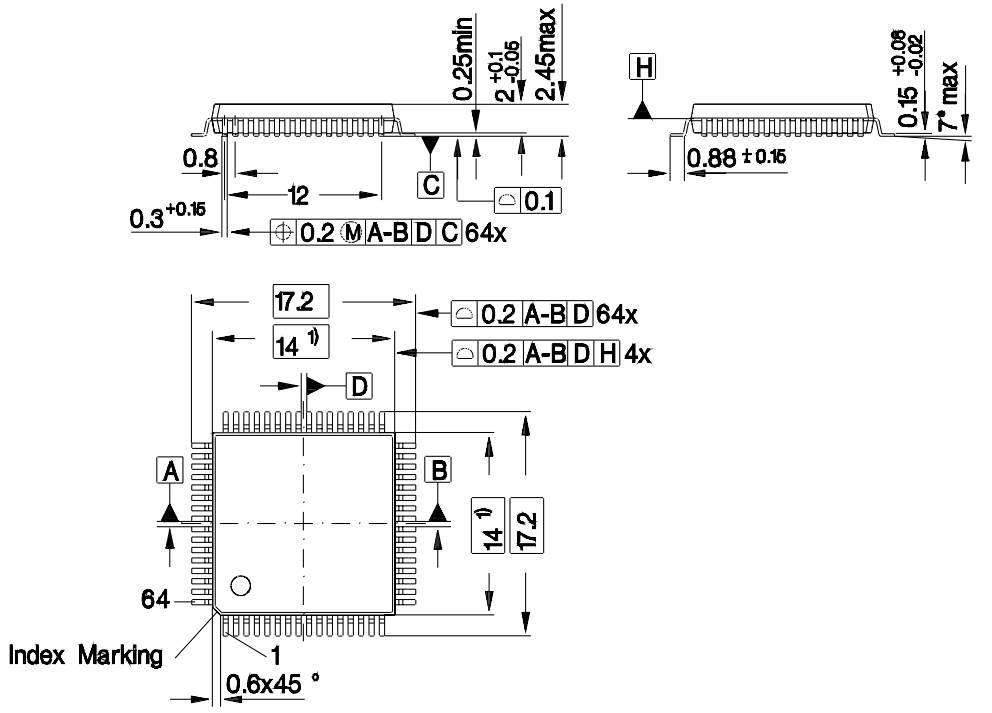
9.5.2 From the SI/SB-pins to the µC-interface (data upstream)

There is no way specifying the time when data applied to SI-pins (and SB-pins if programmed as signaling input pins) is sampled by the SICOFI2/4-TE.

The time only depends on internal signals (16 MHz masterclock, and status of various counters), and there is no link to a low frequency external signal.

10 Package Outlines

P-MQFP-64
(Plastic Metric Quad Flat Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm