

# NTB082N65S3F

## Power MOSFET, N-Channel, SUPERFET<sup>®</sup> III, FRFET<sup>®</sup>, 650 V, 40 A, 82 mΩ

### Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

SUPERFET III FRFET MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

### Features

- 700 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 70\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 81\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 722\text{ pF}$ )
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

### Applications

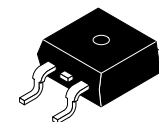
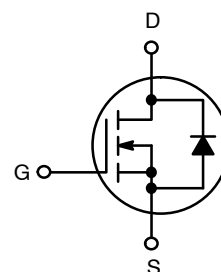
- Telecom / Server Power Supplies
- Industrial Power Supplies
- EV Charger
- UPS / Solar



ON Semiconductor<sup>®</sup>

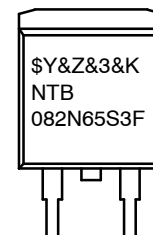
[www.onsemi.com](http://www.onsemi.com)

$V_{DSS}$	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	82 mΩ @ 10 V	40 A



D<sup>2</sup>PAK-3  
CASE 418AJ

### MARKING DIAGRAM



\$Y = ON Semiconductor Logo  
&Z = Assembly Plant Code  
&3 = Data Code (Year & Week)  
&K = Lot  
NTB082N65S3F = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# NTB082N65S3F

## ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C, Unless otherwise specified)

Symbol	Parameter	Value	Unit
V <sub>DSS</sub>	Drain to Source Voltage	650	V
V <sub>GSS</sub>	Gate to Source Voltage	DC	±30
		AC (f > 1 Hz)	±30
I <sub>D</sub>	Drain Current	Continuous (T <sub>C</sub> = 25°C)	40
		Continuous (T <sub>C</sub> = 100°C)	25.5
I <sub>DM</sub>	Drain Current	Pulsed (Note 1)	100
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	510	mJ
I <sub>AS</sub>	Avalanche Current (Note 2)	4.8	A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	3.13	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
P <sub>D</sub>	Power Dissipation	(T <sub>C</sub> = 25°C)	313
		Derate Above 25°C	2.5
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I<sub>AS</sub> = 4.8 A, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 20 A, di/dt ≤ 100 A/μs, V<sub>DD</sub> ≤ 400 V, starting T<sub>J</sub> = 25°C.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction to Case, Max.	0.4	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient (1 in <sup>2</sup> Pad of 2-oz Copper), Max.	62.5	

## PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NTB082N65S3F	NTB082N65S3F	D <sup>2</sup> PAK	Tape and Reel†	330 mm	24 mm	800 Units

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# NTB082N65S3F

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA, T <sub>J</sub> = 25°C	650	–	–	V
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA, T <sub>J</sub> = 150°C	700	–	–	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 10 mA, Referenced to 25°C	–	0.7	–	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V	–	–	10	μA
		V <sub>DS</sub> = 520 V, T <sub>C</sub> = 125°C	–	124	–	
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V	–	–	±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 4 mA	3.0	–	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	–	70	82	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 20 A	–	24	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	3410	–	pF
C <sub>oss</sub>	Output Capacitance		–	70	–	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	–	722	–	pF
C <sub>oss(er.)</sub>	Energy Related Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	–	126	–	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 20 A, V <sub>GS</sub> = 10 V (Note 4)	–	81	–	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		–	24	–	nC
Q <sub>gd</sub>	Gate to Drain “Miller” Charge		–	32	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	1.9	–	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 20 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 3 Ω (Note 4)	–	27	–	ns
t <sub>r</sub>	Turn-On Rise Time		–	27	–	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	79	–	ns
t <sub>f</sub>	Turn-Off Fall Time		–	5	–	ns

### SOURCE-DRAIN DIODE CHARACTERISTICS

I <sub>S</sub>	Maximum Continuous Source to Drain Diode Forward Current	–	–	40	A	
I <sub>SM</sub>	Maximum Pulsed Source to Drain Diode Forward Current	–	–	100	A	
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 20 A	–	–	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 20 A, dI <sub>F</sub> /dt = 100 A/μs	–	108	–	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	410	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

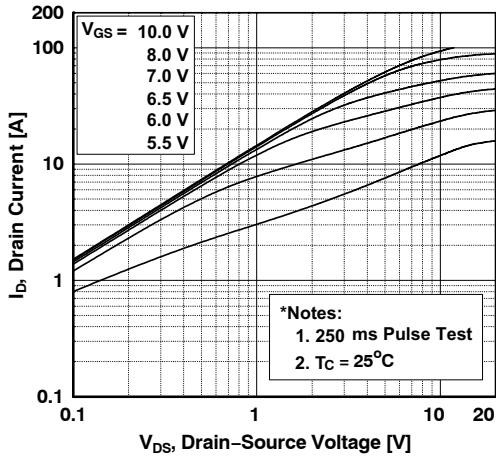


Figure 1. On-Region Characteristics

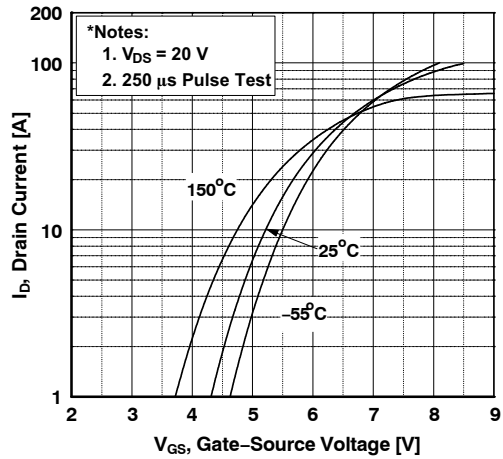


Figure 2. Transfer Characteristics

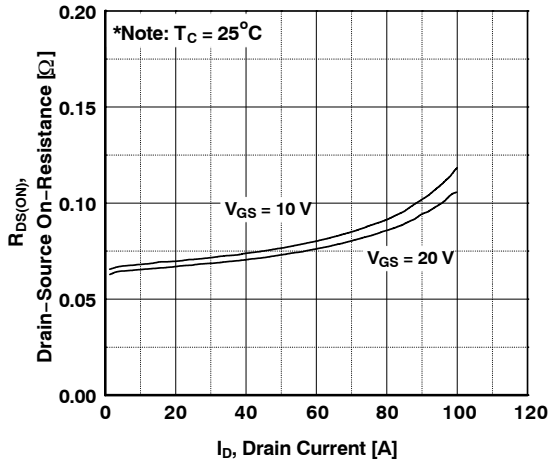


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

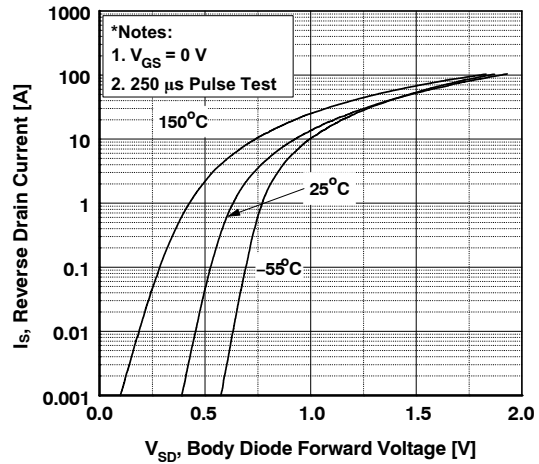


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

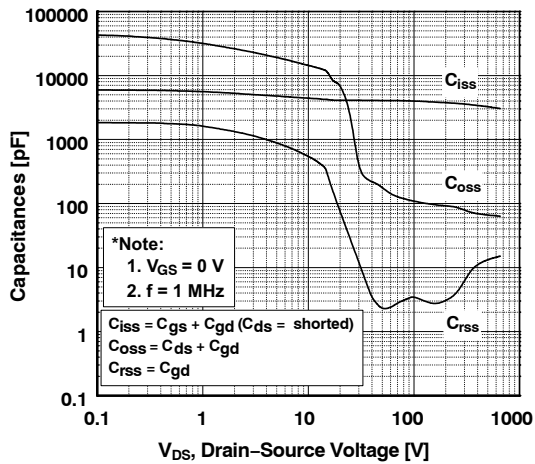


Figure 5. Capacitance Characteristics

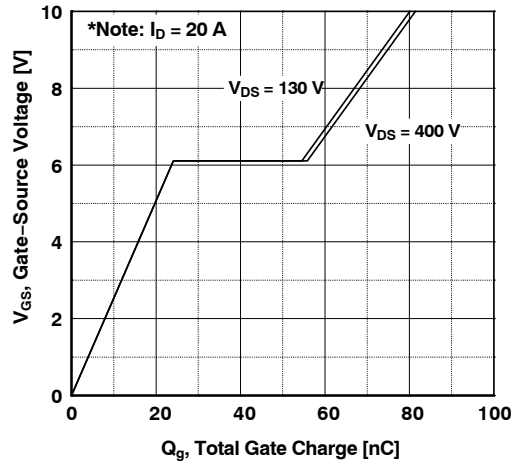


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

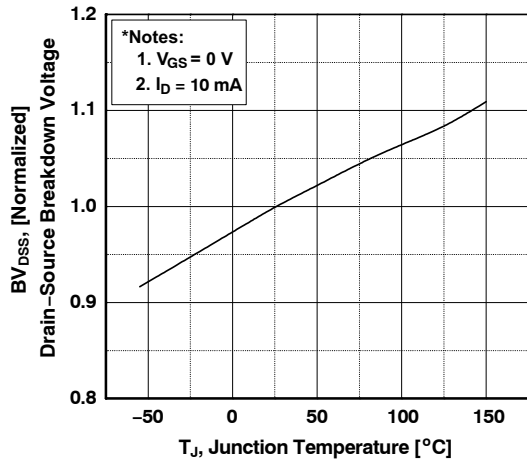


Figure 7. Breakdown Voltage Variation vs. Temperature

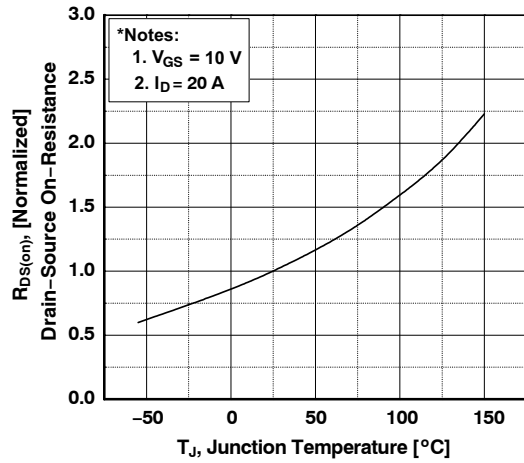


Figure 8. On-Resistance Variant vs. Temperature

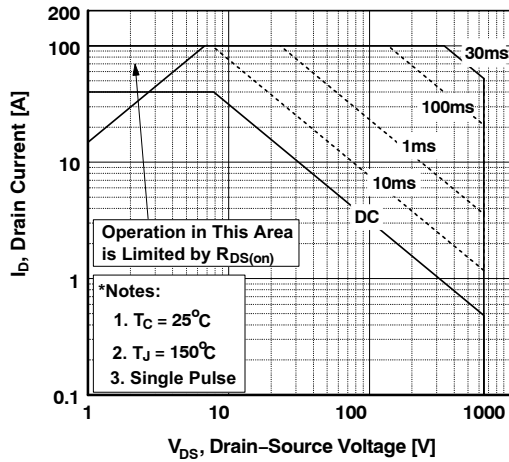


Figure 9. Maximum Safe Operation Area

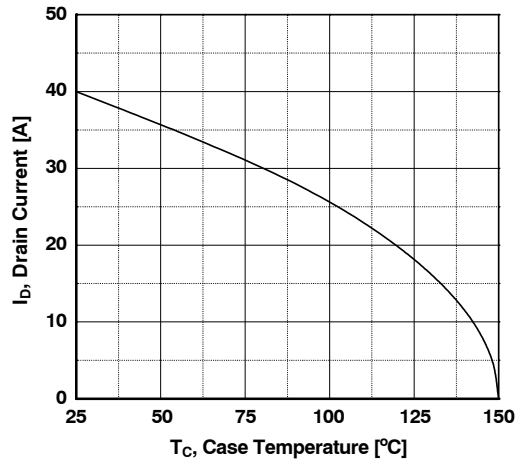


Figure 10. Maximum Drain Current vs. Case Temperature

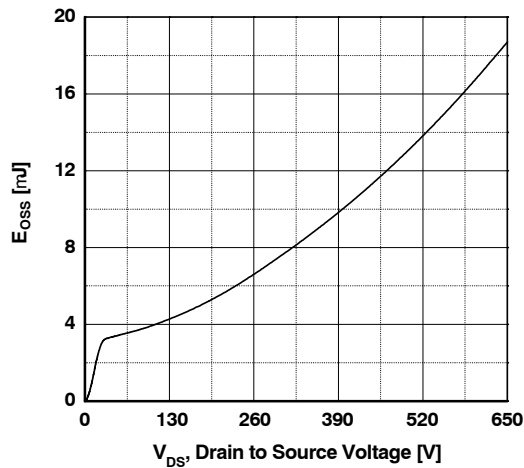


Figure 11.  $E_{OSS}$  vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

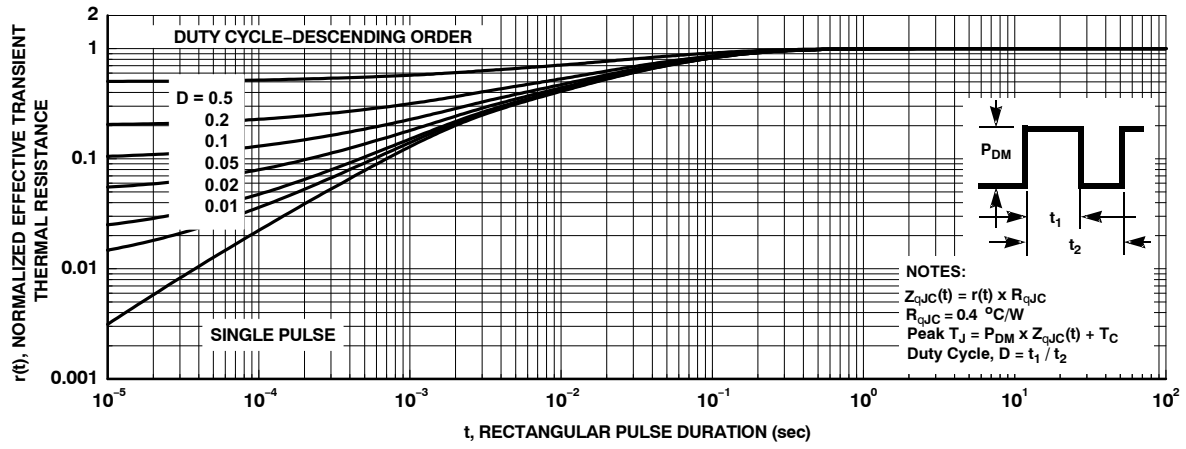


Figure 12. Transient Thermal Response Curve

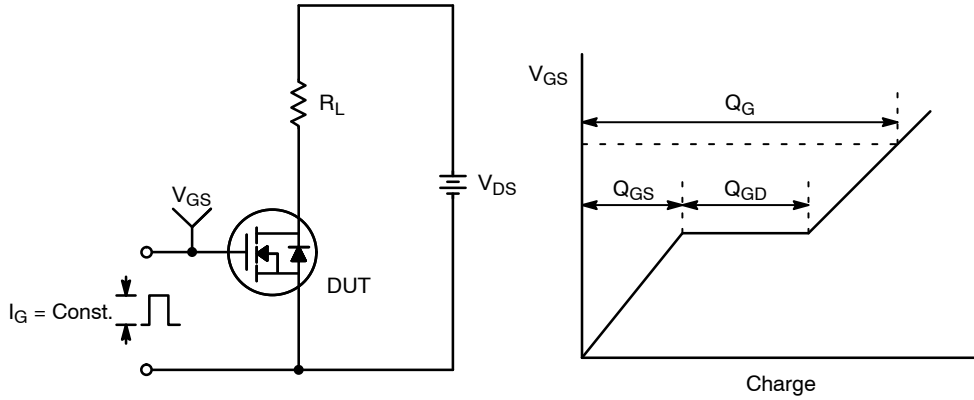


Figure 13. Gate Charge Test Circuit & Waveform

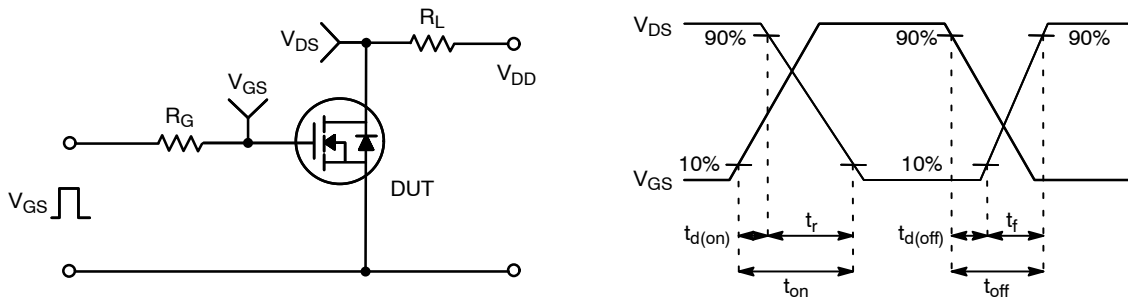


Figure 14. Resistive Switching Test Circuit & Waveforms

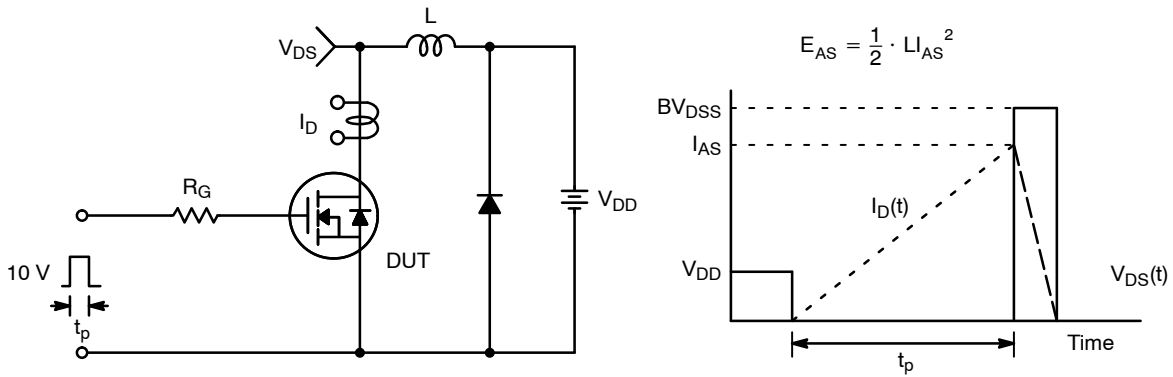


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

NTB082N65S3F

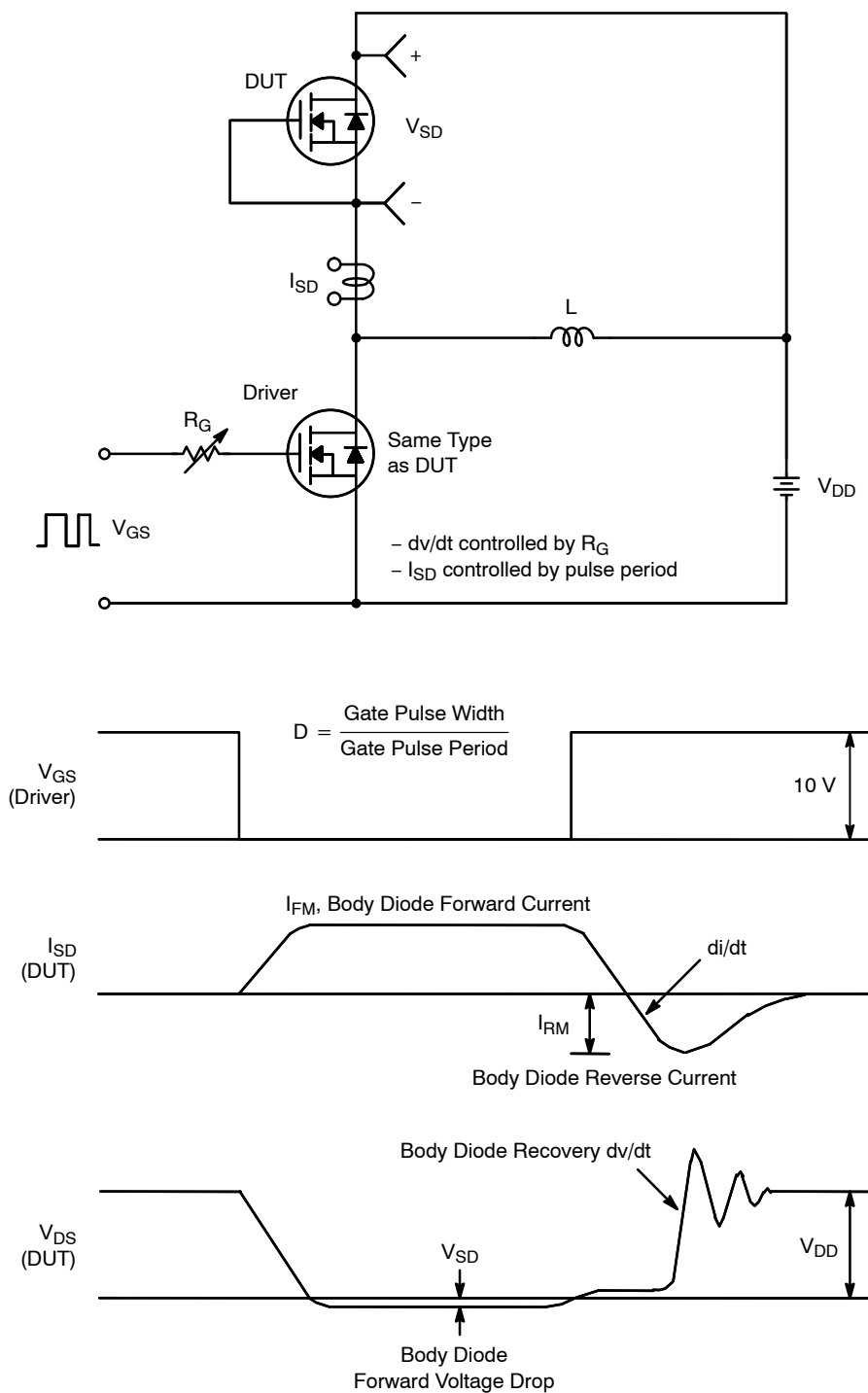


Figure 16. Peak Diode Recovery dt/dt Test Circuit & Waveforms

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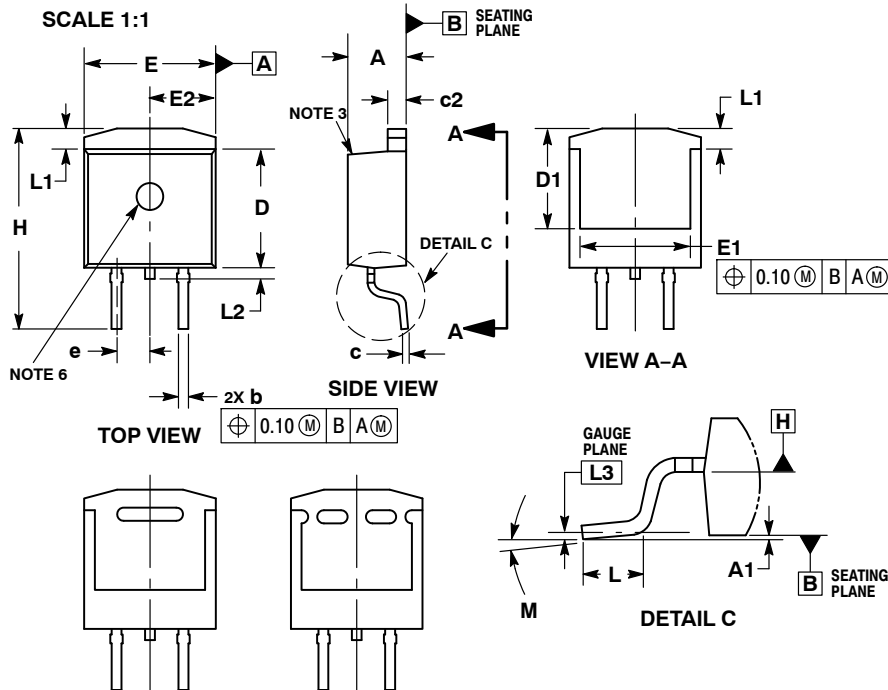
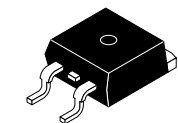
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



## D<sup>2</sup>PAK-3 (TO-263, 3-LEAD) CASE 418AJ ISSUE B

DATE 08 OCT 2013

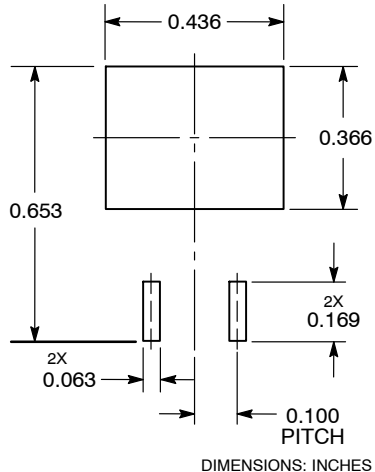


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: INCHES.
  3. CHAMFER OPTIONAL
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
  5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1 AND E1.
  6. OPTIONAL MOLD FEATURE

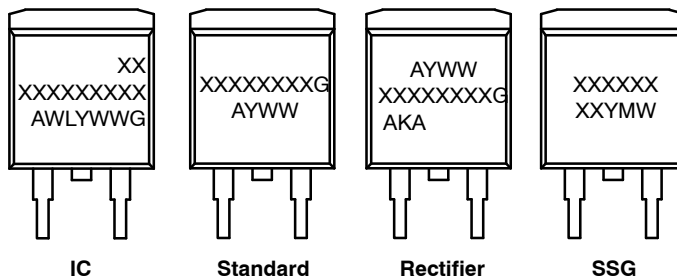
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	----	6.60	----
E	0.380	0.420	9.65	10.67
E1	0.245	----	6.22	----
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	----	0.066	----	1.68
L2	----	0.070	----	1.78
L3	0.010 BSC		0.25 BSC	
M	0°		8°	

VIEW A-A  
OPTIONAL CONSTRUCTIONS

### RECOMMENDED SOLDERING FOOTPRINT\*



### GENERIC MARKING DIAGRAMS\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- W = Week Code (SSG)
- M = Month Code (SSG)
- G = Pb-Free Package
- AKA = Polarity Indicator

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

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STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	D <sup>2</sup> PAK-3 (TO-263, 3-LEAD)	PAGE 1 OF 2



ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY D. TRUHITE.	04 APR 2011
A	CORRECTED PITCH ON SOLDER FOOTPRINT TO BE FROM CENTER LINE TO LEAD. REQ. BY D. TRUHITE.	25 JUL 2011
B	ADDED GENERIC MARKING DIAGRAM FOR SSG. REQ. BY I. CAMBALIZA.	08 OCT 2013

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