DSC2111 | DSC2211

discera

Low-Jitter I²C/SPI Programmable Dual CMOS Oscillator

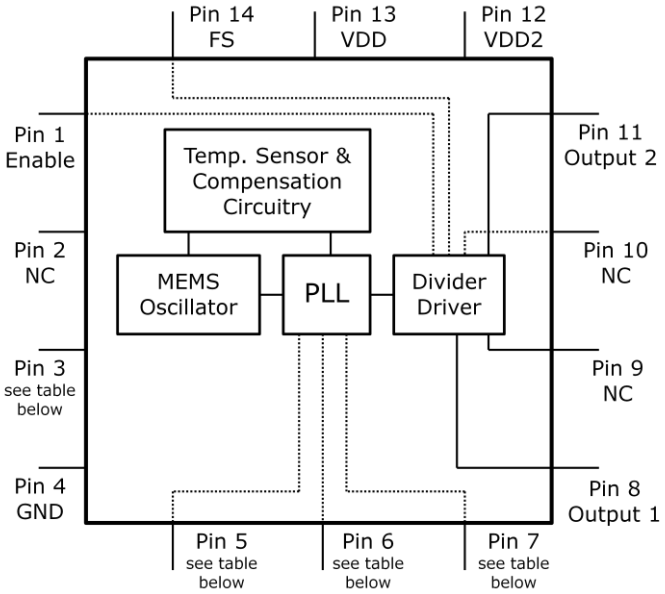
Datasheet

General Description

The DSC2111 and DSC2211 series of programmable, high-performance dual CMOS oscillators utilizes a proven silicon MEMS technology to provide excellent jitter and stability while incorporating high output frequency flexibility and drive strength control. DSC2111 and DSC2211 allow the user to independently modify the frequency of each output and CMOS drive strength using I²C or SPI interface, respectively. User can also select from two pre-programmed default output frequencies using the control pin.

DSC2111 and DSC2211 are packaged in 14-pin 3.2x2.5 mm QFN packages and available in temperature grades from Ext. Commercial to Automotive.

Block Diagram



Pin #	DSC2111 (I²C)	DSC2211 (SPI)
3	NC	SCLK
5	SDA	MOSI
6	SCL	MISO
7	CS_bar	SS

Features

- **Low RMS Phase Jitter: <1 ps (typ)**
- **High Stability: ±25, ±50 ppm**
- **Wide Temperature Range**
  - Automotive: -55° to 125° C
  - Ext. Industrial: -40° to 105° C
  - Industrial: -40° to 85° C
  - Ext. commercial: -20° to 70° C
- **High Supply Noise Rejection: -50 dBc**
- **Two Independent CMOS Outputs**
- **I²C/SPI Programmable Freq & Drive**
- **Short Lead Times: 2 Weeks**
- **Wide Frequency Range:**
  - CMOS Output: 2.3 to 170 MHz
- **Miniature Footprint of 3.2x2.5mm**
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **High Reliability**
  - 20x better MTF than quartz oscillators
- **Supply Range of 2.25 to 3.6 V**
- **Lead Free & RoHS Compliant**

Applications

- **Storage Area Networks**
  - SATA, SAS, Fibre Channel
- **Passive Optical Networks**
  - EPON, 10G-EPON, GPON, 10G-PON
- **Ethernet**
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- **HD/SD/SDI Video & Surveillance**
- **PCI Express**

Pin Description

Pin No.	Pin Name	Pin Type	Description
1	Enable	I	Enables outputs when high and disables when low
2	NC	NA	Leave unconnected or grounded
3	NC	NA	DSC2111: Leave unconnected or grounded
	SCLK	I	DSC2211: Serial clock from master
4	GND	Power	Ground
5	SDA	I	DSC2111: I²C Serial Data
	MOSI		DSC2211: SPI Serial Data from Master to Slave
6	SCL	I	DSC2111: I²C Serial Clock
	MISO	O	DSC2211: SPI Serial Data from Slave to Master
7	CS_bar	I	DSC2111: I²C Chip Select (Active Low)
	SS	I	DSC2211: SPI Slave Select (Active Low)
8	Output1	O	CMOS output 1
9	NC	NA	Leave unconnected or grounded
10	NC	NA	Leave unconnected or grounded
11	Output2	O	CMOS output 2
12	VDD2	Power	Power Supply for CMOS Output 2
13	VDD	Power	Power Supply
14	FS	I	Default output clock frequency bit

Operational Description

The DSC2111/2211 is a dual CMOS oscillator consisting of a MEMS resonator and a support PLL IC. The outputs are generated through independent 8-bit programmable dividers from the output of the internal PLL.

DSC2111/2211 allows for easy programming of the output frequencies using I²C/SPI interface. Upon power-up, the initial output frequencies are controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for two different default frequency pairs. The control pin (FS) selects the initial pair. Once the device is powered up, a new output frequency pair can be programmed using I²C/SPI pins. Programming details are provided in the ***Programming Guide***. Standard default frequency pairs are described in the following sections. Discera supports customer defined versions.

The DSC2111/2211 has independent control of the output voltage levels of the two outputs. The high voltage level of Output 1 is equal to the main supply voltage, VDD (pin 13). VDD2 (pin 12) sets the high voltage level of Output 2. VDD2 must be equal to or less than VDD. VDD2 can be as low as 1.65V.

When Enable (pin 1) is floated or connected to VDD, the DSC2111/2211 is in operational mode. Driving Enable to ground will disable both output drivers (hi-impedance mode).

The DSC2111/2211 has programmable output drive strength, which can be controlled via I²C/SPI. Table 1 displays typical rise / fall times for the output with a 15pf load capacitance as a function of these control bits at VDD=3.3V and room temperature.

Table 1. Rise/Fall times for drive strengths

	Output Drive Strength Bits [OXS2, OXS1, OXS0] - Default [**111**] X=1 for output1, and 2 for output2							
	000	001	010	011	100	101	110	**111**
tr (ns)	2.1	1.7	1.6	1.4	1.3	1.3	1.2	**1.1**
tf (ns)	2.5	2.4	2.4	2	1.8	1.6	1.3	**1.3**

Output Clock Frequencies

Table 2 lists the standard default frequency configurations and the associated ordering information to be used in conjunction with the ordering code. Customer defined combinations are available.

Table 2. Pre-programmed pin-selectable output frequency pairs

Ordering Info	Freq (MHz)	Select Bit [FS] – **Default is [1]**	
		0	**1**
E0001	f_{OUT1}	27	**25**
	f_{OUT2}	24	**125**
E0002	f_{OUT1}	106.25	**100**
	f_{OUT2}	25	**100**
E0004	f_{OUT1}	24	**75**
	f_{OUT2}	24	**75**
E0005	f_{OUT1}	25	**0***
	f_{OUT2}	25	**0***
E0006	f_{OUT1}	27	**74.175**
	f_{OUT2}	13.5	**37.0875**
E0007	f_{OUT1}	24	**0***
	f_{OUT2}	40	**0***
E0008	f_{OUT1}	40	**40**
	f_{OUT2}	200	**128**
EXXXX	f_{OUT1}	Contact factory for additional configurations.	
	f_{OUT2}		

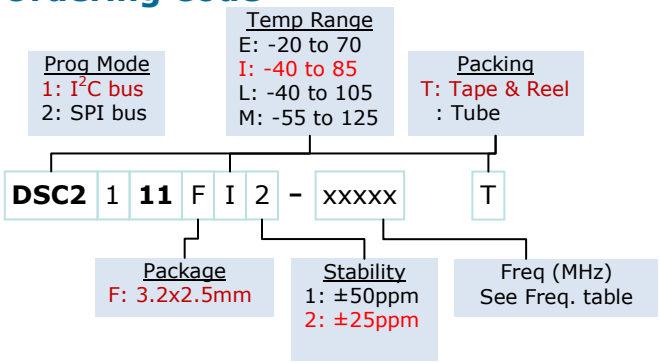
Frequency select bit are weakly tied high so if left unconnected the default setting will be [1] and the device will output the associated frequency highlighted in **Bold**.
0* – denotes invalid selection, output frequency is not specified.

Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V_{DD}+0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD HBM MM CDM	-	 4000 400 1500	V	

Note: 1000+ years of data retention on internal memory

Ordering Code

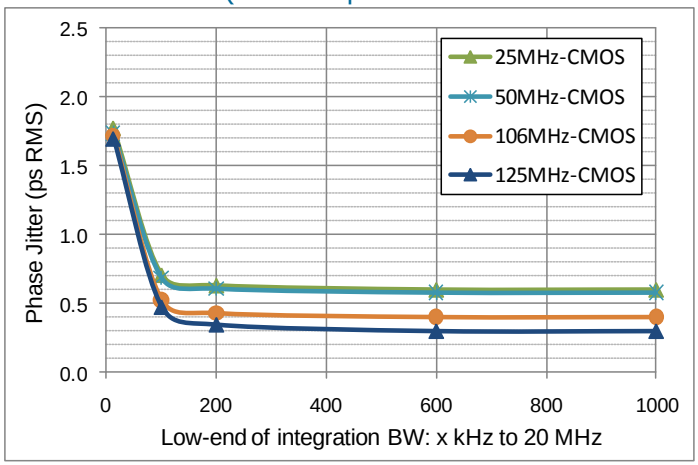


Specifications (Unless specified otherwise: T=25° C)

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage[1]	V_{DD}		2.25		3.6	V
Supply Voltage (Output2)[1]	V_{DD2}		1.65		3.6	V
Supply Current	I_{DD}	EN pin low – outputs are disabled		21	23	mA
Supply Current[2]	I_{DD}	EN pin high – outputs are enabled C_L=15Ω, F_{O1}=F_{O2} =125 MHz		32		mA
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±25 ±50	ppm
Aging	Δf	1 year @25°C			±5	ppm
Startup Time[3]	t_{SU}	T=25°C			5	ms
Input Logic Levels Input logic high Input logic low	 V_{IH} V_{IL}		 0.75xV_{DD} -		 - 0.25xV_{DD}	V
Output Disable Time[4]	t_{DA}				5	ns
Output Enable Time	t_{EN}				20	ns
Pull-Up Resistor[2]		Pull-up exists on all digital IO		40		kΩ
CMOS Outputs						
Output Logic Levels Output logic high Output logic low	 V_{OH} V_{OL}	I=±6mA	 0.9xV_{DD} -		 - 0.1xV_{DD}	V
Output Transition time[4] Rise Time Fall Time	 t_R t_F	20% to 80% C_L=15pf		 1.1 1.4	 2 2	ns
Frequency	f_0	Commercial/Industrial temp range Automotive temp range	2.3		170 100	MHz
Output Duty Cycle	SYM		45		55	%
Period Jitter[5]	J_{PER}	F_{O1}=F_{O2}=125 MHz		3		ps_{RMS}
Integrated Phase Noise	J_{CC}	200kHz to 20MHz @ 125MHz 100kHz to 20MHz @ 125MHz 12kHz to 20MHz @ 125MHz		0.3 0.38 1.7	 2	ps_{RMS}

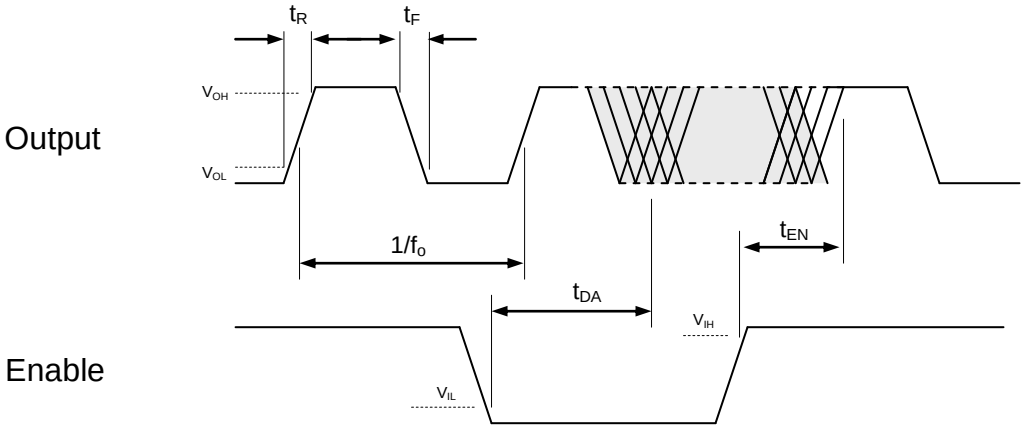
Notes:
1. Pin 4 V_{DD} should be filtered with 0.01uf capacitor.
2. Output is enabled if Enable pad is floated or not connected.
3. t_{su} is time to 100PPM stable output frequency after V_{DD} is applied and outputs are enabled.
4. Output Waveform and Test Circuit figures below define the parameters.
5. Period Jitter includes crosstalk from adjacent output.

Nominal Performance Parameters (Unless specified otherwise: T=25° C, V_{DD}=3.3 V)

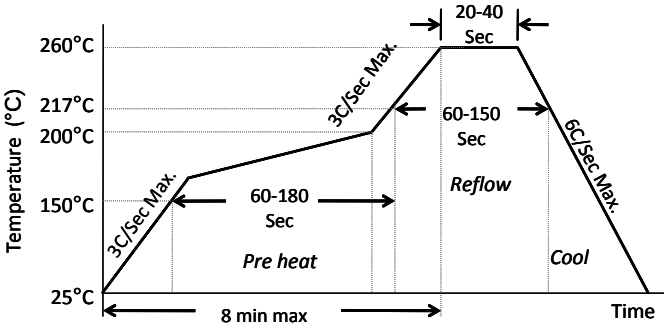


CMOS Phase jitter (integrated phase noise)

Output Waveform: CMOS



Solder Reflow Profile

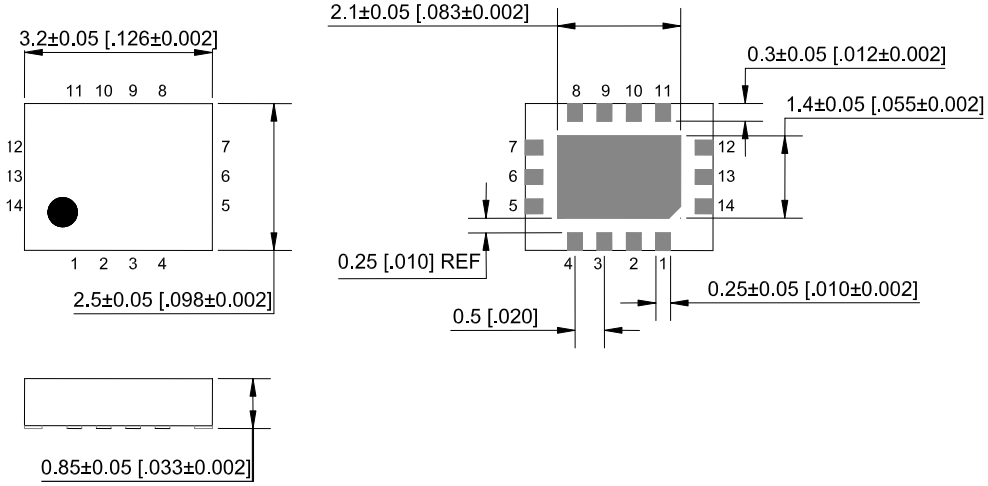


MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

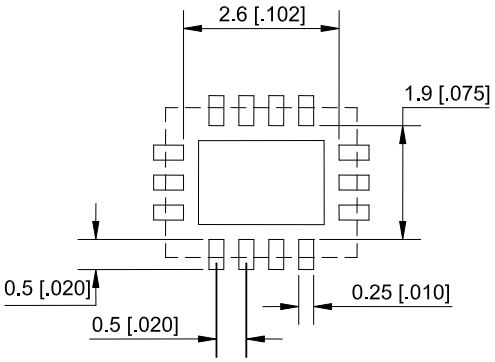
Package Dimensions

3.2 x 2.5 mm 14 Lead Plastic Package

External Dimensions
units: mm[inch]



Recommended
Solder Pad Layout
units: mm[inch]



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