PIC18F8410/8490/8493 FAMILY

Programming Specifications for PIC18F8410/8490/8493 Family Flash MCUs

1.0 DEVICE OVERVIEW

This document includes the programming specifications for the following devices:

- PIC18F6310
- PIC18F6410
- PIC18F8310
- PIC18F8410
- PIC18F6390
- PIC18F6490
- PIC18F8390
- PIC18F8490
- PIC18F6393
- PIC18F6493
- PIC18F8393
- PIC18F8493

2.0 PROGRAMMING OVERVIEW OF THE PIC18F8410/8490/8493 FAMILY

PIC18F8410/8490/8493 family devices can be programmed using the high-voltage In-Circuit Serial Programming™ (ICSP™) method.

This can be done with the device in the user's system. This programming specification applies to PIC18F8410/8490/8493 family devices in all package types.

2.1 Hardware Requirements

In High-Voltage ICSP mode, the PIC18F8410/8490/8493 family devices require two programmable power supplies: one for VDD and one for $\overline{\text{MCLR}}$/VPP. Both supplies should have a minimum resolution of 0.25V. Refer to **Section 6.0 "AC/DC Characteristics Timing Requirements for Program/Verify Test Mode"** for additional hardware parameters.

2.2 Pin Diagrams

The pin diagrams for the PIC18F8410/8490/8493 family are shown in Figure 2-1 through Figure 2-4.

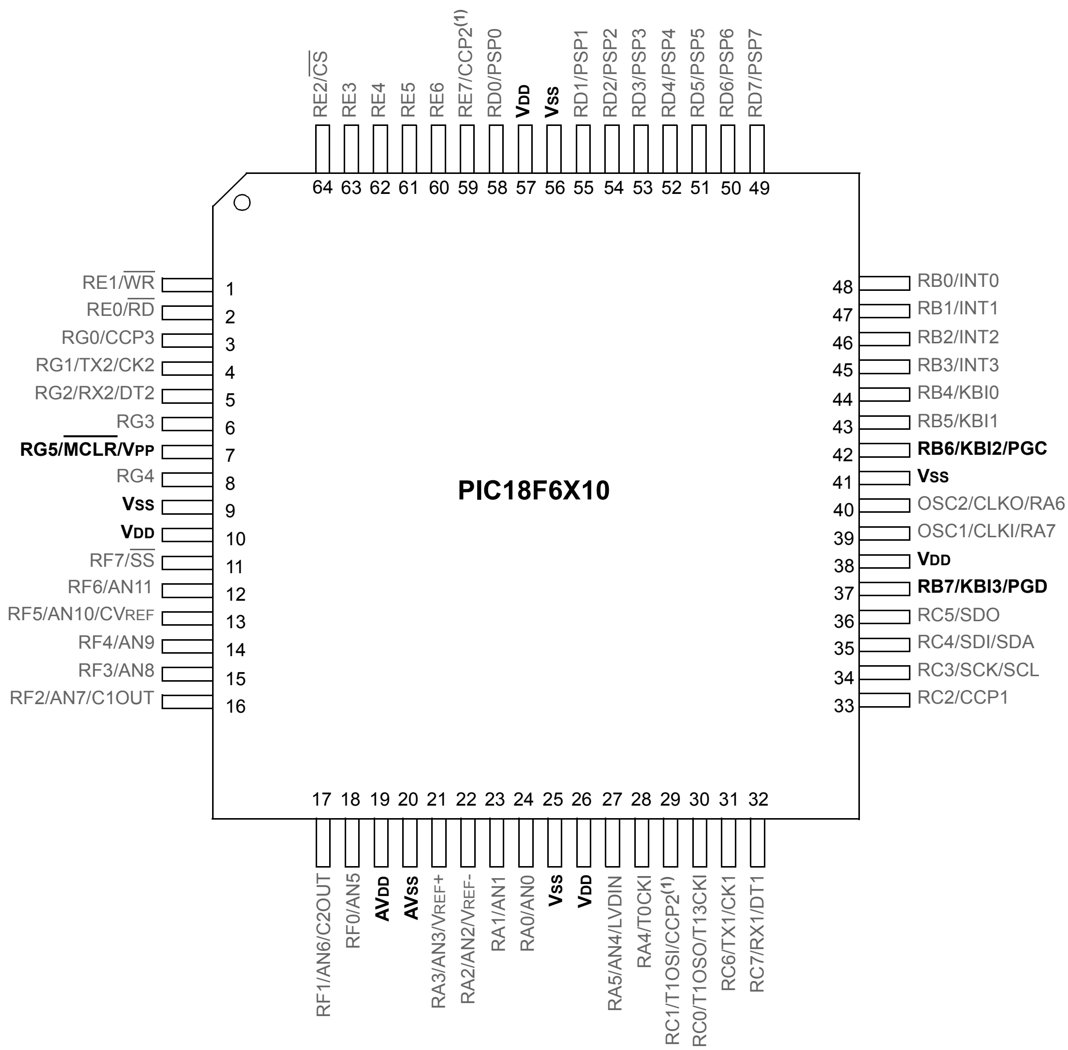
TABLE 2-1 PIN DESCRIPTIONS (DURING PROGRAMMING): PIC18F8410/8490/8493 FAMILY

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
RG5/$\overline{\text{MCLR}}$/VPP	VPP	P	Programming Enable
VDD(1)	VDD	P	Power Supply
VSS(1)	VSS	P	Ground
RB6/PGC	PGC	I	Serial Clock
RB7/PGD	PGD	I/O	Serial Data

Legend: I = Input, O = Output, P = Power

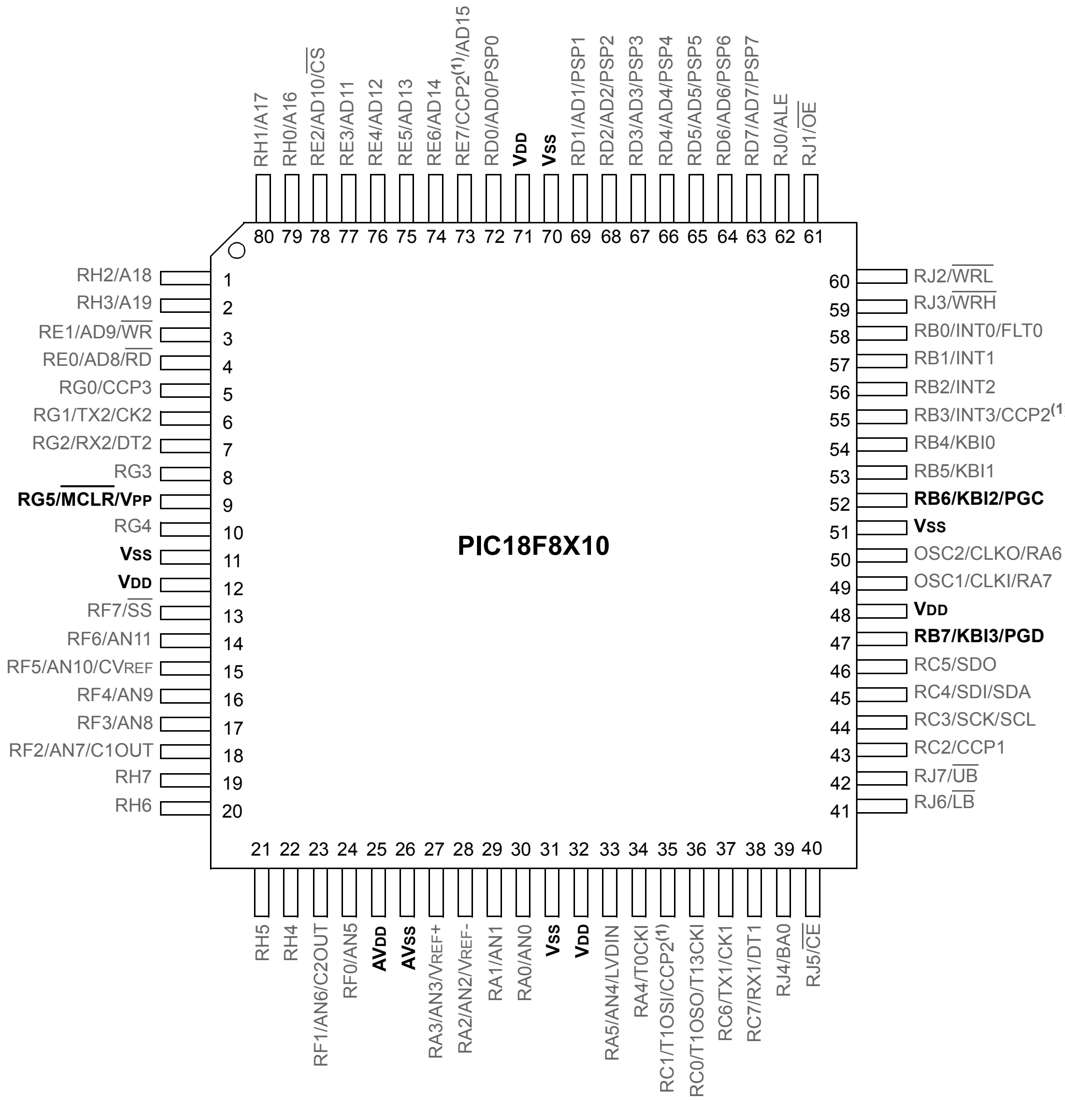
Note 1: All power supply (VDD) and ground (VSS) must be connected.

FIGURE 2-1: PIC18F6X10 FAMILY PIN DIAGRAM



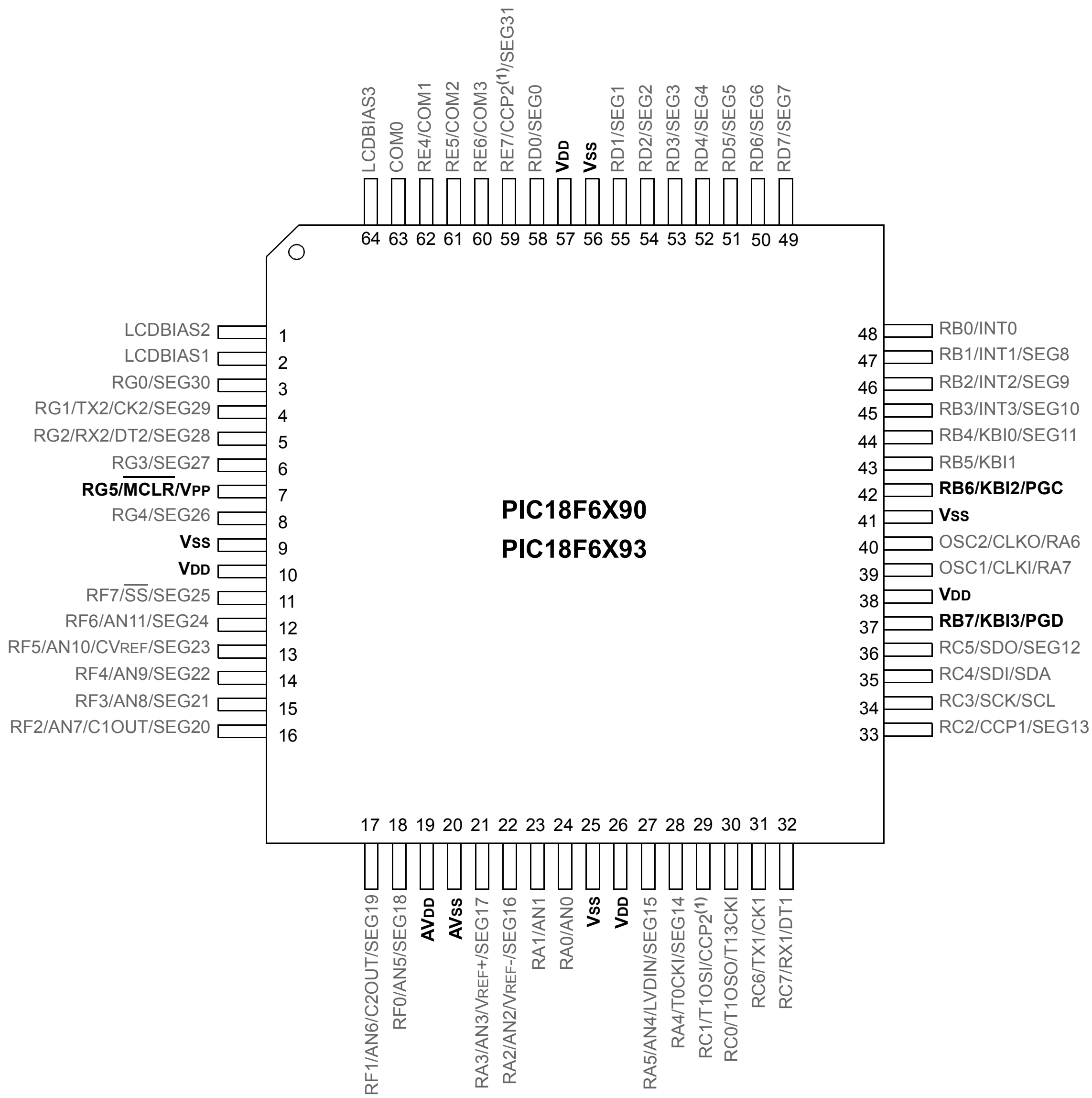
Note 1: RE7 is the alternate pin for CCP2 multiplexing.

FIGURE 2-2: PIC18F8X10 FAMILY PIN DIAGRAM



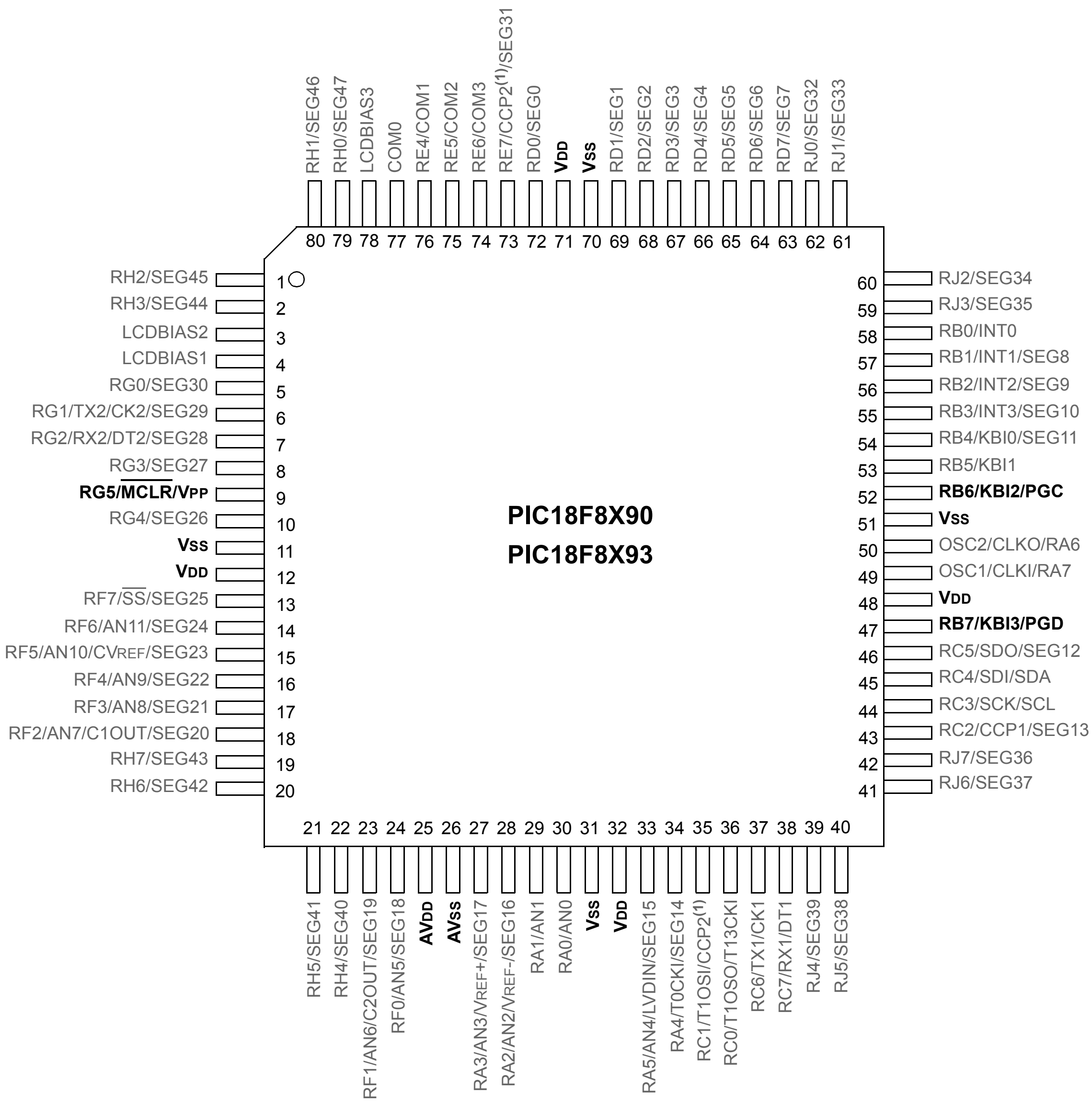
Note 1: RE7 is the alternate pin for CCP2 multiplexing.

FIGURE 2-3: PIC18F6X90/6X93 FAMILY PIN DIAGRAM



Note 1: RE7 is the alternate pin for CCP2 multiplexing.

FIGURE 2-4: PIC18F8X90/8X93 FAMILY PIN DIAGRAM



Note 1: RE7 is the alternate pin for CCP2 multiplexing.

2.3 Memory Map

The code memory space extends from 000000h to 001FFFh (8 Kbytes) in a single block for PIC18FX310/X390/X393 devices and from 000000h to 003FFFh (16 Kbytes) in a single block for PIC18FX410/X490/X493 devices.

TABLE 2-2 IMPLEMENTATION OF CODE MEMORY

Device	Code Memory Size (Bytes)
PIC18F6310	000000h-001FFFh (8K)
PIC18F8310	
PIC18F6390	
PIC18F6393	
PIC18F8390	
PIC18F8393	
PIC18F6410	000000h-003FFFh (16K)
PIC18F8410	
PIC18F6490	
PIC18F6493	
PIC18F8490	
PIC18F8493	

In addition to the code memory space, there are three blocks in the configuration and ID space that are accessible to the user through table reads and table writes (in ICSP mode). Their locations in the memory map are shown in Figure 2-5.

Users may store identification information (user ID) in eight ID registers. These ID registers are mapped in addresses 200000h through 200007h. The ID locations read out normally, even after code protection is applied.

Locations 300000h through 30000Dh are reserved for the configuration bits. These bits select various device options and are described in **Section 5.0 "Configuration Word"**. These configuration bits read out normally, even after code protection.

Locations 3FFFFEh and 3FFFFFh are reserved for the device ID bits. These bits are read-only bits. These bits may be used by the programmer to identify what device type is being programmed and are described in **Section 5.0 "Configuration Word"**. These device ID bits read out normally, even after code protection.

2.3.1 MEMORY ADDRESS POINTER

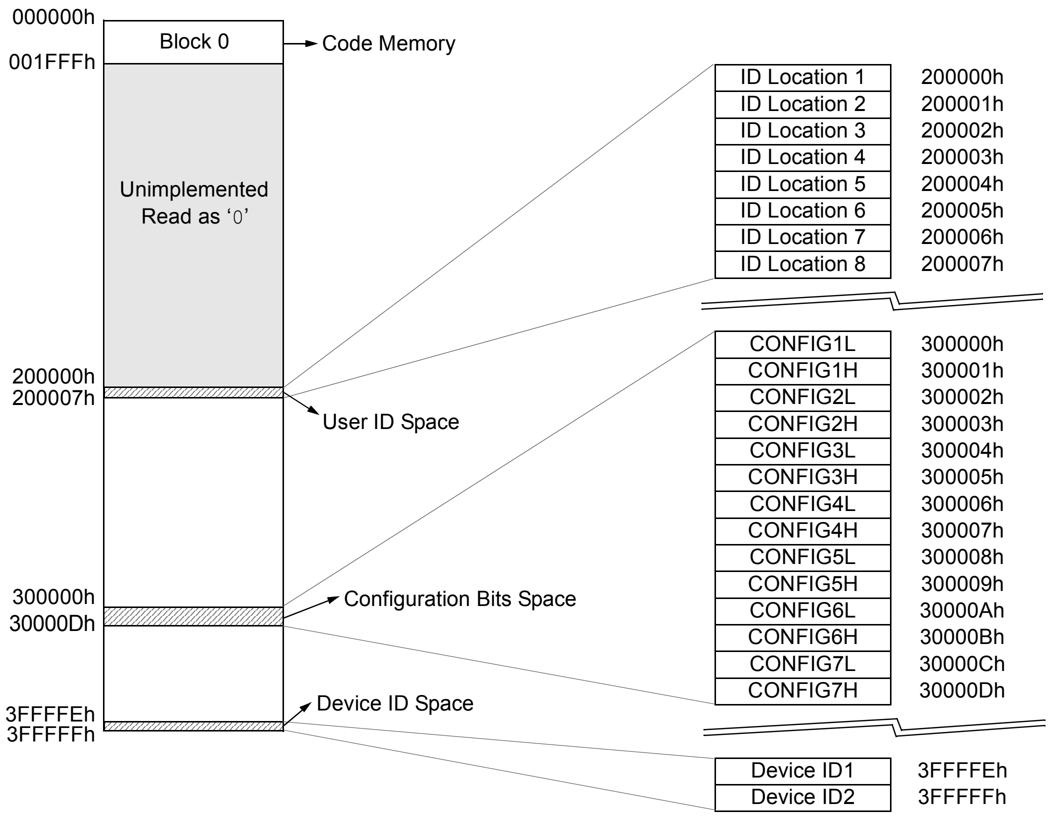
Memory in the address space 0000000h to 3FFFFFh is addressed via the Table Pointer, which is comprised of three pointer registers:

- TBLPTRU, at RAM address 0FF8h
- TBLPTRH, at RAM address 0FF7h
- TBLPTRL, at RAM address 0FF6h

TBLPTRU	TBLPTRH	TBLPTRL
Addr[21:16]	Addr[15:8]	Addr[7:0]

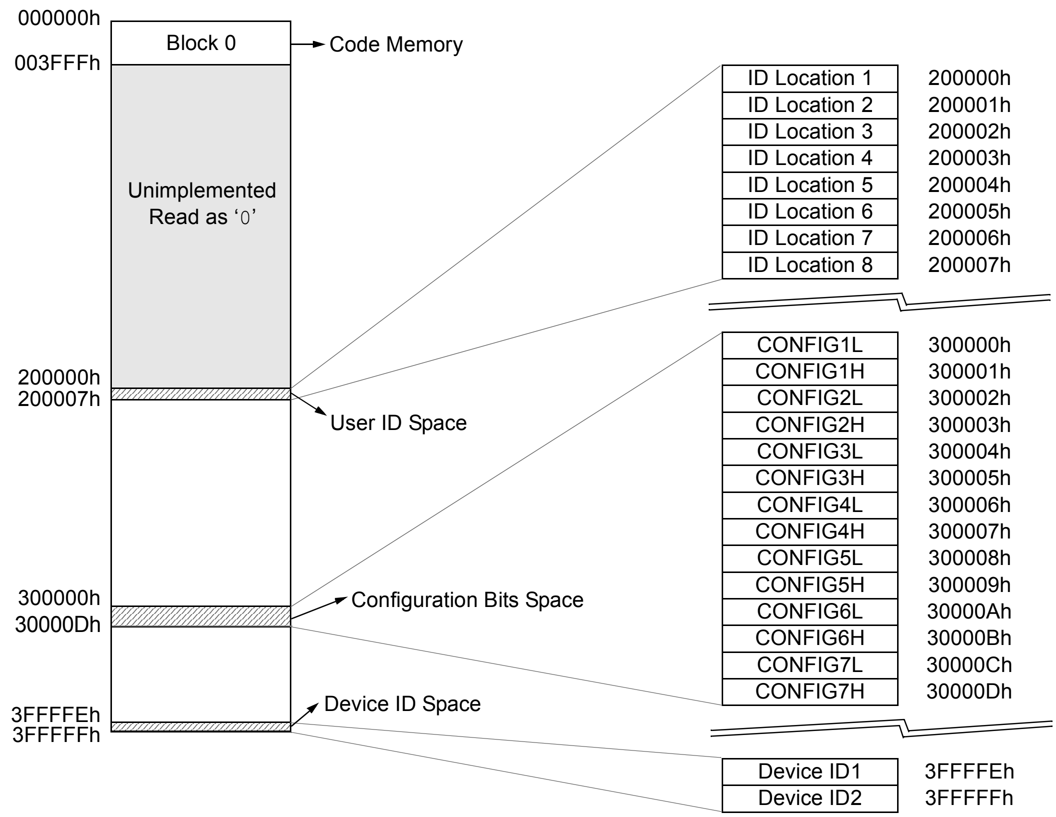
The 4-bit command, '`0000`' (core instruction), is used to load the Table Pointer prior to using many read or write operations.

FIGURE 2-5: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18FX310/X390/X393 DEVICES



Note: Sizes of memory areas are not to scale.

FIGURE 2-6: MEMORY MAP AND THE CODE MEMORY SPACE FOR PIC18FX410/X490/X493 DEVICES



Note: Sizes of memory areas are not to scale.

2.4 High-Level Overview of the Programming Process

Figure 2-8 shows the high-level overview of the programming process. The device is first checked to see if it is blank; if it is not, a Chip Erase is performed. Next, the code memory and ID locations are programmed. These memories are then verified to ensure that programming was successful. If no errors are detected, the configuration bits are then programmed and verified.

2.5 Entering High-Voltage ICSP Program/Verify Mode

The High-Voltage ICSP Program/Verify mode is entered by holding PGC and PGD low and then raising $\overline{MCLR}$/VPP to VIHH (high voltage). Once in this mode, the code memory, ID locations and configuration bits can be accessed and programmed in serial fashion.

The sequence that enters the device into the Program/Verify mode places all unused I/Os in the high-impedance state.

FIGURE 2-7: ENTERING HIGH-VOLTAGE PROGRAM/VERIFY MODE

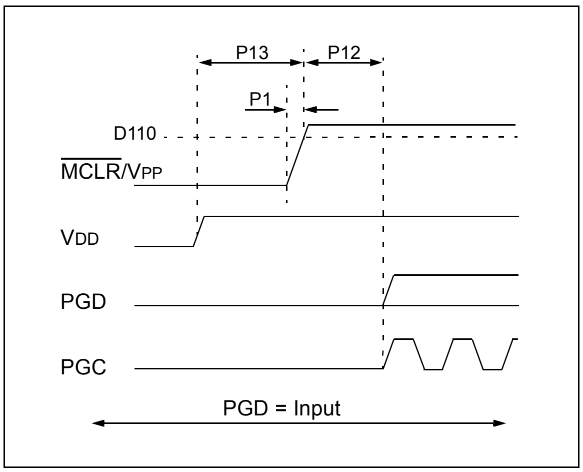
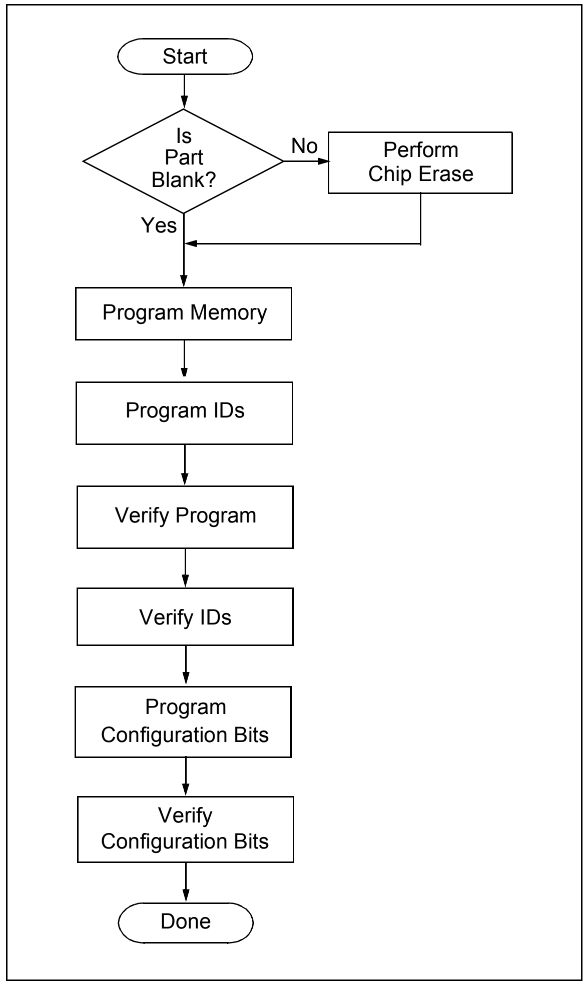


FIGURE 2-8: HIGH-LEVEL PROGRAMMING FLOW



2.6 Serial Program/Verify Operation

The PGC pin is used as a clock input pin and the PGD pin is used for entering command bits and data input/output during serial operation. Commands and data are transmitted on the rising edge of PGC, latched on the falling edge of PGC and are Least Significant bit (LSb) first.

2.6.1 4-BIT COMMANDS

All instructions are 20 bits, consisting of a leading 4-bit command, followed by a 16-bit operand, which depends on the type of command being executed. To input a command, PGC is cycled four times. The commands needed for programming and verification are shown in Table 2-3.

Depending on the 4-bit command, the 16-bit operand represents 16 bits of input data or 8 bits of input data and 8 bits of output data.

Throughout this specification, commands and data are presented as illustrated in Table 2-4. The 4-bit command is shown MSb first. The command operand, or “Data Payload”, is shown <MSB><LSB>. Figure 2-9 demonstrates how to serially present a 20-bit command/operand to the device.

2.6.2 CORE INSTRUCTION

The core instruction passes a 16-bit instruction to the CPU core for execution. This is needed to set up registers as appropriate for use with other commands.

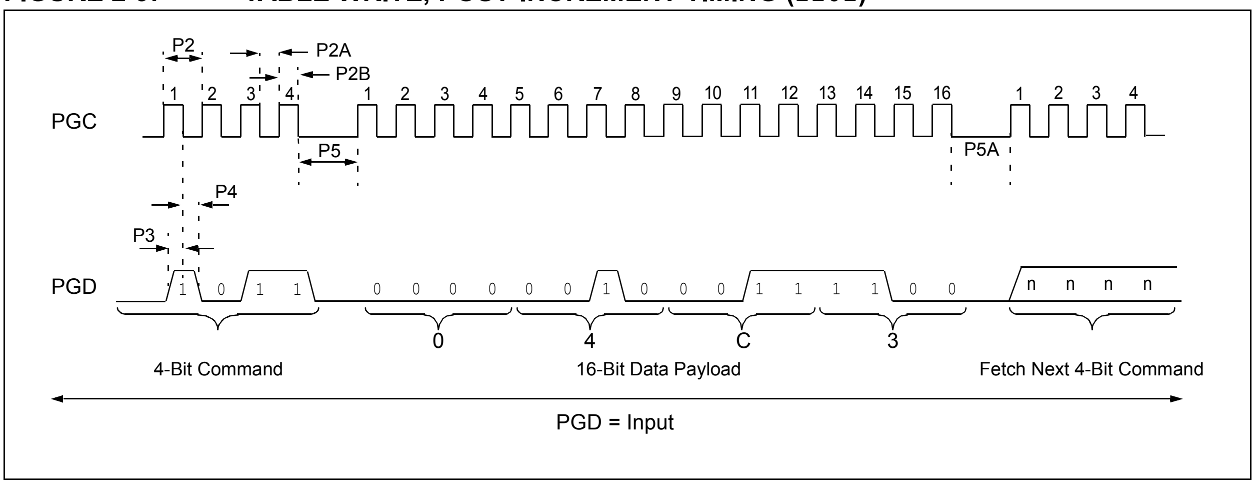
TABLE 2-3 COMMANDS FOR PROGRAMMING

Description	4-Bit Command
Core Instruction (Shift in16-bit instruction)	`0000`
Shift out TABLAT register	`0010`
Table Read	`1000`
Table Read, post-increment	`1001`
Table Read, post-decrement	`1010`
Table Read, pre-increment	`1011`
Table Write	`1100`
Table Write, post-increment by 2	`1101`
Table Write, post-decrement by 2	`1110`
Table Write, start programming	`1111`

TABLE 2-4 SAMPLE COMMAND SEQUENCE

4-Bit Command	Data Payload	Core Instruction
`1101`	`3C 40`	`Table Write, post-increment by 2`

FIGURE 2-9: TABLE WRITE, POST-INCREMENT TIMING (`1101`)



3.0 DEVICE PROGRAMMING

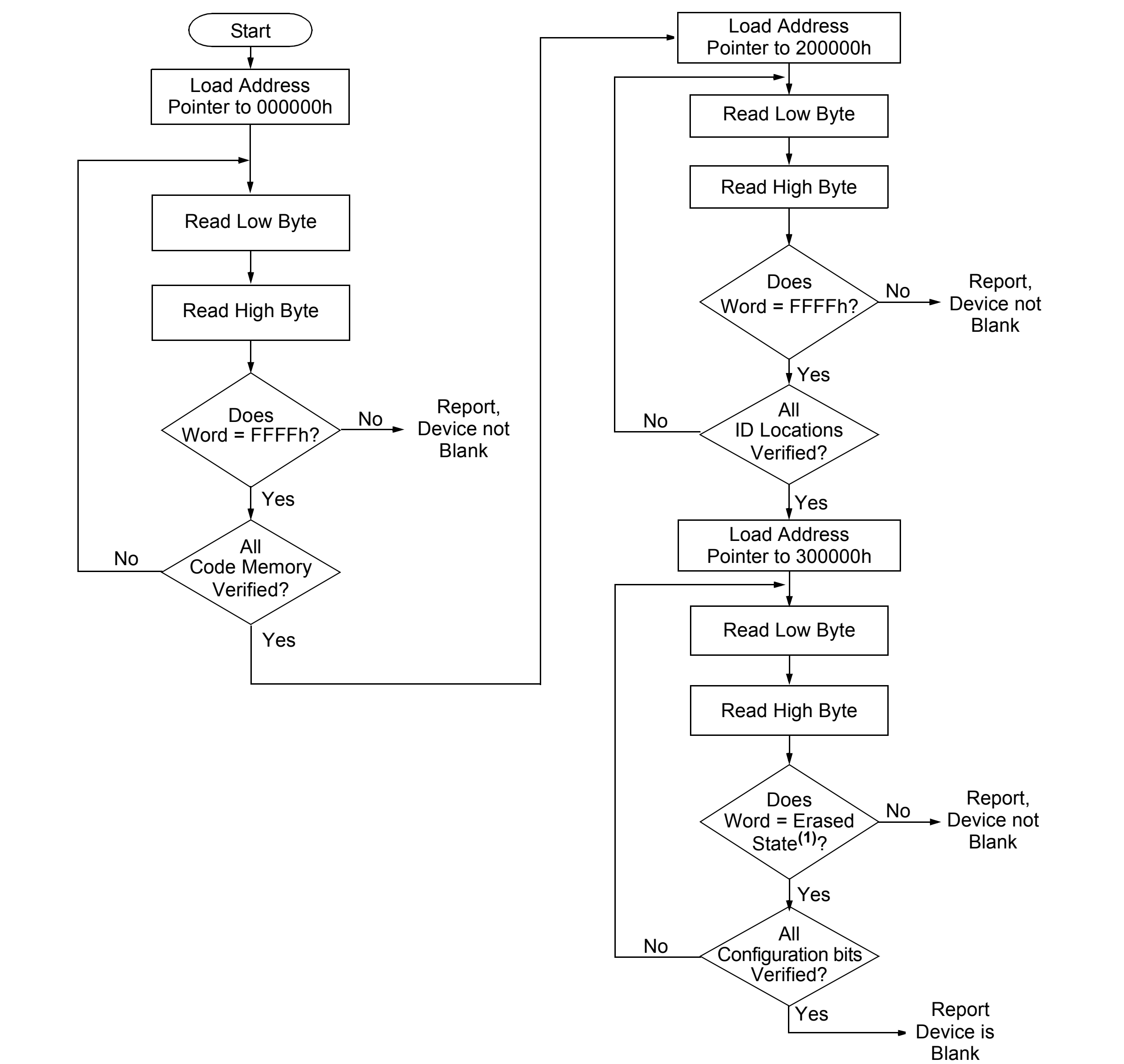
3.1 Blank Check

The term "Blank Check" means to verify that the device has no programmed memory cells. All memories must be verified: code memory, ID locations and configuration bits. The Device ID registers (3FFFFEh:3FFFFFh) should be ignored. The blank checking step involves reading the code memory space and comparing it against FFFFh. Memory reads occur a single byte at a time, so two bytes must be read to compare against FFFFh. Refer to **Section 4.1 "Read Code Memory, ID Locations and Configuration Bits"**.

A "Blank" or "Erased" memory cell will read as a '1'. So, "Blank Checking" a device merely means to verify that all bytes read as FFh, except the configuration bits. Unused (reserved) configuration bits will read as '0'. Refer to Table 5-3 for blank configuration except data for the various PIC18F8410/8490/8493 family devices.

If it is determined that the device is not blank, then the device should be Erased (see **Section 3.2 "High-Voltage ICSP Chip Erase"**) before any attempt to program is made.

FIGURE 3-1: BLANK CHECK FLOW



Note 1: The erased state of configuration bits are given in Table 5-2.

3.2 High-Voltage ICSP Chip Erase

Erasing code is accomplished by writing an “erase option” to address 3C0004h. Code memory is erased by erasing the entire device in one action. “Chip Erase” operations will also clear any code-protect settings. Chip Erase is detailed in Table 3-1.

TABLE 3-1 CHIP ERASE OPTION

Description	Data
Chip Erase	018Ah

The actual Chip Erase function is a self-timed operation. Once the erase has started (falling edge of the 4th PGC after the `NOP` instruction), serial execution will cease until the erase completes (parameter P11). During this time, PGC may continue to toggle, but PGD must be held low. Refer to Figure 3-3.

The code sequence to erase the entire device is shown in Table 3-2 and the flowchart is shown in Figure 3-2.

> **Note:** A Chip Erase is the only way to reprogram code-protect bits from an ON state to an OFF state.

TABLE 3-2 CHIP ERASE COMMAND SEQUENCE

4-Bit Command	Data Payload	Core Instruction
0000	0E 3C	MOVLW 3Ch
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 05	MOVLW 05h
0000	6E F6	MOVWF TBLPTRL
1100	01 0A	Write 01 to 3C0005h
0000	0E 04	MOVLW 04h
0000	6E F6	MOVWF TBLPTRL
1100	01 8A	Write 8Ah TO 3C0004h to erase device.
0000	00 00	NOP
0000		Hold PGD low until erase completes.

FIGURE 3-2: CHIP ERASE FLOW

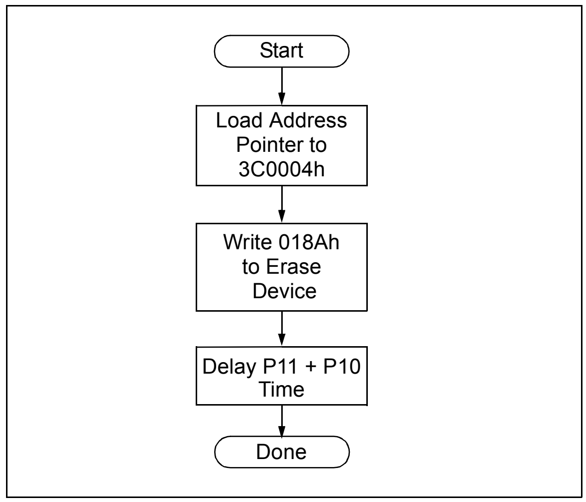
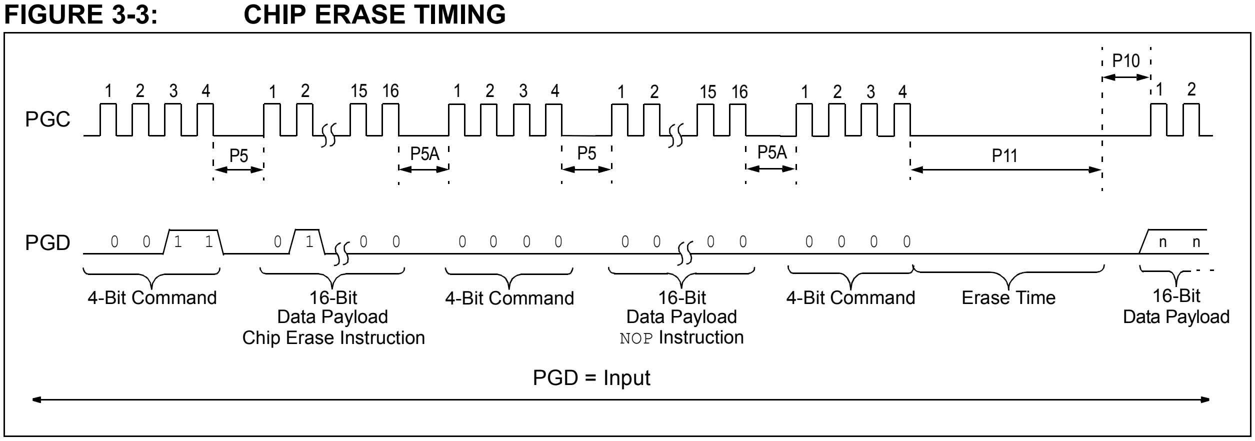


FIGURE 3-3: CHIP ERASE TIMING



3.3 Code Memory Programming

Programming code memory is accomplished by first loading data into the appropriate write buffers and then initiating a programming sequence. The write buffer is 16 bytes in size and can be mapped to any 16-byte area in code memory (see Figure 3-4). The actual memory write sequence takes the contents of these buffers and programs the 16-byte code memory region pointed to by the Table Pointer once the programming sequence is initiated.

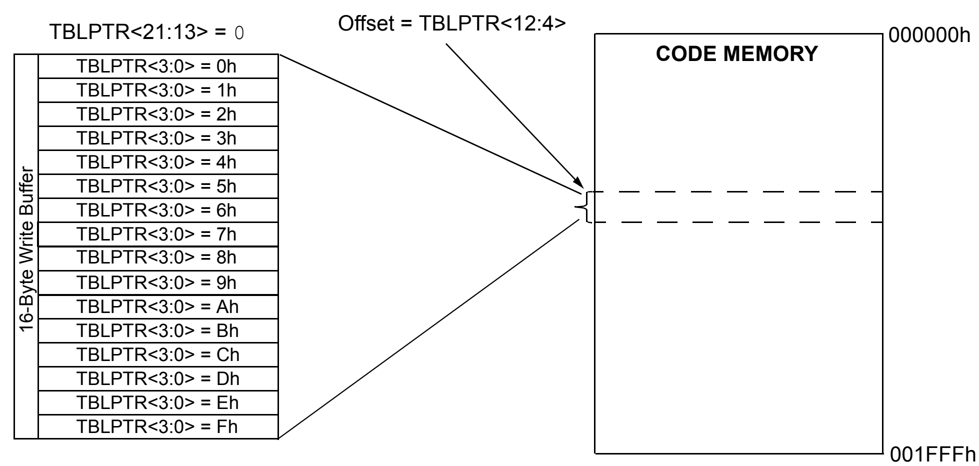
The programming duration is externally timed and is controlled by PGC. After a "Start Programming" command is issued (4-bit command, '`1111`'), a `NOP` is issued, where the 4th PGC is held high for the duration of the programming time, P9 (see Figure 3-7).

After PGC is brought low, the programming sequence is terminated. PGC must be held low for the time specified by parameter P10 to allow high-voltage discharge of the memory array.

The code sequence to program a PIC18F8410/8490/8493 family device is shown in Table 3-3. The flowchart shown in Figure 3-6 depicts the logic necessary to completely write a PIC18F8410/8490/8493 family device. The timing diagram that details the "Start Programming" command and parameter P10, is shown in Figure 3-7.

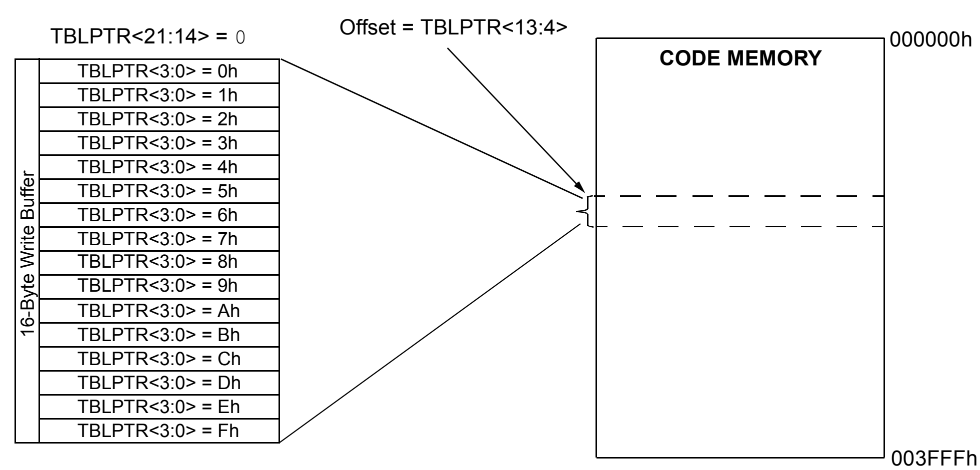
Note:	The TBLPTR register must contain the same offset value when initiating the programming sequence as it did when the write buffers were loaded.

FIGURE 3-4: WRITE BOUNDARIES FOR PIC18FX310/X390/X393 DEVICES



Note: TBLPTR = TBLPTRU:TBLPTRH:TBLPTRL.

FIGURE 3-5: WRITE BOUNDARIES FOR PIC18FX410/X490/X493 DEVICES



Note: TBLPTR = TBLPTRU:TBLPTRH:TBLPTRL.

TABLE 3-3 WRITE CODE MEMORY CODE SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Direct access to code memory and enable writes.		
0000 0000	9C A6 84 A6	BCF EECON1, CFGS BSF EECON1, WREN
Step 2: Load write buffer.		
0000 0000 0000 0000 0000 0000 1101 . . 1101 1111 0000	0E <Addr[21:16]> 6E F8 0E <Addr[15:8]> 6E F7 0E <Addr[7:0]> 6E F6 <LSB><MSB> . . <LSB><MSB> <LSB><MSB> 00 00	MOVLW <Addr[21:16]> MOVWF TBLPTRU MOVLW <Addr[15:8]> MOVWF TBLPTRH MOVLW <Addr[7:0]> MOVWF TBLPTRL Write 2 bytes (First Word) and post-increment address by 2 . . Write 2 bytes (Seventh Word) and post-increment address by 2 Write 2 bytes (Eighth Word) and start programming NOP
To continue writing data, repeat step 2, where the address pointer is incremented by 16 at each iteration of the loop.		

FIGURE 3-6: PROGRAM CODE MEMORY FLOW

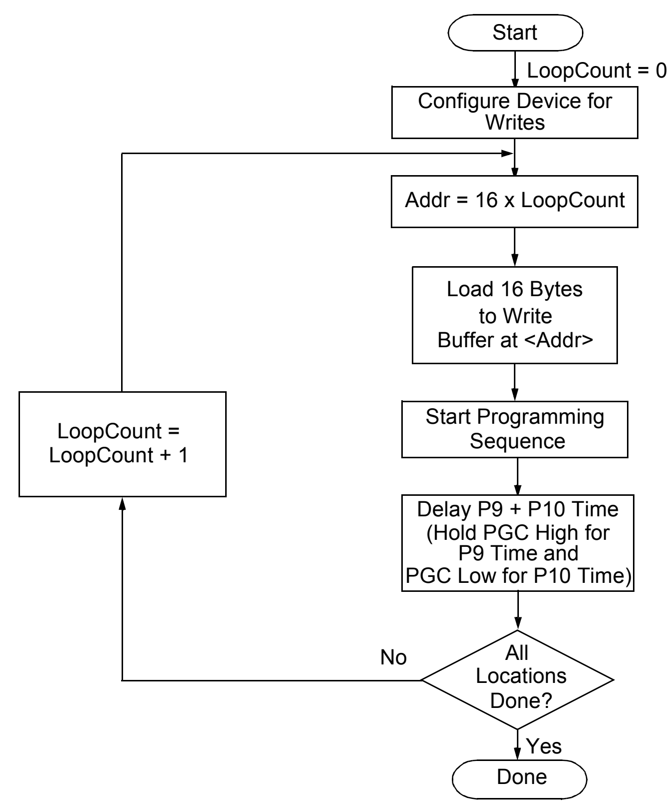
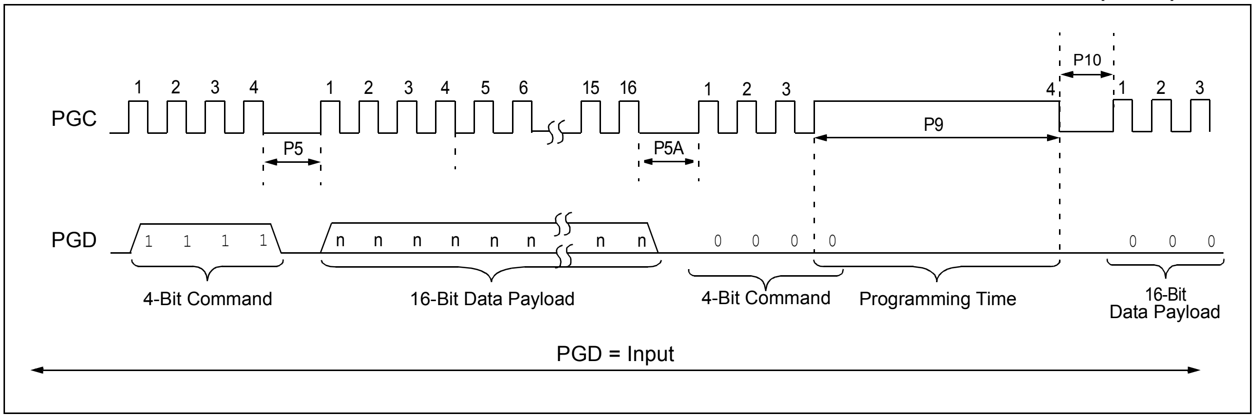


FIGURE 3-7: TABLE WRITE AND START PROGRAMMING INSTRUCTION TIMING (1111)



3.4 ID Location Programming

The ID locations are programmed much like the code memory. The ID registers are mapped in addresses 200000h through 200007h. These locations read out normally, even after code protection.

Note:	The user only needs to fill the 8-byte data buffer to program the ID locations.

Table 3-4 demonstrates the code sequence required to write the ID locations.

The Table Pointer must be manually set to 200000h (base address of the ID locations). The post-increment feature of the table read 4-bit command should not be used to increment the Table Pointer to 200000h. After setting the Table Pointer to 200000h, the post-increment feature may be used to increment to 200001h, 200002h and so on.

TABLE 3-4 WRITE ID SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Direct access to code memory.		
0000	9C A6	BCF EECON1, CFGS
0000	84 A6	BSF EECON1, WREN
Step 2: Load write buffer. Panel will be automatically determined by address.		
0000	0E 20	MOVLW 20h
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 00	MOVLW 00h
0000	6E F6	MOVWF TBLPTRL
1101	<LSB><MSB>	Write 2 bytes and post-increment address by 2
1101	<LSB><MSB>	Write 2 bytes and post-increment address by 2
1101	<LSB><MSB>	Write 2 bytes and post-increment address by 2
1111	<LSB><MSB>	Write 2 bytes and start programming
0000	00 00	NOP

3.5 Boot Block Programming

The PIC18F8410/8490/8493 family devices do not have any Boot Block segment. When the PIC18F8310/8410 devices are configured in Microprocessor with Boot Block mode, the locations from 0000h to 07FFh will be internal memory. This memory region is programmed in exactly the same manner as the code memory (see **Section 3.3 "Code Memory Programming"**).

The code sequence detailed in Table 3-3 should be used, except that the address data used in "Step 2" will be in the range 000000h to 0007FFh.

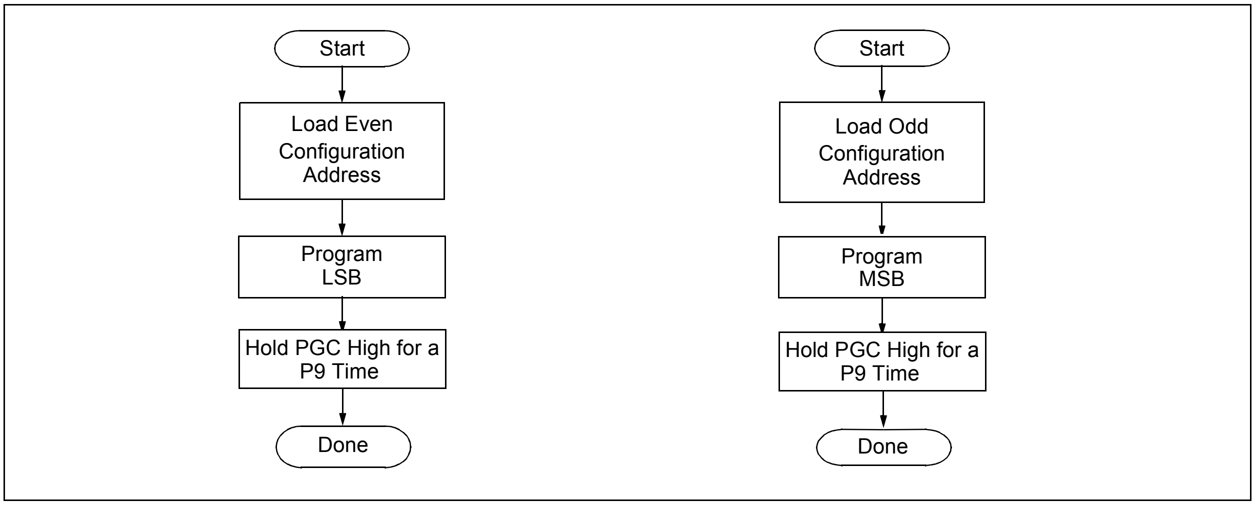
3.6 Configuration Bits Programming

Unlike code memory, the configuration bits are programmed a byte at a time. The write operation programs only 8 bits of the 16-bit payload written. The LSB of the payload will be written to even addresses and the MSB will be written to odd addresses. The code sequence to program two consecutive configuration locations is shown in Table 3-5.

TABLE 3-5 SET ADDRESS POINTER TO CONFIGURATION LOCATION

4-Bit Command	Data Payload	Core Instruction
Step 1: Direct access to config memory.		
0000 0000	84 A6 8C A6	BSF EECON1, WREN BSF EECON1, CFGS
Step 2: Set Table Pointer for config byte to be written. Write even addresses.		
0000 0000 0000 0000 0000 0000 1111 0000 0000 1111 0000	0E 30 6E F8 0E 00 6E F7 0E 00 6E F6 <LSB><MSB ignored> 00 00 2A F6 <LSB ignored><MSB> 00 00	MOVLW 30h MOVWF TBLPTRU MOVLW 00h MOVWF TBLPRTH MOVLW 00h MOVWF TBLPTRL Load 2 bytes and start programming NOP - hold PGC high for time P9 INCF TBLPTRL Load 2 bytes and start programming NOP - hold PGC high for time P9

FIGURE 3-8: CONFIGURATION PROGRAMMING FLOW



4.0 READING THE DEVICE

4.1 Read Code Memory, ID Locations and Configuration Bits

Code memory is accessed one byte at a time via the 4-bit command, '1001' (table read, post-increment). The contents of memory pointed to by the Table Pointer (TBLPTRU:TBLPTRH:TBLPTRL) is serially output on PGD.

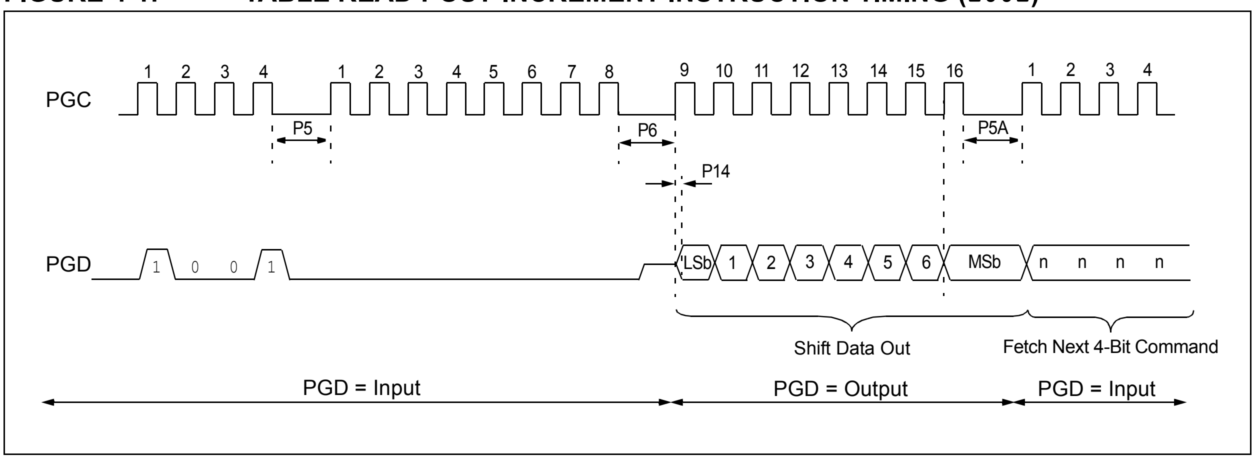
The 4-bit command is shifted in LSb first. The read is executed during the next 8 clocks, then shifted out on PGD during the last 8 clocks, LSb to MSb. A delay of P6 must be introduced after the falling edge of the 8th PGC of the operand to allow PGD to transition from an input to an output. During this time, PGC must be held low (see Figure 4-1). This operation also increments the Table Pointer by one, pointing to the next byte in code memory for the next read.

This technique will work to read any memory in the 000000h to 3FFFFFh address space, so it also applies to the reading of the ID and Configuration registers.

TABLE 4-1 READ CODE MEMORY SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Direct access to code memory.		
0000	8C A6	BCF EECON1, CFGS
Step 1: Set Table Pointer.		
0000 0000 0000 0000 0000 0000	0E <Addr[21:16]> 6E F8 0E <Addr[15:8]> 6E F7 0E <Addr[7:0]> 6E F6	MOVLW Addr[21:16] MOVWF TBLPTRU MOVLW <Addr[15:8]> MOVWF TBLPTRH MOVLW <Addr[7:0]> MOVWF TBLPTRL
Step 2: Read memory into Table Latch and then shift out on PGD, LSb to MSb.		
1001	00 00	TBLRD *+

FIGURE 4-1: TABLE READ POST-INCREMENT INSTRUCTION TIMING (1001)



4.2 Verify Code Memory and ID Locations

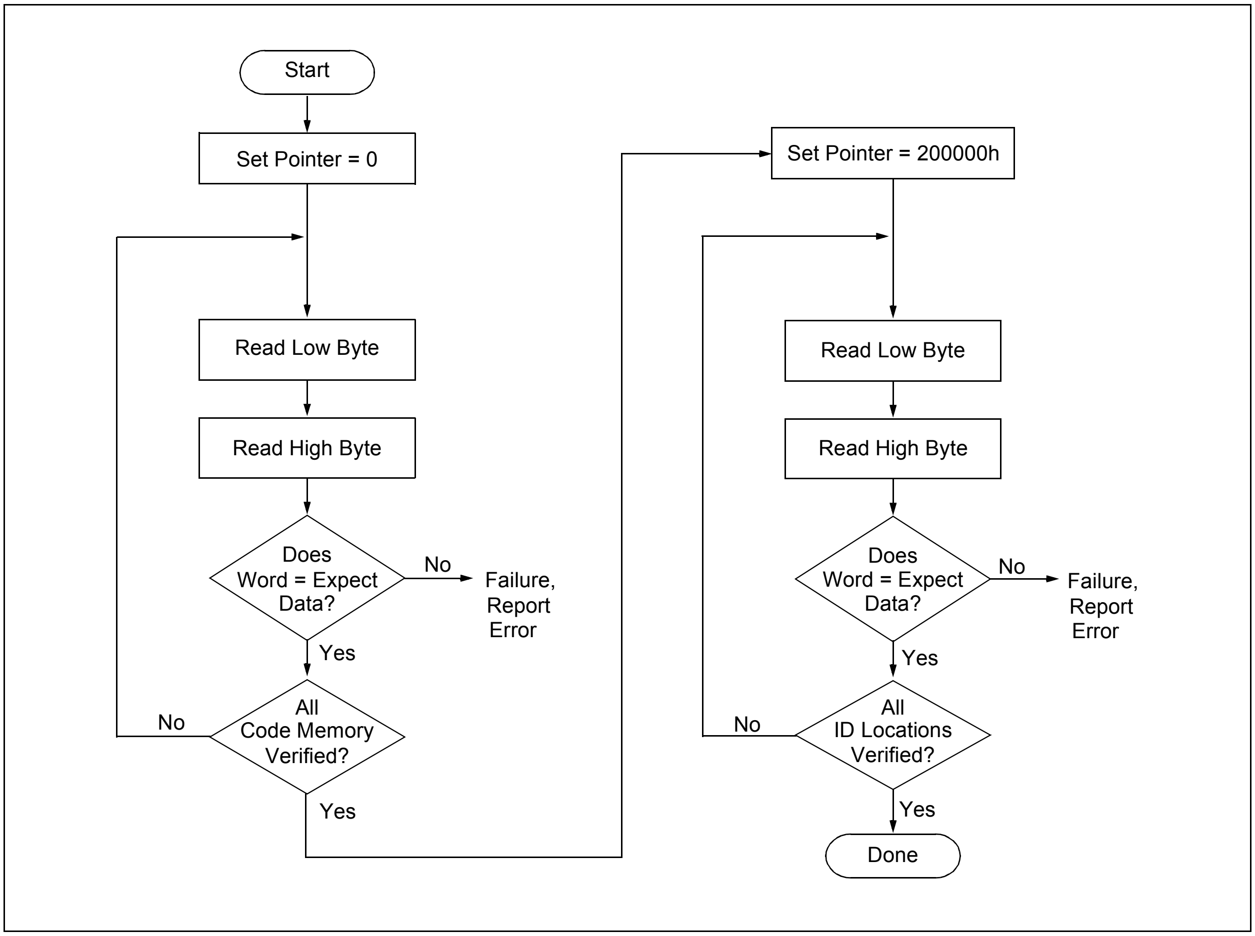
The verify step involves reading back the code memory space and comparing it against the copy held in the programmer's buffer. Memory reads occur a single byte at a time, so two bytes must be read to compare against the word in the programmer's buffer. Refer to **Section 4.1 "Read Code Memory, ID Locations and Configuration Bits"** for implementation details of reading code memory.

The Table Pointer must be manually set to 200000h (base address of the ID locations) once the code memory has been verified. The post-increment feature of the table read 4-bit command may not be used to increment the Table Pointer to 200000h. After setting the Table Pointer to 200000h, the post-increment feature may be used to increment to 200001h, 200002h and so on.

4.3 Verify Configuration Bits

A configuration address may be read and output on PGD via the 4-bit command, `1001`. Configuration data is read and written in a byte-wise fashion, so it is not necessary to merge two bytes into a word prior to a compare. The result may then be immediately compared to the appropriate configuration data in the programmer's memory for verification. Refer to **Section 4.1 "Read Code Memory, ID Locations and Configuration Bits"** for implementation details of reading configuration data.

FIGURE 4-2: VERIFY CODE MEMORY AND ID LOCATIONS FLOW



5.0 CONFIGURATION WORD

The PIC18F8410/8490/8493 family devices have several Configuration Words. These bits can be set or cleared to select various device configurations. All other memory areas should be programmed and verified prior to setting Configuration Words. These bits may be read out normally, even after read or code-protected. Table 5-2 and Table 5-3 provide information on various configuration bits.

5.1 ID Locations

A user may store identification information (ID) in eight ID locations mapped in 200000h:200007h. It is recommended that the Most Significant nibble of each ID be 0Fh. In doing so, if the user code inadvertently tries to execute from the ID space, the ID data will execute as a `NOP`.

5.2 Device ID Word

The device ID word for the PIC18F8410/8490/8493 family is located at 3FFFFEh:3FFFFFh. These bits may be used by the programmer to identify what device type is being programmed and read out normally, even after code or read-protected.

TABLE 5-1 DEVICE ID VALUES

Device	Device ID Value	
	DEVID2	DEVID1
PIC18F6310	0Bh	`111x xxxx`
PIC18F6390	0Bh	`101x xxxx`
PIC18F6393	1Ah	`000x xxxx`
PIC18F8310	0Bh	`110x xxxx`
PIC18F8390	0Bh	`100x xxxx`
PIC18F8393	1Ah	`001x xxxx`
PIC18F6410	06h	`111x xxxx`
PIC18F6490	06h	`101x xxxx`
PIC18F6493	0Eh	`000x xxxx`
PIC18F8410	06h	`110x xxxx`
PIC18F8490	06h	`100x xxxx`
PIC18F8493	0Eh	`001x xxxx`

Note: The ‘`x`’s in DEVID1 contain the device revision code.

TABLE 5-2 PIC18F8410/8490/8493 FAMILY CONFIGURATION BITS AND DEVICE IDS

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300000h	CONFIG1L	—	—	—	—	—	—	—	—	`---- ----`
300001h	CONFIG1H	IESO	FCMEN	—	—	FOSC3	FOSC2	FOSC1	FOSC0	`00-- 0111`
300002h	CONFIG2L	—	—	—	BORV1	BORV0	BOREN1	BOREN0	PWRTEN	`---1 1111`
300003h	CONFIG2H	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	WDTEN	`---1 1111`
300004h(1)	CONFIG3L	WAIT	BW	—	—	—	—	PM1	PM0	`11-- --11`
300005h	CONFIG3H	MCLRE	—	—	—	—	LPT1OSC	—	CCP2MX	`1--- -0-1`
300006h	CONFIG4L	DEBUG	XINST	—	—	—	—	—	STVREN	`10-- ---1`
300008h	CONFIG5L	—	—	—	—	—	—	—	CP	`---- ---1`
300009h	CONFIG5H	—	—	—	—	—	—	—	—	`---- ----`
30000Ah	CONFIG6L	—	—	—	—	—	—	—	—	`---- ----`
30000Bh	CONFIG6H	—	—	—	—	—	—	—	—	`---- ----`
30000Ch	CONFIG7L	—	—	—	—	—	—	—	EBTR	`---- ---1`
30000Dh	CONFIG7H	—	—	—	—	—	—	—	—	`---- ----`
3FFFFEh	DEVID1(2)	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	`1xxx xxxx`
3FFFFFh	DEVID2(2)	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	`0000 xxxx`

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition.
Shaded cells are unimplemented, read as ‘0’.

Note 1: Unimplemented in PIC18F8410/8490/8493 family devices; maintain the default unprogrammed value.

2: DEVIDx registers are read-only and cannot be programmed by the user.

TABLE 5-3 PIC18F8410/8490/8493 FAMILYCONFIGURATION BIT DESCRIPTIONS

Bit Name	Configuration Words	Description
FOSC3:FOSC0	CONFIG1H	Oscillator Selection bits 1111 = External RC oscillator w/ OSC2 configured as 'divide by 4 clock output' 1110 = External RC oscillator w/ OSC2 configured as 'divide by 4 clock output' 1101 = External RC oscillator w/ OSC2 configured as 'divide by 4 clock output' 1100 = External RC oscillator w/ OSC2 configured as 'divide by 4 clock output' 1011 = External RC oscillator w/ OSC2 configured as 'divide by 4 clock output' 1010 = External RC oscillator w/ OSC2 configured as 'divide by 4 clock output' 1001 = Internal RC oscillator w/ OSC2 configured as 'divide by 4 clock output' and OSC1 configured as RA7 1000 = Internal RC oscillator w/ OSC2 and OSC1 configured as RA6 and RA7 0111 = External RC oscillator w/ OSC2 configured as RA6 0110 = HS oscillator w/ PLL enabled 0101 = EC w/ OSC2 configured as RA6 0100 = EC w/ OSC2 configured as 'divide by 4 clock output' 0011 = External RC oscillator w/ OSC2 configured as 'divide by 4 clock output' 0010 = HS oscillator 0001 = XT oscillator 0000 = LP oscillator
FCMEN	CONFIG1H	Fail-Safe Clock Monitor Enable bit 1 = Fail-Safe Clock Monitor enabled 0 = Fail-Safe Clock Monitor disabled
IESO	CONFIG1H	Internal External Switchover Mode Enable bit 1 = Internal External Switchover Mode enabled 0 = Internal External Switchover Mode disabled
$\overline{\text{PWRTEN}}$	CONFIG2L	Power-up Timer Enable bit 1 = PWRT disabled 0 = PWRT enabled
BOREN1:BOREN0	CONFIG2L	Brown-out Reset Enable bit 11 = Brown-out Reset enabled in hardware; RCON<SBOREN> bit disabled 10 = Brown-out Reset enabled only when device is active and disabled in Sleep; RCON<SBOREN> bit disabled 01 = Brown-out Reset is controlled with the RCON<SBOREN> bit setting 00 = Brown-out Reset disabled in hardware; RCON<SBOREN> bit disabled
BORV1:BORV0	CONFIG2L	Brown-out Reset Voltage bits 11 = V_{BOR} set to 2.0V 10 = V_{BOR} set to 2.7V 01 = V_{BOR} set to 4.2V 00 = V_{BOR} set to 4.5V
WDTEN	CONFIG2H	Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled (control is placed on SWDTEN bit)

Note 1: Unimplemented in PIC18F8410/8490/8493 family devices; maintain the default unprogrammed value.

TABLE 5-3 PIC18F8410/8490/8493 FAMILYCONFIGURATION BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
WDTPS3:WDTPS0	CONFIG2H	Watchdog Timer Postscaler Select bits 1111 = 1:32768 1110 = 1:16384 1101 = 1:8192 1100 = 1:4096 1011 = 1:2048 1010 = 1:1024 1001 = 1:512 1000 = 1:256 0111 = 1:128 0110 = 1:64 0101 = 1:32 0100 = 1:16 0011 = 1:8 0010 = 1:4 0001 = 1:2 0000 = 1:1
PM1:PM0(1)	CONFIG3L	Processor Mode Select bits 11 = Microcontroller mode 10 = Microprocessor mode 01 = Microprocessor with Boot Block mode 00 = Extended Microcontroller mode
BW(1)	CONFIG3L	Data Bus Width bit 1 = 16-bit External Bus Width mode 0 = 8-bit External Bus Width mode
WAIT(1)	CONFIG3L	External Bus Data Wait Enable bit 1 = Wait selections unavailable 0 = Wait selections determined by WAIT1:WAIT0 bits of MEMCON register
CCP2MX	CONFIG3H	CCP2 MUX bit 1 = CCP2 input/output is multiplexed with RC1 0 = CCP2 input/output is multiplexed with RE7 in Microcontroller mode; CCP2 input/output is multiplexed with RB3 in Microprocessor mode(1), Extended Microcontroller mode(1) or Microprocessor w/ Boot Block mode(1)
LPT1OSC	CONFIG3H	Low-Power Timer1 Oscillator Enable bit 1 = Timer1 oscillator configured for low-power consumption (lower noise immunity) 0 = Timer1 oscillator configured for higher power consumption (high noise immunity)
MCLRE	CONFIG3H	MCLRE Enable bit 1 = $\overline{\text{MCLR}}$ pin enabled, RG5 disabled 0 = RG5 input pin enabled, $\overline{\text{MCLR}}$ disabled
STVREN	CONFIG4L	Stack Overflow/Underflow Reset Enable bit 1 = Stack Overflow/Underflow will cause Reset 0 = Stack Overflow/Underflow will not cause Reset
XINST	CONFIG4L	Enhanced CPU Enable bit 1 = Enhanced CPU enabled 0 = Enhanced CPU disabled

Note 1: Unimplemented in PIC18F8410/8490/8493 family devices; maintain the default unprogrammed value.

TABLE 5-3 PIC18F8410/8490/8493 FAMILYCONFIGURATION BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
DEBUG	CONFIG4L	Background Debugger Enable bit 1 = Background debugger disabled 0 = Background debugger enabled
CP	CONFIG5L	Code Protection bit (code memory area 0000h-3FFFh for PIC18FX410/X490/X493 devices and 0000h-1FFFh for PIC18FX310/X390/X393 devices) 1 = Code memory not code-protected 0 = Code memory code-protected
EBTR	CONFIG7L	Table Read Protection bit (code memory area 0000h-3FFFh for PIC18FX410/X490/X493 devices and 0000h-1FFFh for PIC18FX310/X390/X393 devices) 1 = Code memory not protected from table reads executed in external memory 0 = Code memory protected from table reads executed in external memory
DEV10:DEV3	DEVID2	Device ID bits These bits are used with the DEV2:DEV0 bits in the DEVID1 register to identify part number.
DEV2:DEV0	DEVID1	Device ID bits These bits are used with the DEV10:DEV3 bits in the DEVID2 register to identify part number.
REV4:REV0	DEVID1	These bits are used to indicate the revision of the device.

Note 1: Unimplemented in PIC18F8410/8490/8493 family devices; maintain the default unprogrammed value.

5.3 Embedding Configuration Word Information in the Hex File

To allow portability of code, a PIC18F8410/8490/8493 family device programmer is required to read the Configuration Word locations from the Hex file. If Configuration Word information is not present in the Hex file, then a simple warning message should be issued. Similarly, while saving a Hex file, all Configuration Word information must be included. An option to not include the Configuration Word information may be provided. When embedding Configuration Word information in the Hex file, it should start at address 300000h.

Microchip Technology Inc. feels strongly that this feature is important for the benefit of the end customer.

5.4 Checksum Computation

The checksum is calculated by summing the following:

- The contents of all code memory locations
- The Configuration Word, appropriately masked
- ID locations

The Least Significant 16 bits of this sum are the checksum.

Table 5-4 describes how to calculate the checksum for each device.

Note:	The checksum calculation differs depending on the code-protect setting. Since the code memory locations read out differently, depending on the code-protect setting, the table describes how to manipulate the actual code memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire code memory can simply be read and summed. The Configuration Word and ID locations can always be read.

TABLE 5-4 CHECKSUM COMPUTATION

Device	Code Protect	Checksum	Blank Value	AAh at 0 and Max Address
PIC18F6310 PIC18F8310 PIC18F6390 PIC18F6393 PIC18F8390 PIC18F8393	None	SUM(0000:1FFF)+(CONFIG1L & 0000)+(CONFIG1H & 00CF)+(CONFIG2L & 001F)+(CONFIG2H & 001F)+(CONFIG3L & 00C3)+(CONFIG3H & 0085)+(CONFIG4L & 00C1)+(CONFIG4H & 0000)+(CONFIG5L & 0001)+(CONFIG5H & 0000)+(CONFIG6L & 0000)+(CONFIG6H & 0000)+(CONFIG7L & 0001)+(CONFIG7H & 0000)	E20C	E162
	All	(CONFIG1L & 0000)+(CONFIG1H & 00CF)+(CONFIG2L & 001F)+(CONFIG2H & 001F)+(CONFIG3L & 00C3)+(CONFIG3H & 0085)+(CONFIG4L & 00C1)+(CONFIG4H & 0000)+(CONFIG5L & 0001)+(CONFIG5H & 0000)+(CONFIG6L & 0000)+(CONFIG6H & 0000)+(CONFIG7L & 0001)+(CONFIG7H & 0000)+SUM(IDs)	0227	0222
PIC18F6410 PIC18F8410 PIC18F6490 PIC18F6493 PIC18F8490 PIC18F8493	None	SUM(0000:3FFF)+(CONFIG1L & 0000)+(CONFIG1H & 00CF)+(CONFIG2L & 001F)+(CONFIG2H & 001F)+(CONFIG3L & 00C3)+(CONFIG3H & 0085)+(CONFIG4L & 00C1)+(CONFIG4H & 0000)+(CONFIG5L & 0001)+(CONFIG5H & 0000)+(CONFIG6L & 0000)+(CONFIG6H & 0000)+(CONFIG7L & 0001)+(CONFIG7H & 0000)	C20C	C162
	All	(CONFIG1L & 0000)+(CONFIG1H & 00CF)+(CONFIG2L & 001F)+(CONFIG2H & 001F)+(CONFIG3L & 00C3)+(CONFIG3H & 0085)+(CONFIG4L & 00C1)+(CONFIG4H & 0000)+(CONFIG5L & 0001)+(CONFIG5H & 0000)+(CONFIG6L & 0000)+(CONFIG6H & 0000)+(CONFIG7L & 0001)+(CONFIG7H & 0000)+SUM(IDs)	0225	0220

Legend:	Item	Description
	CFGW =	Configuration Word
	SUM[a:b] =	Sum of locations, a to b inclusive
	SUM_ID =	Byte-wise sum of lower four bits of all customer ID locations
	+ =	Addition
	& =	Bit-wise AND

6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions Operating Temperature: 25°C is recommended						
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
D110	VIHH	High-Voltage Programming Voltage on $\overline{\text{MCLR}}$/VPP	10	12	V	
D111	VDD	Supply Voltage During Programming	2.00	5.50	V	Normal Programming
			2.9	5.50	V	Chip Erase
D112	IPP	Programming Current on $\overline{\text{MCLR}}$/VPP	—	250	μA	
D113	IDDP	Supply Current During Programming	—	1	mA	
D031	VIL	Input Low Voltage	VSS	0.2 VDD	V	
D041	VIH	Input High Voltage	0.8 VDD	VDD	V	
D080	VOL	Output Low Voltage	—	0.6	V	IOL = 8.5 mA @ 4.5V
D090	VOH	Output High Voltage	VDD – 0.7	—	V	IOH = -3.0 mA @ 4.5V
D012	CIO	Capacitive Loading on I/O pin (PGD)	—	50	pF	To meet AC specifications
P1	TR	$\overline{\text{MCLR}}$/VPP Rise Time to enter Program/Verify mode	—	1.0	μs	(See **Note 1**)
P2	TPGC	Serial Clock (PGC) Period	100	—	ns	VDD = 5.0V
			1	—	μs	VDD = 2.0V
P2A	TPGCL	Serial Clock (PGC) Low Time	40	—	ns	VDD = 5.0V
			400	—	ns	VDD = 2.0V
P2B	TPGCH	Serial Clock (PGC) High Time	40	—	ns	VDD = 5.0V
			400	—	ns	VDD = 2.0V
P3	TSET1	Input Data Setup Time to Serial Clock ↓	15	—	ns	
P4	THLD1	Input Data Hold Time from PGC ↓	15	—	ns	
P5	TDLY1	Delay between 4-bit Command and Command Operand	40	—	ns	
P5A	TDLY1A	Delay between 4-bit Command Operand and next 4-bit Command	40	—	ns	
P6	TDLY2	Delay between Last PGC ↓ of Command Byte to First PGC ↑ of Read of Data Word	200	—	ns	
P9	TDLY5	PGC High Time (minimum programming time)	2	—	ms	
P10	TDLY6	PGC Low Time after Programming (high-voltage discharge time)	120	—	μs	
P11	TDLY7	Delay to allow Self-Timed Data Write or Chip Erase to occur	30	—	ms	
P12	THLD2	Input Data Hold Time from $\overline{\text{MCLR}}$/VPP ↑	2	—	μs	
P13	TSET2	VDD ↑ Setup Time to $\overline{\text{MCLR}}$/VPP ↑	100	—	ns	
P14	TVALID	Data Out Valid from PGC ↑	10	—	ns	

Note 1: Do not allow excess time when transitioning $\overline{\text{MCLR}}$ between VIL and VIHH; this can cause spurious program executions to occur. The maximum transition time is:
1 TCY + TPWRT (if enabled) + 1024 TOSC (for LP, HS, HS/PLL and XT modes only)
+2 ms (for HS/PLL mode only) + 1.5 μs (for EC mode only)
where TCY is the Instruction Cycle Time, TPWRT is the Power-up Timer Period and TOSC is the Oscillator Period.

For specific values, refer to the Electrical Characteristics section of the Device Data Sheet for the particular device.

NOTES:

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