FEATURES

- 5-phase & 8-phase dual output PWM Controller with phases flexibly assigned between Loops 1 & 2
- Dynamic voltage control by 2-bit parallel interface with Gamer Mode override and Vmax setting
- Input Voltage Management for up to 3 Input Voltages
- ICRITICAL Monitor and Phase Current Capture Mode
- Phase Switching frequency from 200kHz to 1.2MHz
- IR Efficiency Shaping Features including Variable Gate Drive, Dynamic Phase Control
- Programmable 1-phase or 2-phase for Light Loads and Active Diode Emulation for Very Light Loads
- IR Adaptive Transient Algorithm (ATA) minimizes output bulk capacitors and system cost
- Per-Loop Fault Protection: OVP, UVP, OCP, OTP
- I2C/SMBus/PMBus system interface for telemetry of Temperature, Voltage, Current & Power for both loops
- Non-Volatile Memory (NVM) for custom configuration
- Compatible with IR ATL and 3.3V tri-state Drivers
- +3.3V supply voltage; 0ºC to 85ºC ambient operation
- Pb-Free, RoHS, 6x6 40-pin & 8x8 56-pin QFN, MSL2 package

APPLICATIONS

- Multiphase GPU systems

DESCRIPTION

The CHL8225G/8G are dual-loop, digital multi-phase buck controllers. The CHL8225G drives up to 5 phases and the CHL8228G drives up to 8 phases. They feature Input Voltage Management allowing up to 3 input voltages to be monitored to ensure adequate power is delivered to the load. Dynamic voltage control is provided by 4 registers which are programmed through I2C/SMBus/PMBus and then selected using a 2-bit parallel bus for fast access.

The CHL8225G/8G includes the IR Efficiency Shaping Technology to deliver exceptional efficiency at minimum cost across the entire load range. IR Variable Gate Drive optimizes the MOSFET gate drive voltage as a function of real-time load current. IR Dynamic Phase Control adds and drops phases based upon load current. The CHL8225G/8G can be configured to enter 1-phase operation and active diode emulation based upon load current or by command.

IR's unique Adaptive Transient Algorithm (ATA), based on proprietary non-linear digital PWM algorithms, minimizes output bulk capacitors.

The I2C/PMBus interface can communicate with up to 16 CHL8225G/8G-based VR loops. Device configuration and fault parameters are defined using the IR Digital Power Design Center (DPDC) GUI and stored in on-chip NVM.

The CHL8225G/8G provides extensive OVP, UVP, OCP and OTP fault protection and includes thermistor based temperature sensing with VRHOT signal. The CHL8225G/8G includes numerous features like register diagnostics for fast design cycles and platform differentiation, simplifying VRD design and enabling fastest time-to-market with its "set-and-forget" methodology.

PIN DIAGRAM

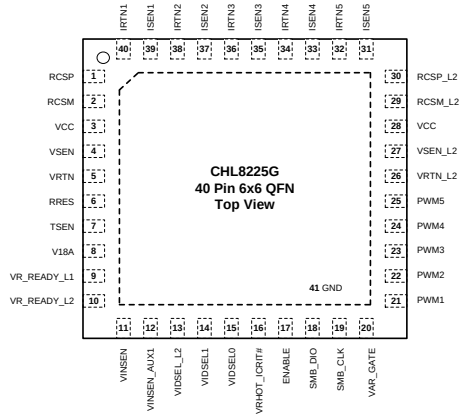


Figure 1: CHL8225G Package Top View

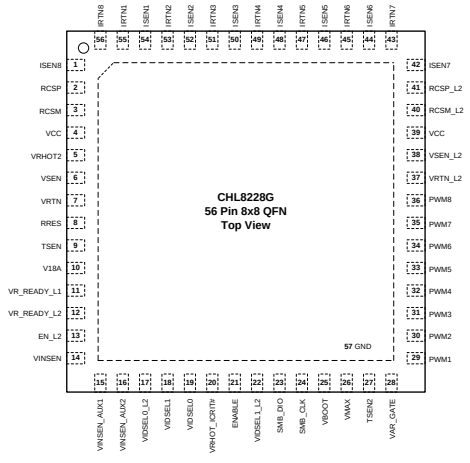
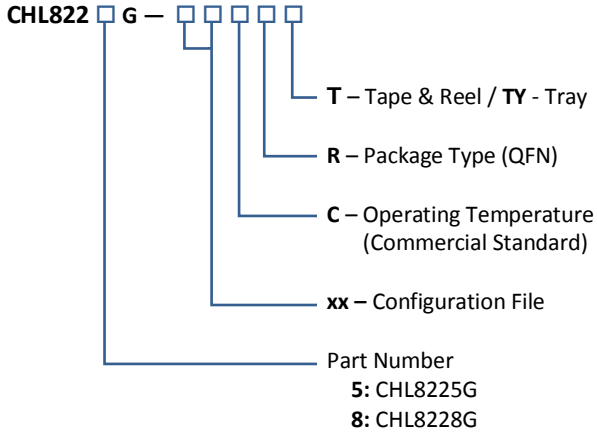


Figure 2: CHL8228G Package Top View

ORDERING INFORMATION



Package	Packing Qty	Part Number
QFN	T=3000 TY=4900	CHL8225G-00CRT CHL8225G-00CRTY
QFN	T=3000	CHL8225G-xxCRT[1]
QFN	T=3000 TY=2600	CHL8228G-00CRT CHL8228G-00CRTY
QFN	T=3000	CHL8228G-xxCRT[1]

Notes:

1. "xx" indicates customer specific configuration file.

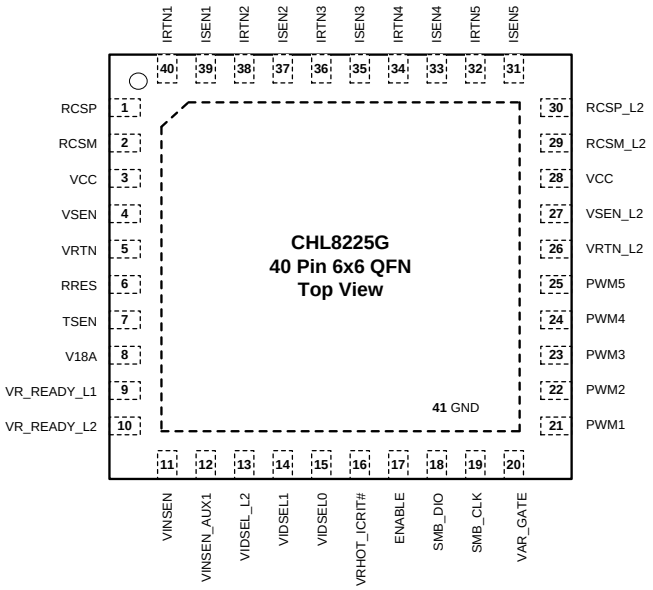


Figure 3: CHL8225G Top View Enlarged

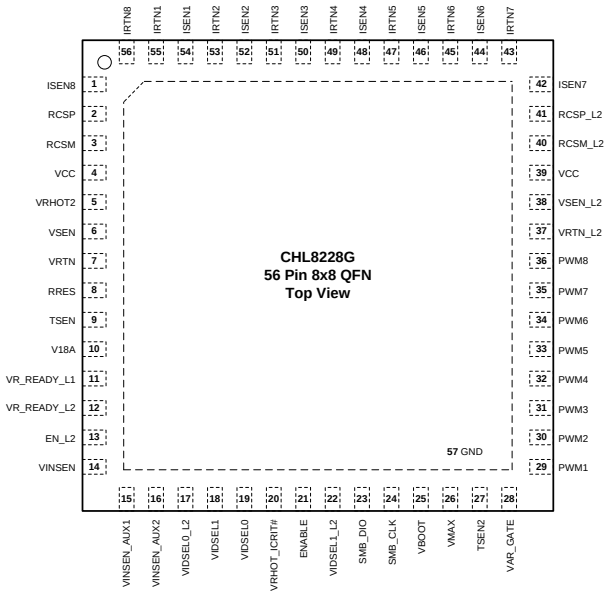


Figure 4: CHL8228G Top View Enlarged

FUNCTIONAL BLOCK DIAGRAM

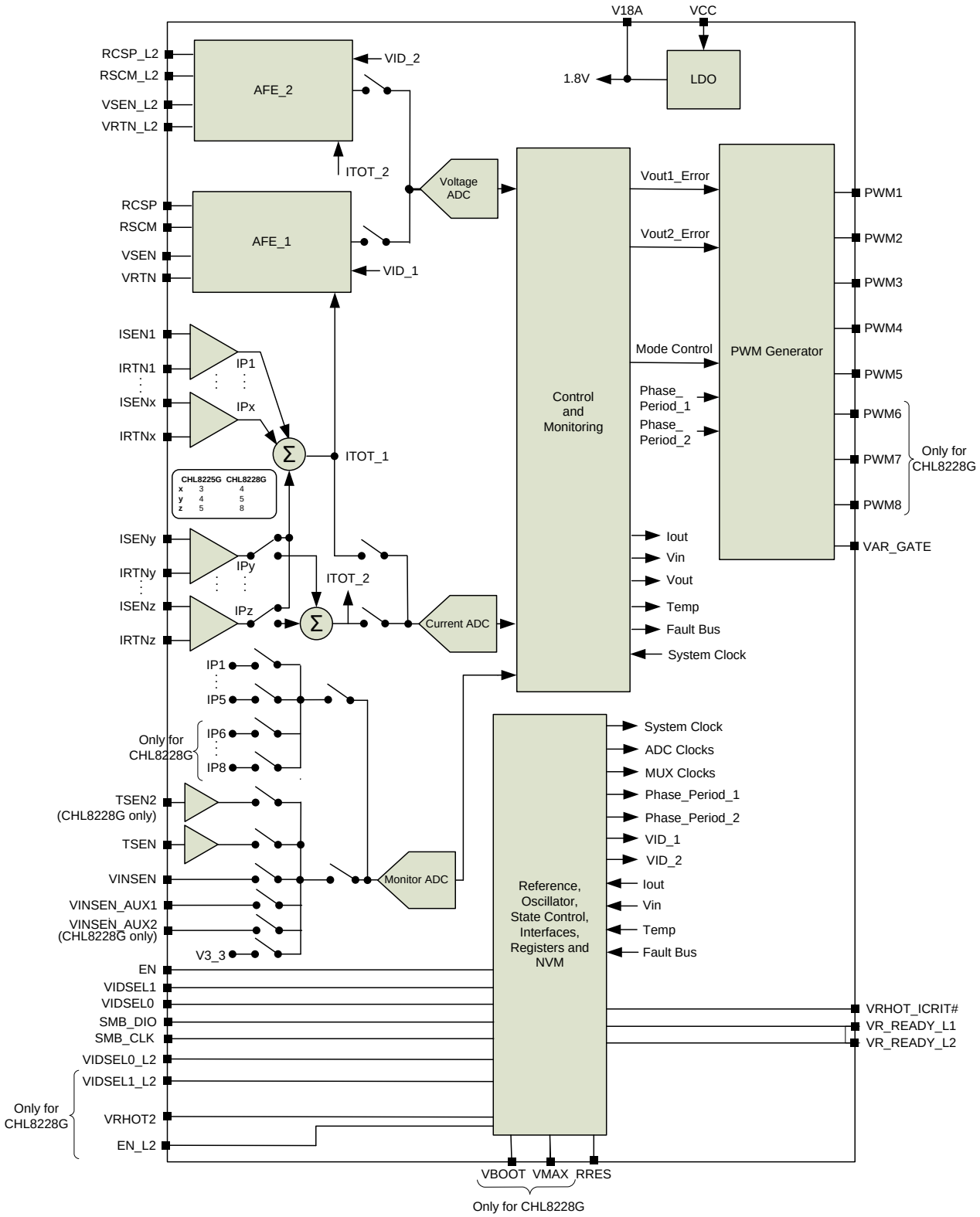


Figure 5: CHL8225G & CHL8228G Functional Block Diagram