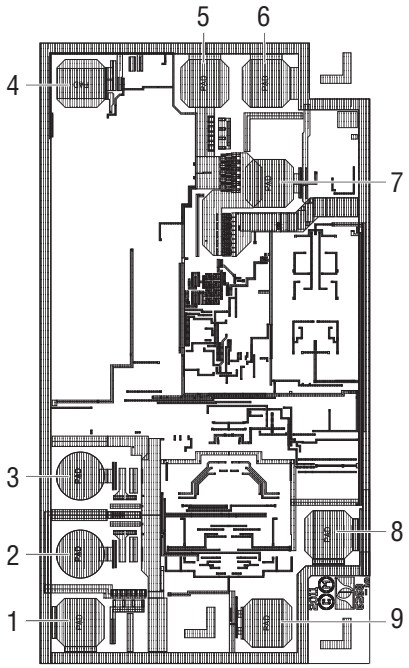
DICE/DWF SPECIFICATION

LTC6268-10
4GHz Ultra-Low Bias Current FET Input Op Amp



PAD FUNCTION

1. V^-
2. +IN
3. –IN
4. $\overline{SHDN}$
5. V^+
6. V^+
7. OUT
8. V^-
9. $\overline{SHDN}$

50mils × 29mils,
28mils thick.
Backside metal: None
Backside potential: V^-

DIE CROSS REFERENCE

LTC® Finished Part Number	Order Part Number
LTC®6268-10	LTC6268-10 DICE/DWF

Please refer to LTC standard product data sheet for other applicable product information.
***DWF = DICE in wafer form.**

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ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage V^+ to V^- 5.5V
Input Voltage .....V^- – 0.2V to V^+ + 0.2V
Input Current (+IN, –IN) (Note 2).....±1mA
Input Current ($\overline{SHDN}$) .....±1mA
Output Current (I_{OUT}) (Note 4, 5).....135mA

DICE/DWF ELECTRICAL TEST LIMITS

Specifications are at T_A = 25°C, V_{SUPPLY} = 5.0V (V^+ = 5V, V^- = 0V, V_{CM} = mid-supply), R_L = 1kΩ, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 2.75V	–0.7	0.7	mV
		V_{CM} = 4.0V	–1.0	1.0	mV
I_B	Input Bias Current (Notes 3, 4)	V_{CM} = 2.75V	–20	20	fA
		V_{CM} = 4.0V	–20	20	fA
I_{OS}	Input Offset Current (Notes 3, 4)	V_{CM} = 2.75V	–40	40	fA
CMRR	Common Mode Rejection Ratio	V_{CM} = 0.5V to 3.2V (PNP Side)	72		dB
		V_{CM} = –0.1V to 4.5V	64		dB
IVR	Input Voltage Range	Guaranteed by CMRR	–0.1	4.5	V
PSRR	Power Supply Rejection Ratio	V_{CM} = 1.0V, V_{SUPPLY} Ranges from 3.1V to 5.25V	78		dB
	Supply Voltage Range		3.1	5.25	

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DICE/DWF ELECTRICAL TEST LIMITS

Specifications are at T_A = 25°C, V_{SUPPLY} = 5.0V (V^+ = 5V, V^- = 0V, V_{CM} = mid-supply), R_L = 1kΩ, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS			MIN	MAX	UNITS
A_V	Open Loop Voltage Gain	V_{OUT} = 0.5V to 4.5V	R_{LOAD} = 10k		125		V/mV
			R_{LOAD} = 100		10		V/mV
I_{SC}	Output Short Circuit Current (Note 5)				60		mA
I_S	Supply Current Per Amplifier				15	18	mA
	Supply Current in Shutdown (Per Amplifier)					0.85	mA
$I_{\overline{SHDN}}$	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 0.75V $V_{\overline{SHDN}}$ =1.50V			–12 –12	12 12	µA µA
V_{IL}	$\overline{SHDN}$ Input Low Voltage	Disable				0.75	V
V_{IH}	$\overline{SHDN}$ Input High Voltage	Enable. If $\overline{SHDN}$ is Unconnected, Amp is Enabled			1.5		V
I_{LEAK}	Output Leakage Current in Shutdown	$V_{\overline{SHDN}}$ = 0V, V_{OUT} = 0V $V_{\overline{SHDN}}$ = 0V, V_{OUT} = 5V				400 400	nA nA

DICE/DWF ELECTRICAL TEST LIMITS

Specifications are at T_A = 25°C, V_{SUPPLY} = 3.3V (V^+ = 3.3V, V^- = 0V, V_{CM} = mid-supply), R_L = 1kΩ, $V_{\overline{SHDN}}$ is unconnected.

SYMBOL	PARAMETER	CONDITIONS			MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = 1.0V			–0.7	0.7	mV
		V_{CM} = 2.3V			–1.0	1.0	mV
I_B	Input Bias Current (Notes 3, 4)	V_{CM} = 1.0V			–20	20	fA
		V_{CM} = 2.3V			–20	20	fA
I_{OS}	Input Offset Current (Notes 3, 4)	V_{CM} = 1.0V			–40	40	fA
CMRR	Common Mode Rejection Ratio	V_{CM} = 0.5V to 1.2V (PNP Side)			63		dB
		V_{CM} = –0.1V to 2.8V (Full Range)			60		dB
IVR	Input Voltage Range	Guaranteed by CMRR			–0.1	2.8	V
A_V	Open Loop Voltage Gain	V_{OUT} = 0.5V to 2.8V	R_{LOAD} = 10k		80		V/mV
			R_{LOAD} = 100		10		V/mV
I_{SC}	Output Short Circuit Current (Note 5)				50		mA
I_S	Supply Current per Amplifier				14.5	17.5	mA
	Supply Current in Shutdown (Per Amplifier)					0.6	mA
$I_{\overline{SHDN}}$	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 0.75V $V_{\overline{SHDN}}$ = 1.5V			–12 –12	12 12	µA µA
V_{IL}	$\overline{SHDN}$ Input Low Voltage	Disable				0.75	V
V_{IH}	$\overline{SHDN}$ Input High Voltage	Enable. If $\overline{SHDN}$ is Unconnected, Amp Is Enabled			1.5		V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by two series connected ESD protection diodes to each power supply. The input current should be limited to less than 1mA. The input voltage should not exceed 200mV beyond the power supply.

Note 3: The input bias current is the average of the currents into the positive and negative input pins.

Note 4: This parameter is specified by design and/or characterization and is not tested in production.

Note 5: The LTC6268-10 is capable of producing peak output currents in excess of 135mA. Current density limitations within the IC require the continuous current supplied by the output (sourcing or sinking) over the operating lifetime of the part be limited to under 135mA (Absolute Maximum).

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

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