Reference Manual

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SPX-4

Four-channel Analog Output
Serial Peripheral Expansion
(SPX™) Board

VERSA**L**OGIC
C O R P O R A T I O N

VERSALOGIC CORPORATION

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MSPX4

Product Release Notes

Rev. 1
- Production release.

Support Page

The SPX support page, at **http://www.versalogic.com/private/SPX4support.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Data sheets and manufacturers' links for chips used in this product
- Utility routines and benchmark software

This is a private page for SPX users that can be accessed only be entering this address directly. It cannot be reached from the VersaLogic homepage.

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Introduction

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Description

The VersaLogic SPX-4 is a 4-channel analog output expansion module designed to be used with any SPX™ enabled base board. Its features include:

- Texas Instruments DAC7554 digital-to-analog converter
- Four analog output channels
- 12-bit resolution

- Compatible with any SPX enabled base board
- Maximum 5 µs settling time
- 0V to +4.095V range

VersaLogic SPX boards are a line of I/O expansion boards using the industry standard Serial Peripheral Interface (SPI) bus. These are small 1.2" x 3.775" boards that can mounted on the PC/104 and PC/104-*Plus* stack using normal standoffs. They can also mount up to two feet away from the base board using custom cabling.

SPX boards are electrically connected to a base board via a 14-pin 2 mm cable. Up to four boards can be daisy-chained together. The SPI bus requires each chip to have a discrete chip-select signal, and the 14-pin interface supplies four chip-select signals. The maximum clock rate is 8 MHz.

Power for SPX boards is supplied through the interface cable. I/O connections on SPX boards are provided through screw terminal/wire connections.

All SPX boards are RoHS compliant and industrial temperature rated.

ABOUT SPI

The SPI bus specifies four logic signals: SCLK – Serial clock (output from master); MOSI – Master output, slave input (output from master); MISO – Master input, slave output (output from slave); and SS – Slave select (output from master).

The SPI implementation on VersaLogic CPU boards adds additional features, such as hardware interrupt input to the master. The master initiates all SPI transactions. A slave device responds when its slave select is asserted and it receives clock pulses from the master.

Slave selects are controlled in one of two modes: manual or automatic. In automatic mode, the slave select is asserted by the SPI controller when the most significant data byte is written. This initiates a transaction to the specified slave device. In manual mode, the slave select is controlled by the user and any number of data frames can be sent. The user must command the slave select high to complete the transaction.

The SPI clock rate can be software configured to operate at speeds between 1 MHz and 8 MHz. All four common SPI modes are supported through the use of clock polarity and clock phase controls.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size: 1.2" x 3.775"; SPX compliant
Storage Temperature: -40° C to 85° C
Free Air Operating Temperature:
    -40° C to +85° C
Power Requirements:
    +5.0V ± 5% @ 15.36 mA (76.8 mW) with
    10 mA load typ., 65.5 mA (327.4 mW) max.
    (Interface cable provides 500 mA total, to be
    shared by all SPX modules)
Analog Output:
    4-channel, 12-bit
    Output range: unipolar, 0V to +4.095V
    5 µs max settling time
    Slew rate: 1V/µs
Compatibility:
    SPX – Full compliance
    (Any 3.3V signaling SPI interface, 8 MHz
    maximum clock)
Weight:
    0.030 lbs (0.014 kg)
Compliance:
    RoHS – Full compliance

Specifications are subject to change without notice.

RoHS-Compliance

The SPX-4 is RoHS-compliant.

ABOUT RoHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corporation is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Warnings

ELECTROSTATIC DISCHARGE

Electrostatic discharge (ESD) can damage boards, disk drives, and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Technical Support

If you are unable to solve a problem with this manual please visit the SPX Product Support web page listed below. If you have further questions, contact VersaLogic technical support at (503) 747-2261. VersaLogic technical support engineers are also available via e-mail at Support@VersaLogic.com.

SPX Support Website

http://www.versalogic.com/private/SPX4support.asp

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (503) 747-2261. VersaLogic's standard turn-around time for repairs is five working days after the product is received.

Please provide the following information:

- Your name, the name of your company and your phone number
- The name of a technician or engineer that can be contact if any questions arise.
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair   All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair   All non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note   Please mark the RMA number clearly on the outside of the box before returning. Failure to do so can delay the processing of your return.

SPX-4 Board Layout

The figure below shows the dimensions of the SPX-4 board, as well as the location of connectors, jumpers, and mounting holes.
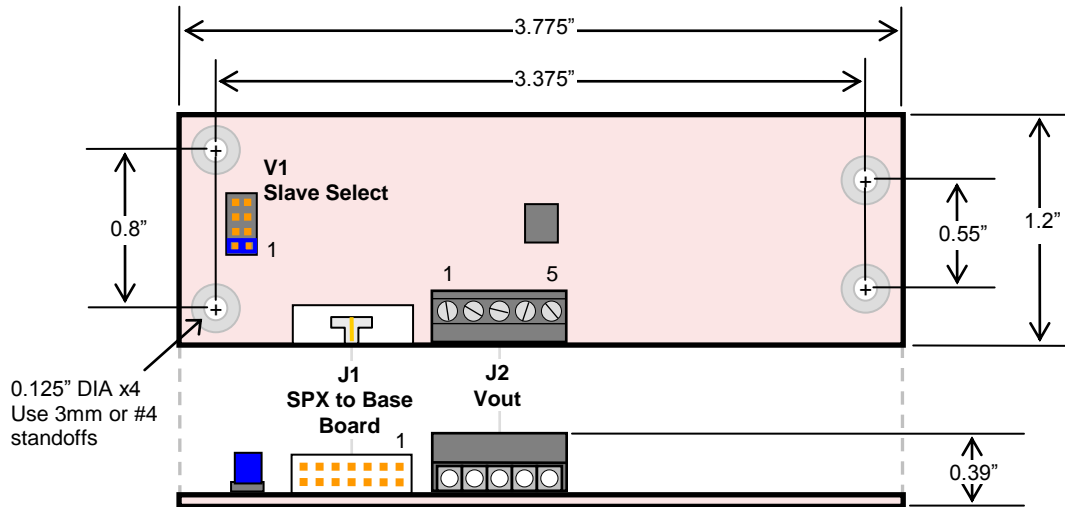

Figure 1. SPX-4 Board Layout
(Not to scale. All dimensions in inches.)

HARDWARE ASSEMBLY

The SPX-4 mounts on two hardware standoffs using the corner mounting holes. These standoffs are secured to the board, typically across the PC/104 and PC/104-*Plus* stack locations, using pan head screws, shown in Figure 2.

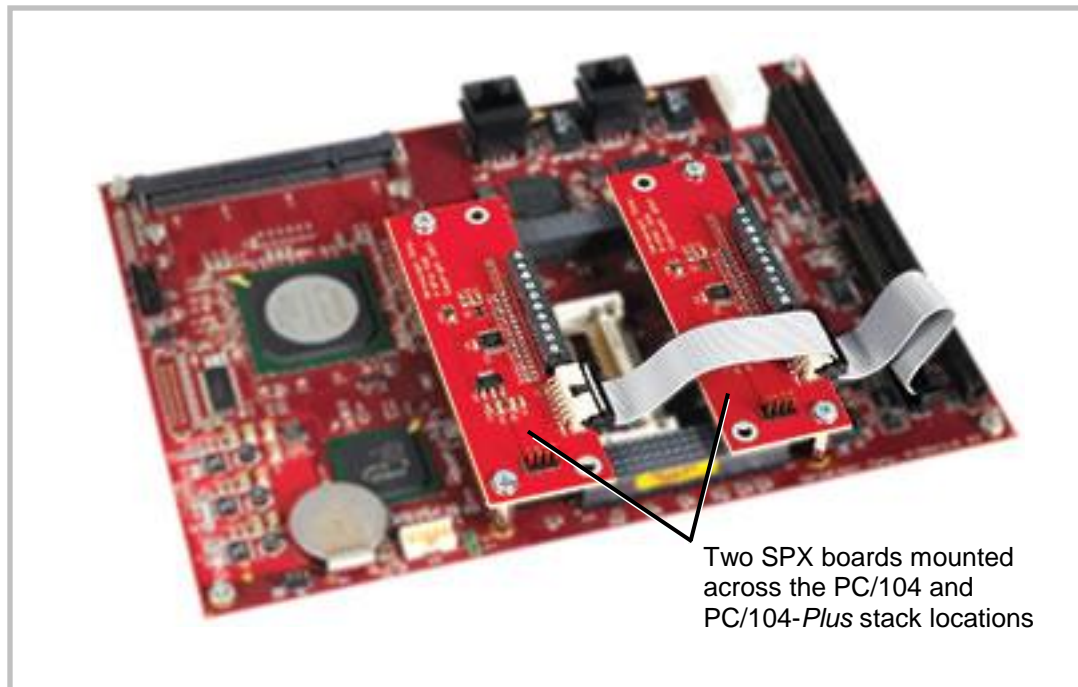Standoffs and screws are available as part number VL-HDW-101.

Two SPX boards mounted across the PC/104 and PC/104-*Plus* stack locations

Figure 2. SPX Board Mounting

Connector Functions and Interface Cables

The following table shows the function of each connector, as well as mating connectors and cables.

Table 1: Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description
J1	SPX to Base Board	FCI 89361-714LF or equivalent	CBR-1401 CBR-1402	2 SPX Module Cable 4 SPX Module Cable
J2	Analog Output	Bare wires to 5-pin screw terminal	–	16-28 AWG wire

Jumper Summary

Table 2: Jumper Summary

Jumper Block	Description	As Shipped
V1[1-2]	Slave Select 0	In
V1[3-4]	Slave Select 1	Out
V1[5-6]	Slave Select 2	Out
V1[7-8]	Slave Select 3	Out

J1 Connector Pinout

Table 3: J1 Connector Pinout

Pin	Signal Name	Description
1	V5_0	+5.0V
2	SCLK	Serial Clock
3	GND	Ground
4	MISO	Master In Slave Out
5	GND	Ground
6	MOSI	Master Out Slave In
7	GND	Ground
8	SS0#	Slave Select 0
9	SS1#	Slave Select 1
10	SS2#	Slave Select 2
11	SS3#	Slave Select 3
12	GND	Ground
13	SINT#	SPI Interrupt
14	V5_0	+5.0V

Analog Output 3

Description

The SPX-4 provides a 12-bit, four-channel, unipolar, digital-to-analog converter (DAC). Each DAC channel has two registers: an input register and a DAC register, as shown in Figure 3. The input register is a buffer, and the DAC register is the actual data output register. You can update the input and DAC registers separately or together. And you can update a single channel or all four channels at once. The SPX-4 communicates with the base board through the SPX interface.
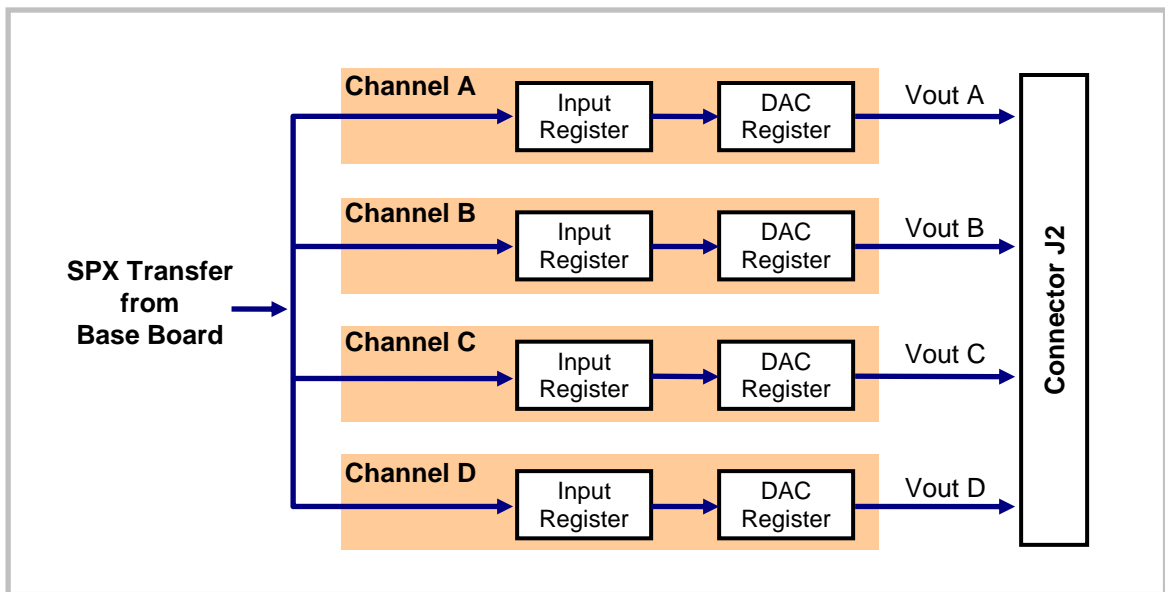

Figure 3. SPX-4 Digital-to-Analog Converter

The SPX-4 DAC is implemented using the Texas Instruments (TI) DAC7554 chip. For detailed information on this chip, refer to the DAC7554 Data Sheet.

EXTERNAL CONNECTIONS

Analog outputs are transmitted through connector J2 of the SPX-4 as shown in the following table.

Table 4: Analog Output Connectors

J2 Pin	Signal Name	Description
1	VoutA	Voltage Output A
2	VoutB	Voltage Output B
3	VoutC	Voltage Output C
4	VoutD	Voltage Output D
5	Ground	Ground

WRITING TO AN ANALOG OUTPUT CHANNEL

Analog outputs are sent from the base board to the SPX-4 using the base board's SPX interface. Each output consists of a 16-bit DAC word, divided into a 12-bit data word and a 4-bit control word. The 12-bit data word specifies the output voltage, and the 4-bit control word determines the channel or channels to which the output voltage is sent, as well as whether the input register, DAC register, or both, are being acted upon.

The VersaLogic SPI implementation (SPX interface), employs four 8-bit data registers, SPIDATA0-3. Only two of these registers (SPIDATA2-3) are used to send the 16-bit DAC word to the SPX-4. Writing the MSB to the SPIDATA3 register triggers the SPI transaction (that is, causes the output voltage DAC word to be transmitted).

Table 5 shows the relationship of the base board's SPI data registers and the 16-bit DAC word. See Appendix A for more information about base board registers.

Table 5: Base Board SPI Data Registers and the 16-bit DAC Word

Base Board SPI Data Registers															
SPIDATA3								SPIDATA2							
MSbit							LSbit	MSbit							LSbit

16-bit DAC Word															
4-bit Control Word				12-bit Data Word											
Function		Ch. Select		Data MSB				Data LSB							
LD1	LD0	Sel1	Sel0	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Data Word

The 12-bit data word spans the two SPI data registers, with the LSB written to SPIDATA2 and the MSB written to SPIDATA3.

The data word is binary with all zeroes corresponding to 0V output and all ones corresponding to full-scale output (+4.095V). Each LSbit step equals 1 mV.

The TI DAC7554 data sheet refers to these bits as DB0 through DB11.

Control Word

The control word is written to the four most significant bits of the SPIDATA3 register. In automatic slave select mode, the DAC transaction executes when the MSB is written.

The control word is divided into a channel select (SPIDATA3 bits 4 and 5) and a function (SPIDATA3 bits 6 and 7).

The TI DAC7554 data sheet refers to the channel select bits as Sel0 and Sel1, and the function bits as LD0 and LD1. Table 6 shows the channel select bit settings.

Table 6: Channel Select Bit Settings

Sel1	Sel0	Channel Select
0	0	Channel A
0	1	Channel B
1	0	Channel C
1	1	Channel D

Note: The function of the channel select bits changes when the LD0 and LD1 bits are set to 11b. See Table 8 for details.

Table 7 shows the function bit settings.

Table 7: Function Bit Settings

LD1	LD0	Function
0	0	Single channel store. The selected input register is updated.
0	1	Single channel DAC update. The selected DAC register is updated with input register information.
1	0	Single channel update. The selected input and DAC register is updated.
1	1	Depends on the Sel1 and Sel0 bits. See Table 8.

DAC Word Functions

Table 8 lists all possible 16-bit DAC words and their functions.

Table 8: 16-bit DAC Words

Control				Data	DAC Ch.	Function
LD1	LD0	Sel1	Sel0	DB11-DB0		
0	0	0	0	data	A	Input register updated
0	0	0	1	data	B	Input register updated
0	0	1	0	data	C	Input register updated
0	0	1	1	data	D	Input register updated
0	1	0	0	data	A	DAC register updated, output updated
0	1	0	1	data	B	DAC register updated, output updated
0	1	1	0	data	C	DAC register updated, output updated
0	1	1	1	data	D	DAC register updated, output updated
1	0	0	0	data	A	Input register and DAC register updated, output updated
1	0	0	1	data	B	Input register and DAC register updated, output updated
1	0	1	0	data	C	Input register and DAC register updated, output updated
1	0	1	1	data	D	Input register and DAC register updated, output updated
1	1	0	0	data	A-D	Input register updated
1	1	0	1	data	A-D	DAC register updated, output updated
1	1	1	0	data	A-D	Input register and DAC register updated, output updated
1	1	1	1	data	–	Power down. (See DAC7554 Data Sheet.)

CALIBRATION

There are no calibration adjustments. Calibration, if desired, is accomplished by mathematical transformation in software.

Initiating an Analog Voltage Output

The following procedure can be used to initiate an analog voltage output to the SPX-4.

1. Write D1h to the SPICONTROL register (I/O address 1D8h) – This value configures the SPI port to select external slave select 0 (SPX-4 default jumper setting), 16-bit frame length, SCLK high idle state, falling SCLK edge for the active edge, and automatic slave select.

2. Write 30h to the SPISTATUS register (I/O address 1D9h) – This value selects 8 MHz SCLK speed, hardware IRQ disable, and left-shift data.

3. Write the lower eight (least significant) bits of the analog output data word to SPIDATA2 (1DCh).

4. Combine the 4-bit control word (upper half of register) along with the four most significant bits of the analog output data (lower half of register) and write to SPIDATA3 (1DDh). Any write operation to SPIDATA3 will trigger an SPI transaction.

5. Poll the BUSY bit until the conversion is completed.

6. If a control word updating the DAC register or both the input and DAC registers was sent, the corresponding output channel(s) on the SPX-4 should have the voltage:

   Vout = [data word in decimal] mV

Analog Output Code Example

This code configures the base board's SPX registers to update the input and DAC registers of all four channels (A-D) and output the voltage data word, 0xAAA (2730d), equivalent voltage. This code example causes the output voltage on J2 pins 1-4 (with respect to ground, J2 pin 5) to change from 0V to 2.730V. You can change the data word to see the corresponding voltage change using the relationship: Vout = [data word in decimal] mV.

```
      ; Set up SPI configuration registers.
      MOV   DX, 0x1D8
      MOV   AL, 0xD1    ;SPICONTROL: SS0#, 16-bit frame, high idle,
                        ;falling edge, automatic slave select
      OUT   DX, AL      ;Set up SPICONTROL for analog output
      MOV   DX, 0x1D9
      MOV   AL, 0x30    ;SPISTATUS: 8 MHz, no IRQ, left-shift data
      OUT   DX, AL

      ; Output analog value.
      MOV   DX, 0x1DC
      MOV   AL, 0xAA    ; SPIDATA2: lower 8 bits of 12-bit data
      OUT   DX, AL
      MOV   DX, 0x1DD
      MOV   AL, 0xEA    ; SPIDATA3: update all input and DAC registers
      OUT   DX, AL
      ;
```

For more detailed information on the SPX-4 digital-to-analog converter, refer to the Texas Instruments DAC7554 Data Sheet.

Base Board SPI Registers

A

The following tables describe the SPI control and data registers of the EBX-11 Rev. 6.00 and later. This is the standard set of SPI registers for VersaLogic CPU boards with an SPX interface. See the appropriate base-board reference manual for details and updates.

SPICONTROL (READ/WRITE) 1D8h

D7	D6	D5	D4	D3	D2	D1	D0
CPOL	CPHA	SPILEN1	SPILEN0	MAN_SS	SS2	SS1	SS0

Table 9: SPI Control Register 1 Bit Assignments

Bit	Mnemonic	Description
D7	CPOL	**SPI Clock Polarity –** Sets the SCLK idle state. 0 = SCLK idles low 1 = SCLK idles high
D6	CPHA	**SPI Clock Phase –** Sets the SCLK edge on which valid data will be read. 0 = Data read on rising edge 1 = Data read on falling edge
D5-D4	SPILEN	**SPI Frame Length –** Sets the SPI frame length. This selection works in manual and auto slave select modes. SPILEN1 SPILEN0 Frame Length 0 0 8-bit 0 1 16-bit 1 0 24-bit 1 1 32-bit
D3	MAN_SS	**SPI Manual Slave Select Mode –** This bit determines whether the slave select lines are controlled through the user software or are automatically controlled by a write operation to SPIDATA3 (1DDh). If MAN_SS = 0, then the slave select operates automatically; if MAN_SS = 1, then the slave select line is controlled manually through SPICONTROL bits SS2, SS1, and SS0. 0 = Automatic, default 1 = Manual
D2-D0	SS	**SPI Slave Select –** These bits select which slave select will be asserted. The SSx# pin on the base board will be directly controlled by these bits when MAN_SS = 1. SS2 SS1 SS0 Slave Select 0 0 0 None, port disabled 0 0 1 SPX Slave Select 0, J17 pin-8 0 1 0 SPX Slave Select 1, J17 pin-9 0 1 1 SPX Slave Select 2, J17 pin-10 1 0 0 SPX Slave Select 3, J17 pin-11 1 0 1 On-Board A/D Converter Slave Select 1 1 0 On-Board Digital I/O Ch 0-Ch 15 Slave Select 1 1 1 On-Board Digital I/O Ch 16-Ch 31 Slave Select

SPISTATUS (READ/WRITE) 1D9h

D7	D6	D5	D4	D3	D2	D1	D0
IRQSEL1	IRQSEL0	SPICLK1	SPICLK0	HW_IRQ_EN	LSBIT_1ST	HW_INT	BUSY

Table 10: SPI Control Register 2 Bit assignments

Bit	Mnemonic	Description
D7-D6	IRQSEL	**IRQ Select** – These bits select which IRQ will be asserted when a hardware interrupt from a connected SPI device occurs. The HW_IRQ_EN bit must be set to enable SPI IRQ functionality. **IRQSEL1 IRQSEL0 IRQ** 0 0 IRQ3 0 1 IRQ4 1 0 IRQ5 1 1 IRQ10 **Note:** The on-board digital I/O chips must be configured for open-drain and mirrored interrupts in order for any SPI device to use hardware interrupts.
D5-D4	SPICLK	**SPI SCLK Frequency –** These bits set the SPI clock frequency. **SPICLK1 SPICLK0 Frequency** 0 0 1.042 MHz 0 1 2.083 MHz 1 0 4.167 MHz 1 1 8.333 MHz
D3	HW_IRQ_EN	**Hardware IRQ Enable** – Enables or disables the use of the selected IRQ (IRQSEL) by an SPI device. 0 = SPI IRQ disabled, default 1 = SPI IRQ enabled **Note:** The selected IRQ is shared with PC/104 ISA bus devices. CMOS settings must be configured for the desired ISA IRQ.
D2	LSBIT_1ST	**SPI Shift Direction** – Controls the SPI shift direction of the SPIDATA registers. The direction can be shifted toward the least significant bit or the most significant bit. 0 = SPIDATA data is left-shifted (MSbit first), default 1 = SPIDATA data is right-shifted (LSbit first)
D1	HW_INT	**SPI Device Interrupt State –** This bit is a status flag that indicates when the hardware SPX signal SINT# is asserted. 0 = Hardware interrupt on SINT# is deasserted 1 = Interrupt is present on SINT# This bit is read-only and is cleared when the SPI device's interrupt is cleared.
D0	BUSY	**SPI Busy Flag** – This bit is a status flag that indicates when an SPI transaction is underway. 0 = SPI bus idle 1 = SCLK is clocking data in and out of the SPIDATA registers This bit is read-only.

SPI DATA REGISTERS

SPIDATA0 (READ/WRITE) 1DAh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA1 (READ/WRITE) 1DBh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA2 (READ/WRITE) 1DCh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 (READ/WRITE) 1DDh

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 contains the most significant byte (MSB) of the SPI data word. A write to this register will initiate the SPI clock and, if the MAN_SS bit = 0, will also assert a slave select to begin an SPI bus transaction. Increasing frame sizes from 8-bit use the lowest address for the least significant byte of the SPI data word; for example, the LSB of a 24-bit frame would be SPIDATA1. Data is sent according to the LSBIT_1ST setting. When LSBIT_1ST = 0, the MSbit of SPIDATA3 is sent first, and received data will be shifted into the LSbit of the selected frame size set in the SPILEN field. When LSBIT_1ST = 1, the LSbit of the selected frame size is sent first, and the received data will be shifted into the MSbit of SPIDATA3.