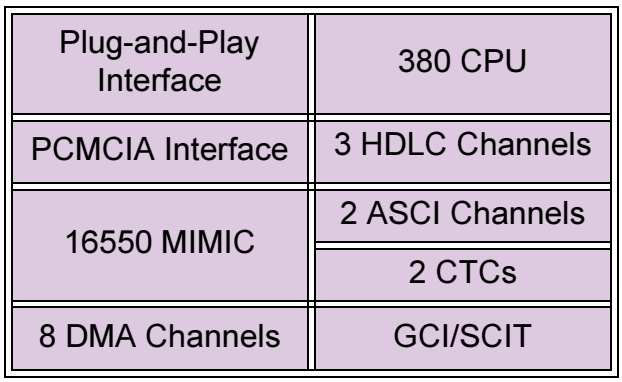
Z80382, Z8L382

Data Communications Processors

PB007502-1201

Preliminary Product Brief

Product Block Diagram



Features

- Embedded Z380™ Microprocessor
  - Maintains Object Code Compatibility with Z80® and Z180™ Microprocessors
  - Enhanced Instruction Set for 16-Bit Operation
  - 16 MB Linear Addressing
  - Two Clock Cycle Instruction Execution Minimum
  - Four On-Chip Register Banks
  - BC/DE/HL/IX/IY Augmented to 32 Bits
  - Clock Divide-by-Two and Multiply-by-Two Options
  - Fully Static CMOS Design with Low-Power STANDBY Mode
  - 16-Bit Internal Bus
  - Dynamic Bus Sizing (8/16-Bit Inter-Operability)
- 16550 MIMIC with I/O Mailbox, DMA Mailbox, and 16 mA Bus Drive
- Three HDLC Synchronous Serial Channels
  - Serial Data Rate of up to 10 Mbps
- GCI/SCIT Bus Interface
- Eight Advanced DMA Channels with 24-Bit Addressing
- Plug-and-Play ISA Interface
- PCMCIA Interface
- Two Enhanced ASCIs (UARTs) with 16-Bit Baud Rate Generators (BRG)
- Clocked Serial I/O Channel (CSIO) for Use with Serial Memory
- Two 16-Bit Timers with Flexible Prescalers
- Three Memory Chip Selects with Wait-State Generators
- Watch-Dog Timer (WDT)
- Up to 32 General-Purpose I/O Pins
- DC to 20 MHz Operating Frequency @ 5.0V
- DC to 10 MHz Operating Frequency @ 3.3V
- 144-Pin QFP and VQFP Style Packages

General Description

The Z80382 (Z382) is designed to address high-end data communication applications such as digital modems (ISDN, GSM, Mobitex & Modacom), xDSL and analog modems (V.34 and beyond). The Z382 provides a performance upgrade to existing Z80- and Z18x-based designs by utilizing the increased bandwidth of the 380C processor. The Z8L382 is a low voltage version of the device.

In this document the notation 380C denotes the Z380-compatible CPU core which is embedded in the Z382.

The 380C microprocessor is a high-performance processor with fast and efficient throughput and increased memory addressing capabilities. The 380C offers a continuing growth path for present Z80- or Z18x-based designs, while maintaining Z80 and Z180 object code compatibility. Its enhancements include added instructions, expanded 16 MB address space and flexible bus interface timing.

In the 380C, the basic addressing modes of the Z80 microprocessor have been augmented to include Stack Pointer Relative loads and stores, 16-bit and 24-bit indexed offsets, and more flexible Indirect Register addressing. Internally, all of the addressing modes allow up to 32-bit linear addressing; however, the Z382 has 24 address pins, therefore it can address a maximum of 16 MB of memory.

Other additions to the instruction set include a full complement of 16-bit arithmetic and logical operations, 16-bit I/O operations, multiply and divide, and a complete set of register-to-register loads and exchanges.

The 380C register file includes alternate versions of the IX and IY registers. There are four banks of registers in the 380C, along with instructions for switching among them. All of the 16-bit register pairs and index registers in the basic Z80 microprocessor register file are expanded to 32 bits.

The Z382 includes dynamic bus sizing to allow any mix of 8- and 16-bit memory, and I/O devices in a system. One application for this capability would be to copy code from a low-cost, slow 8-bit ROM to 16-bit RAM, from which it can be executed at much higher speeds. Memory bus sizes can be configured internally by software to eliminate the need for external logic to drive MSIZE.

Some features that have traditionally been handled by external peripherals have been incorporated in the Z382. These on-chip peripherals reduce system chip count and interconnections on the external bus. Figure 1, the Z382 Block Diagram, summarizes these peripherals. Figure 2 illustrates the Z382 pinout and pin direction diagram.

HDLC Synchronous Channels. Three HDLC channels operate at serial data rates of up to 10 Mbps and feature 8-byte receive and transmit FIFOs. These can be used for modems, general data communications, and ISDN. The ISDN can be handled separately or through the GCI/SCIT bus interface. HDLC Channels always transfer data through the DMA channels. A transparent mode is selectable. Two of the HDLC cells can be pin multiplexed with the ASCIs (UARTs) to provide dynamically switchable (async-sync) DTE interfaces.

DMA Channels. The eight DMA channels provide 24-bit memory addressing and can transfer memory block sizes of up to 64 KB (16-bits) word. These DMA channels can be dynamically assigned to serve the HDLC ports, MIMIC COM port, Host DMA Mailbox, or ASCIs in any mixture. Linked list operation allows all HDLC transmitters and receivers to operate at or above T1/E1 rates simultaneously without loading the bus bandwidth.

16550 MIMIC. Provides connection to a PC ISA bus and emulation of the 16550 UART register set. Improvements include 16 mA output drivers and internal COM port address decoding to reduce external PC interface components.

ASCI. Two flexible asynchronous serial channels with baud rate generators, modem control and status.

CSIO. A clocked serial I/O channel which can be used for serial memory interface.

Timers. Two 16-bit counter/timers with flexible prescalers for wide-range timing applications.

GCI/SCIT Bus Interface. A common interface to ISDN interface devices. Internal signals from this module can be connected to the HDLC channels to provide two B-channels and one D-channel for ISDN.

Plug-and-Play ISA Interface. Provides auto-configuration in ISA (AT bus) applications.

PCMCIA Interface. Provides connectivity to a PCMCIA bus.

32-Bit General-Purpose I/O. For non-PC add-in applications, four 8-bit ports are provided for general- purpose I/O. In ISA or PCMCIA applications, the pins from two of the ports are reallocated to host bus signals and are not available. Pins from the other two ports are selectively multiplexed with on-chip peripheral functions (ASCIs, CSIO, PRT). These pins are individually programmable for input/output mode.

I/O Chip Selects. Two I/O chip selects are provided to support I/O access of external peripherals. Each has a programmable base address and provides I/O decode sizes ranging from 8 to 512 bytes.

ROM/RAM Chip Selects with Wait-State Generators. Chip select outputs are provided to decode memory addresses and provide memory chip enables. Each chip select has its own Wait State Generator to allow use of memories with different speeds.

Watch-Dog Timer. A Watch-Dog Timer (WDT) with a wide range of time-constants prevents code runaway and possible resulting system damage. The RESET input can be forced as an output upon the terminal count of the WDT. This allows external peripherals to be reset along with the Z382.

Block Diagram

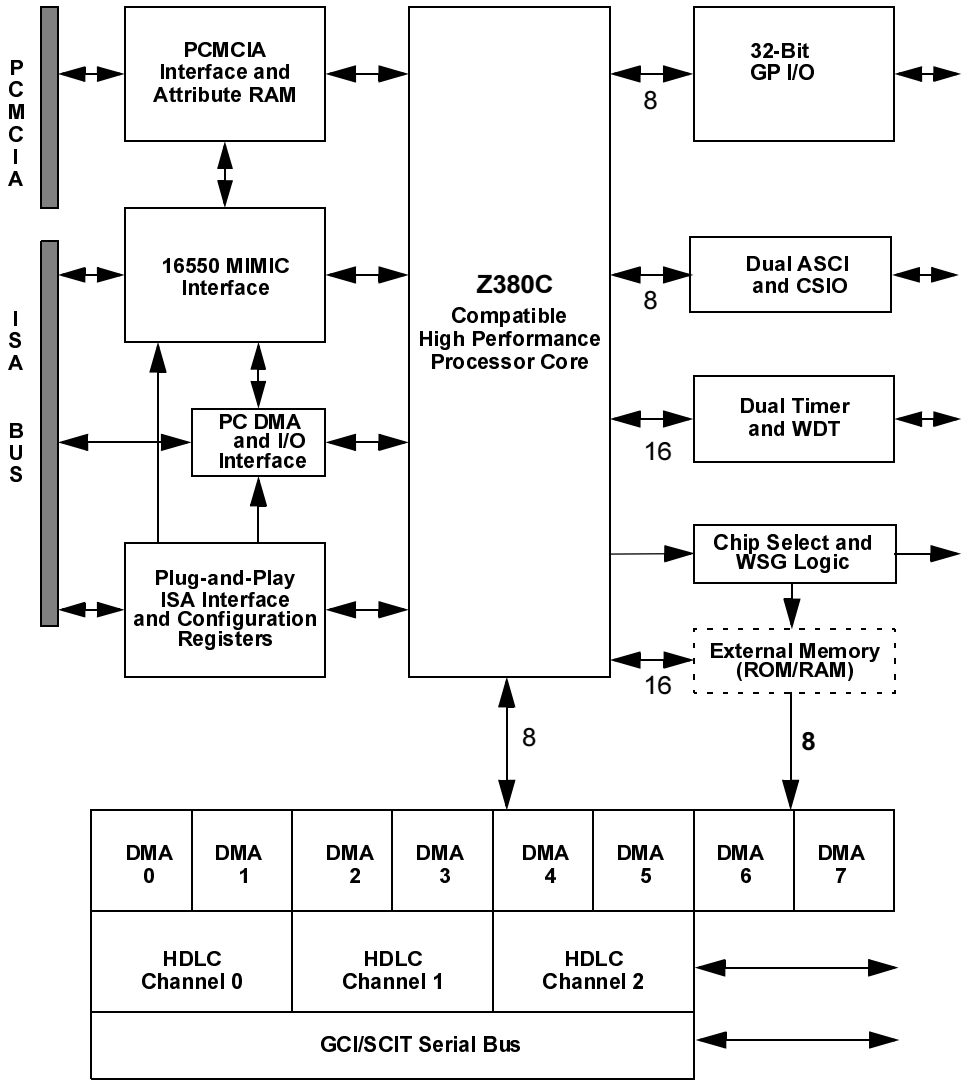


Figure 1. Z80382 Block Diagram

Pin-Outs and Pin Direction

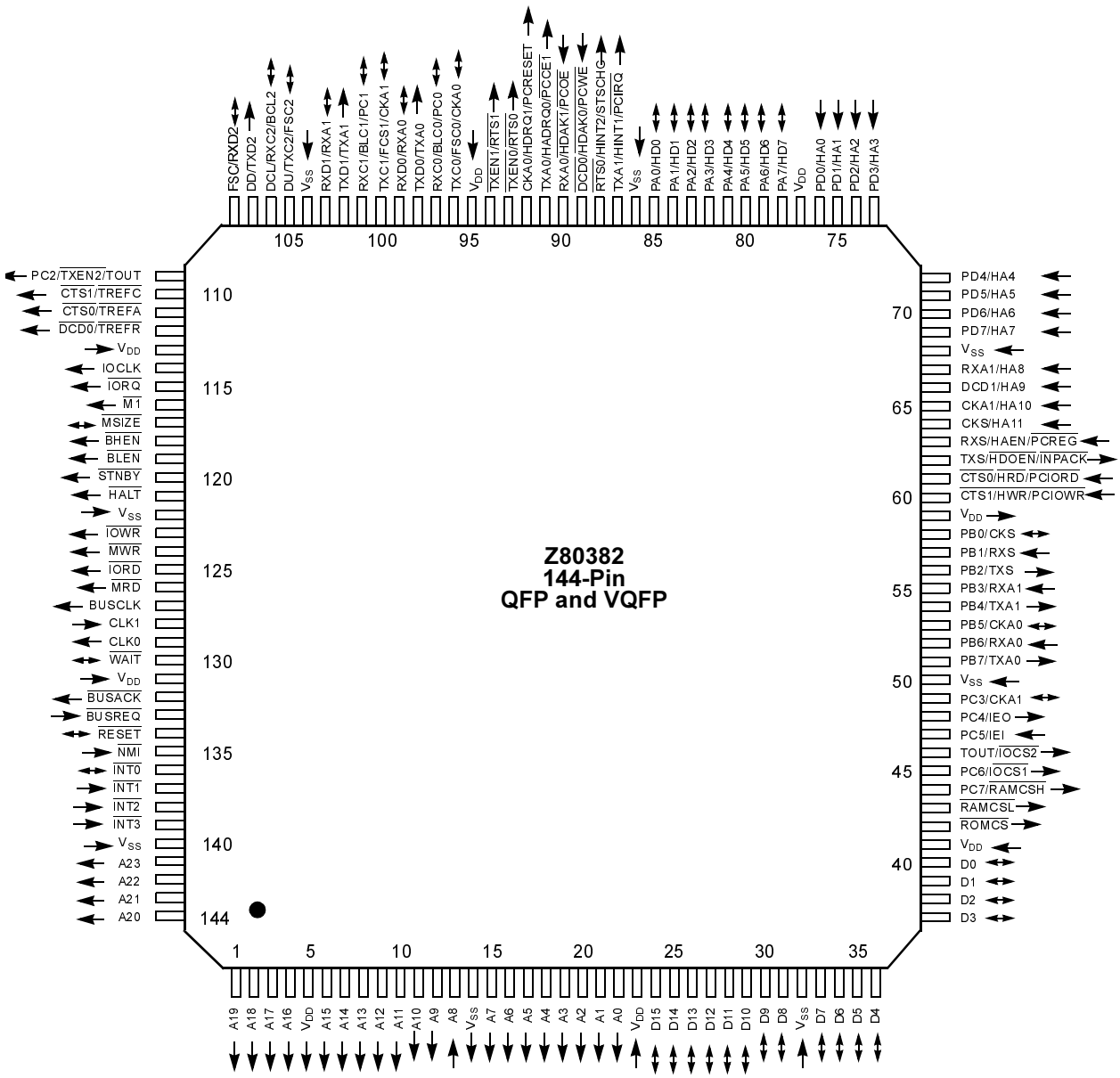


Figure 2. Z80382 Pinout and Pin Direction Diagram

Applications and Support Tools

- Z380ZDA0100ZCC - Compiler

Related Products

Products of interest are:

Table 1 Related Products

Z80380	Embedded Microprocessor
XXXXXXXXZCO	Evaluation Board
Z80180	Embedded Microprocessor

Electrical Features Summary

- Power Dissipation:
  - Z80382—750mW
  - Z8L382—250 mW
- +4.5V≤ V_{DD} ≤ +5.5V Operating Range (Z80382 versions)
- +3.0V≤ V_{DD} ≤ +3.6V Operating Range (Z8L382 versions)

Ordering Information

Part	PSI	Description
Z8038220ASC	20 MHz	16-Bit Z80 Embedded Procesor
Z8038220FSC	20 MHz	16-Bit Z80 Embedded Processor

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