infineon

BGS16MN14

SP6T Diversity Antenna Switch with MIPI RFFE Interface

Data Sheet

Revision 3.3 - September 16, 2016

Power Management & Multimarket

Edition September 16, 2016

Published by Infineon Technologies AG
81726 Munich, Germany

©2016 Infineon Technologies AG
All Rights Reserved.

LEGAL DISCLAIMER

THE INFORMATION GIVEN IN THIS APPLICATION NOTE IS GIVEN AS A HINT FOR THE IMPLEMENTATION OF THE INFINEON TECHNOLOGIES COMPONENT ONLY AND SHALL NOT BE REGARDED AS ANY DESCRIPTION OR WARRANTY OF A CERTAIN FUNCTIONALITY, CONDITION OR QUALITY OF THE INFINEON TECHNOLOGIES COMPONENT. THE RECIPIENT OF THIS APPLICATION NOTE MUST VERIFY ANY FUNCTION DESCRIBED HEREIN IN THE REAL APPLICATION. INFINEON TECHNOLOGIES HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND (INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY) WITH RESPECT TO ANY AND ALL INFORMATION GIVEN IN THIS APPLICATION NOTE.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Document No.: BGS16MN14_v3.3.pdf	
Revision History: Revision 3.3	
Previous Version: Revision 3.2	
Page	**Subjects (major changes since last revision)**
16	Tape drawing updated in Figure 13

Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™,CoolGaN™,CoolMOS™, CoolSET™, CoolSiC™, CORECONTROL™, DAVE™, DI-POL™,EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, ISOFACE™, I²RF™, IsoPACK™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OptiMOS™, ORIGA™, OPTIGA™, PROFET™, PRO-SIL™, PRIMARION™, PrimePACK™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SIPMOS™, SOLID FLASH™, SmartLEWIS™, TEMPFET™, thinQ!™, TriCore™, TRENCHSTOP™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, PRIMECELL™, REALVIEW™, THUMB™ of ARM Limited, UK. AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. Mifare™ of NXP. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Sattelite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Last Trademarks Update 2012-12-13

Contents

1 **Features** 5
2 **Product Description** 5
3 **Maximum Ratings** 6
4 **Operation Ranges** 7
5 **RF Characteristics** 8
6 **MIPI RFFE Specification** 10
7 **Pin Definition and Package Outline** 14

List of Figures

1 BGS16MN14 block diagram . . . 6
2 MIPI to RF Time . . . 9
3 Received clock signal constraints . . . 11
4 Bus active data receiver timing requirements . . . 12
5 Bus park cycle timing . . . 12
6 Bus active data transmission timing specification . . . 13
7 Requirements for VIO-initiated reset . . . 13
8 Pin configuration (top view) . . . 14
9 Application circuit . . . 15
10 Package outline . . . 15
11 Marking . . . 16
12 Land pattern and stencil mask . . . 16
13 Tape dimensions . . . 16

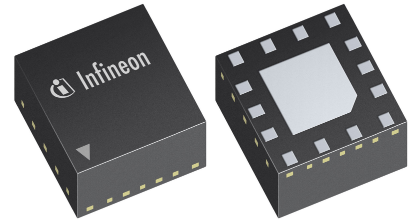
List of Tables

1 Ordering information . . . 5
2 Maximum ratings, Table I . . . 6
3 Maximum ratings, Table II . . . 7
4 Operation ranges . . . 7
5 RF input power . . . 7
6 RF characteristics . . . 8
7 IMD2 Testcases . . . 9
8 IMD3 Testcases . . . 9
9 Switching Time . . . 9
10 Register mapping . . . 10
11 MIPI RFFE operating timing . . . 11
12 Truth table . . . 13
13 Pin configuration . . . 14

SP6T Diversity Antenna Switch

1 Features

- Suitable for multi-mode WCDMA / LTE diversity applications
- Ultra-low insertion loss and harmonics generation
- 6 high-linearity, interchangeable RX ports
- 0.1 to 6.0 GHz coverage
- High port-to-port-isolation
- Direct to battery supply enabled by large supply voltage range from 2.5 V to 5.5 V
- Integrated MIPI RFFE interface supporting 1.2 and 1.8 V bus voltage
- Software programmable MIPI RFFE USID
- No decoupling capacitors required if no DC applied on RF lines
- Small form factor 2.0 mm x 2.0 mm
- 1 kV HBM ESD protection
- RoHS and WEEE compliant package



2 Product Description

The BGS16MN14 is a Single Pole Six Throw (SP6T) Diversity Switch Module optimized for wireless applications up to 2.7 GHz. It is a perfect solution for multi-mode handsets based on EDGE, WCDMA and LTE. The switch module configuration is shown in Fig. 1. The module comes in a miniature TSNP package and comprises of a high power CMOS SP6T switch with integrated MIPI RFFE interface.

No external DC blocking capacitors are required in typical applications as long as no DC is applied to any RF port.

Table 1: Ordering Information

Type	Package	Marking
BGS16MN14	PG-TSNP-14-3	16M2

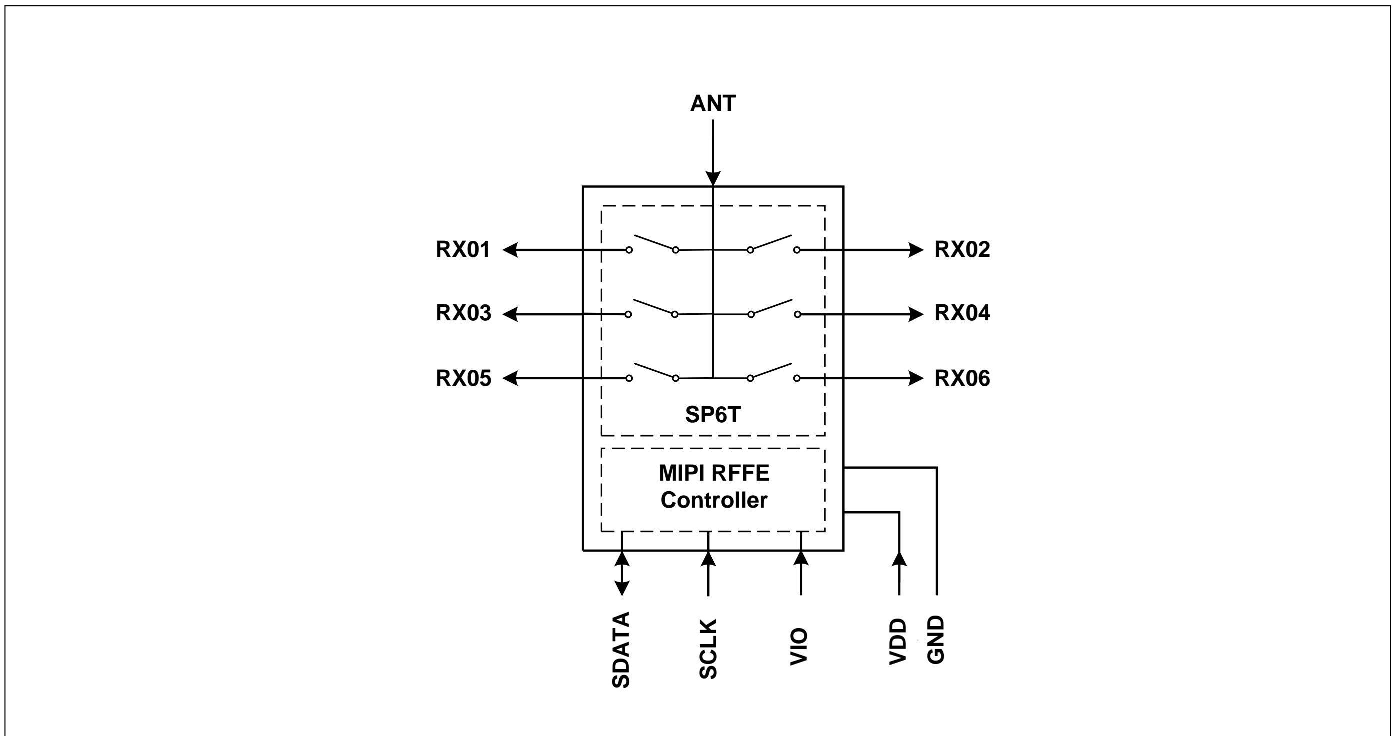


Figure 1: BGS16MN14 block diagram

3 Maximum Ratings

Table 2: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency range	f	0.1	–	–	GHz	[1]
Supply voltage	V_{DD}	-0.5	–	6.0	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
Junction temperature	T_j	–	–	125	°C	–
RF input power at all RX ports	P_{RF_RX}	–	–	32	dBm	CW
ESD capability, CDM [2]	$V_{ESD_{CDM}}$	−500	–	+500	V	All pins
ESD capability, HBM [3]	$V_{ESD_{HBM}}$	-1	–	+1	kV	Digital, digital versus RF
		-1	–	+1	kV	RF
ESD capability, system level [4]	$V_{ESD_{ANT}}$	−8	–	+8	kV	ANT versus system GND, with 27 nH shunt inductor

[1] Switch has no highpass response. There is also a DC connection between switched paths. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Field-Induced Charged-Device Model JESD22-C101. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[3] Human Body Model ANSI/ESDA/JEDEC JS-001-2012 (R = 1.5 kΩ, C = 100 pF).
[4] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Table 3: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction - soldering point	R_{thJS}	–	60	–	K/W	–
Maximum DC-voltage on RF ports and RF ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF ports
RFFE supply voltage	V_{IO}	-0.5	–	3.6	V	–
RFFE control voltage levels	V_{SCLK}, V_{SDATA}	-0.7	–	V_{IO}+0.7	V	–

4 Operation Ranges

Table 4: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	2.5	3.5	5.5	V	–
Supply current[2)]	I_{DD}	–	80	200	μA	–
Supply current in user low power mode[2)]	I_{LP}	-	0.6	10	μA	–
Supply current in shutdown state[2)]	I_{SD}	-	0.5	1	μA	–
RFFE supply voltage	V_{IO}	1.1	1.8	1.95	V	–
RFFE input high voltage[1)]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1)]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1)]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1)]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current[2)]	I_{VIO}	–	15	–	μA	Idle state
Ambient temperature	T_A	-30	25	85	°C	–

[1)]SCLK and SDATA
[2)] T_A = -30 °C...+85 °C, V_{DD} = 2.5...5.5 V

Table 5: RF Input Power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RX ports (50Ω)	P_{RF_RX}	–	–	27	dBm	–

5 RF Characteristics

Table 6: RF Characteristics at T_A = -30 °C...+85 °C, P_{IN} = 0 *dBm*, V_{DD} = 2.5...5.5 *V*, Z_0=50Ω, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss						
RX01-06	IL	–	0.30	0.40	dB	0.1 to 1.0 GHz
		–	0.40	0.50	dB	1.0 to 2.0 GHz
		–	0.45	0.55	dB	1.0 to 2.7 GHz
		–	0.75	1.30	dB	5.0 to 6.0 GHz
Return Loss[1)]						
RX01-06	RL	16	22	–	dB	0.1 to 1.0 GHz
		15	20	–	dB	1.0 to 2.0 GHz
		13	18	–	dB	2.0 to 2.7 GHz
		9	15	–	dB	5.0 to 6.0 GHz
Isolation (ANT-RX)						
RX01-06	ISO	30	42	–	dB	0.1 to 1.0 GHz
		25	37	–	dB	1.0 to 2.0 GHz
		23	35	–	dB	2.0 to 2.7 GHz
		15	23	–	dB	5.0 to 6.0 GHz
Intermodulation Distortion (UMTS Band 1, Band 5)[1)]						
2nd order intermodulation	IMD2 low	–	-105	-95	dBm	IMT, US Cell (see Tab. 7)
3rd order intermodulation	IMD3	–	-110	-105	dBm	IMT, US Cell (see Tab. 8)
2nd order intermodulation	IMD2 high	–	-110	-100	dBm	IMT, US Cell (see Tab. 7)
Harmonic Generation (UMTS Band 1, Band 5)[1)]						
H2	P_{Harm}	75	85	–	dBc	25 dBm, 50Ω, CW mode
H3	P_{Harm}	80	90	–	dBc	25 dBm, 50Ω, CW mode

[1)]On application board with application circuit according to Fig. 9

Table 7: IMD2 Testcases

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	190 (IMD2 low)	-15
			4090 (IMD2 high)	
US Cell	835	20	45 (IMD2 low)	-15
			1715 (IMD2 high)	

Table 8: IMD3 Testcases

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	1760	-15
US Cell	835	20	790	-15

Table 9: Switching Time at T_A = -30 °C...+85 °C, P_{IN} = 0 *dBm*, Supply Voltage = 2.5 V...2.5 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching Time						
MIPI to RF time	t_{INT}	–	1.5	2	μs	50 % last SCLK falling edge to 90 % ON, see Fig. 2
Power up settling time	t_{PUP}	–	10	25	μs	After power down mode

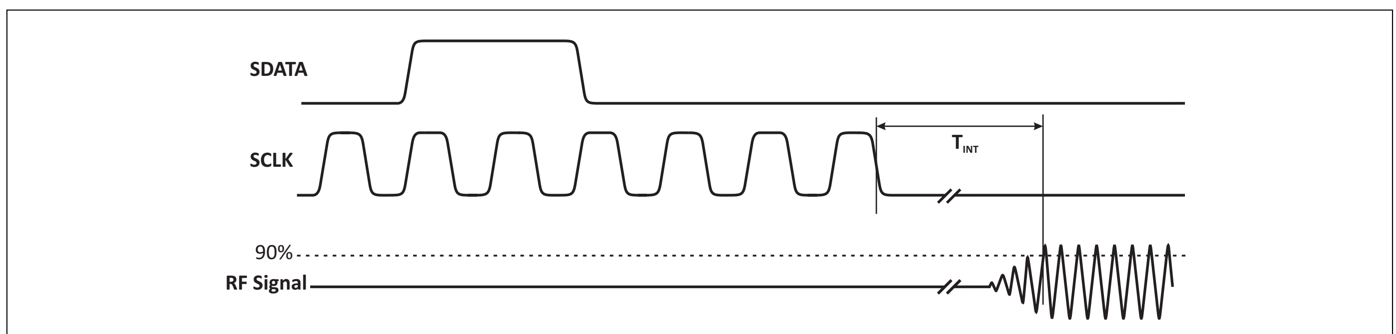


Figure 2: MIPI to RF Time

6 MIPI RFFE Specification

Supported MIPI Functions

The MIPI RFFE interface supports following functions:

- Register write command sequence
- Register read command sequence
- Register 0 write command sequence
- Programmable USID
- Trigger function

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 1.10 - 26. July 2011. By default the device goes into low power mode after power on.

Table 10: Register Mapping

Register Address	Register Name	Data Bits	Function	Default	Broadcast Support	Trigger Support	R/W
0x0000	REGISTER_0	7:0	MODE_CTRL	00000000	No	Yes	R/W
0x001C	PM_TRIG	7:6	PWR_MODE	10	Yes	No	R/W
		5	TRIGGER_MASK_2	0	No	No	
		4	TRIGGER_MASK_1	0	No	No	
		3	TRIGGER_MASK_0	0	No	No	
		2	TRIGGER_2	0	Yes	No	
		1	TRIGGER_1	0	Yes	No	
		0	TRIGGER_0	0	Yes	No	
0x001D	PRODUCT_ID	7:0	PRODUCT_ID	10001001	No	No	R
0x001E	MANUFACTURER_ID	7:0	MANUFACTURER_ID [7:0]	00011010	No	No	R
0x001F	MAN_USID	7:6	SPARE	00	No	No	R/W
		5:4	MANUFACTURER_ID [9:8]	01			
		3:0	USID	1010			
0x001B	GROUP_SID	7:4	RESERVED	0	No	No	R/W
		3:0	GROUP_SID	0			

Table 11: MIPI RFFE Operating Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK Frequency	FSCLK	0.032	–	26	MHz	Full speed
		0.032	–	13	MHz	Half speed
SCLK Period	TSCLK	0.038	–	32	μs	Full speed
		0.077	–	32	μs	Half speed
SCLK Low Period	TSCLKIL	11.25	–	–	ns	Full speed, see Fig. 3
		24	–	–	ns	Half speed, see Fig. 3
SCLK High Period	TSCLKIH	11.25	–	–	ns	Full speed, see Fig. 3
		24	–	–	ns	Half speed, see Fig. 3
SDATA Setup Time	TS	1	–	–	ns	Full speed, see Fig. 4
		2	–	–	ns	Half speed, see Fig. 4
SDATA Hold Time	TH	5	–	–	ns	Full speed, see Fig. 4
		5	–	–	ns	Half speed, see Fig. 4
SDATA Release Time	TSDATAZ	–	–	10	ns	Full speed, see Fig. 5
		–	–	18	ns	Half speed, see Fig. 5
Time for Data Output	TD	–	–	10.25	ns	Full speed, see Fig. 6
		–	–	22	ns	Half speed, see Fig. 6
SDATA Rise/Fall Time	TSDATAOTR	2.1	–	6.5	ns	Full speed, see Fig. 6
		2.1	–	10	ns	Half speed, see Fig. 6
VIO Rise Time	TVIO-R	10	–	450	μs	See Fig. 7
VIO Reset Time	TVIO-RST	10	–	–	μs	See Fig. 7
Reset Delay Time	TSIGOL	0.12	–	–	μs	See Fig. 7

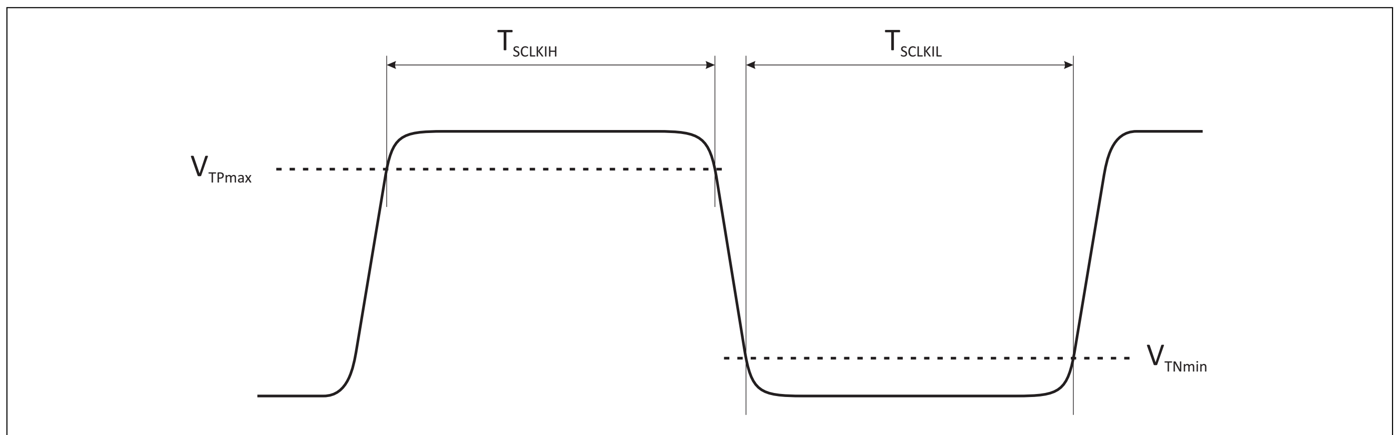


Figure 3: Received clock signal constraints

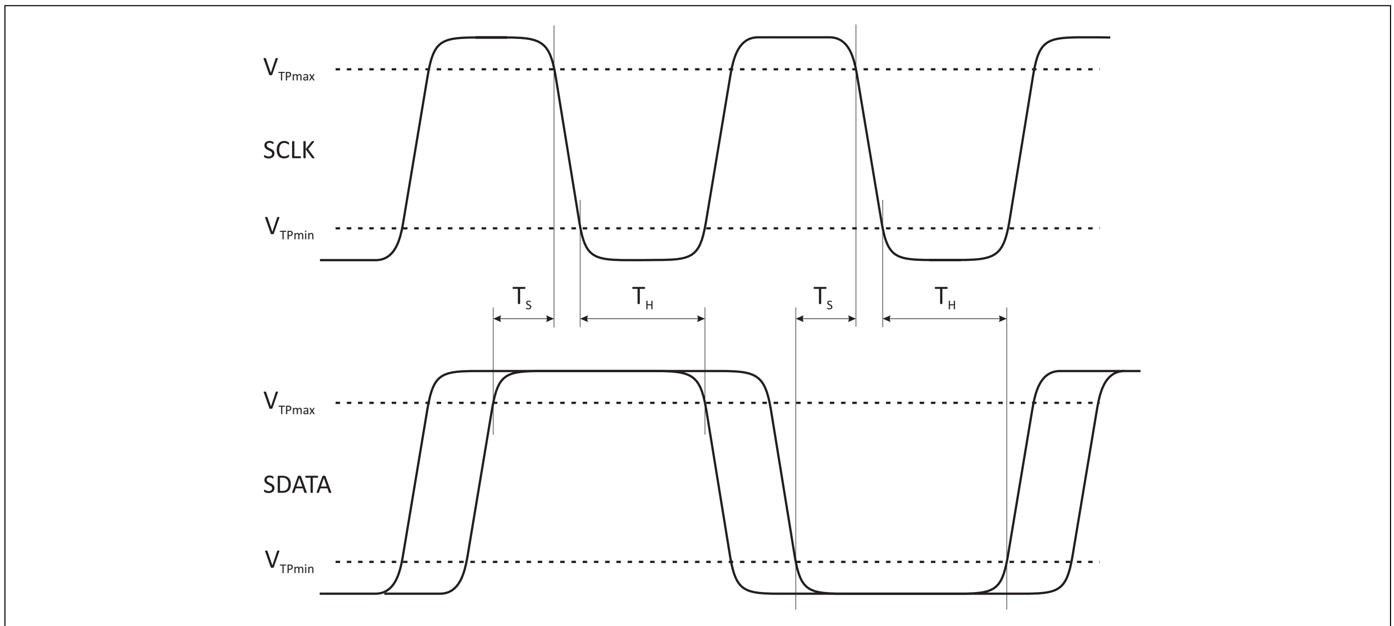


Figure 4: Bus active data receiver timing requirements

V_{TPmax}

SCLK

V_{TNmin}

T_{SDATAZ}

V_{OHmin}

SDATA

V_{OLmax}

Bus Park Cycle

Signal driven

Signal not driven, pull down only

T_{SDATAZ} is measured from SCLK V_{TN} level for a device receiving SCLK and driving SDATA lines

Figure 5: Bus park cycle timing

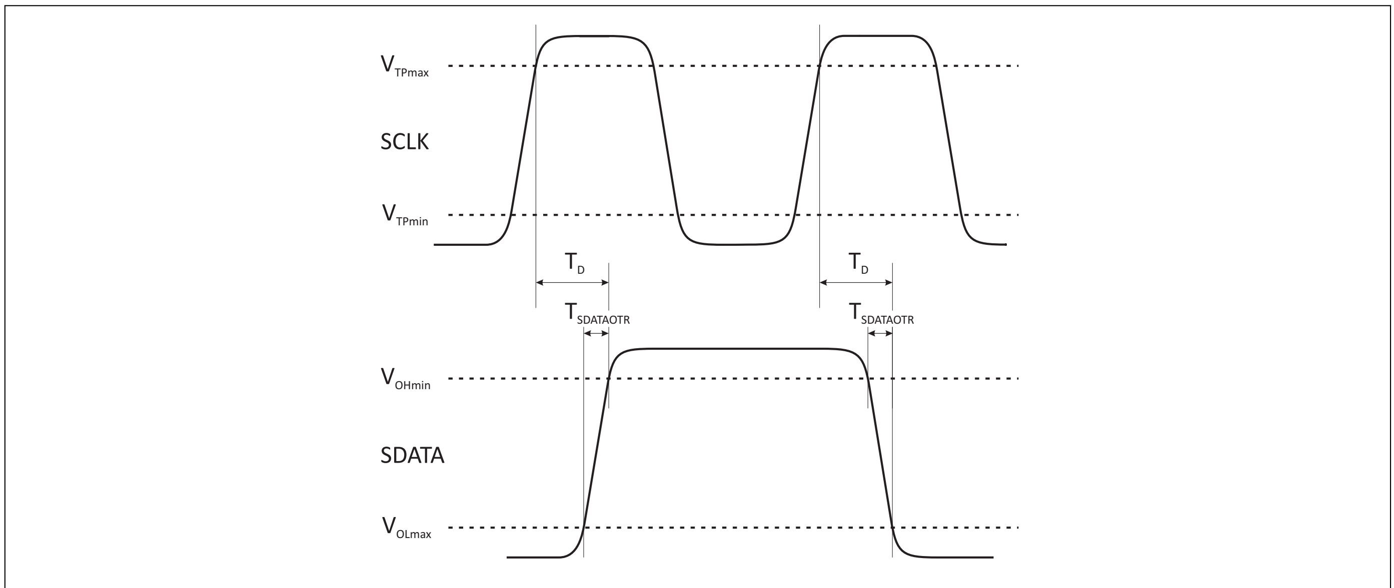


Figure 6: Bus active data transmission timing specification

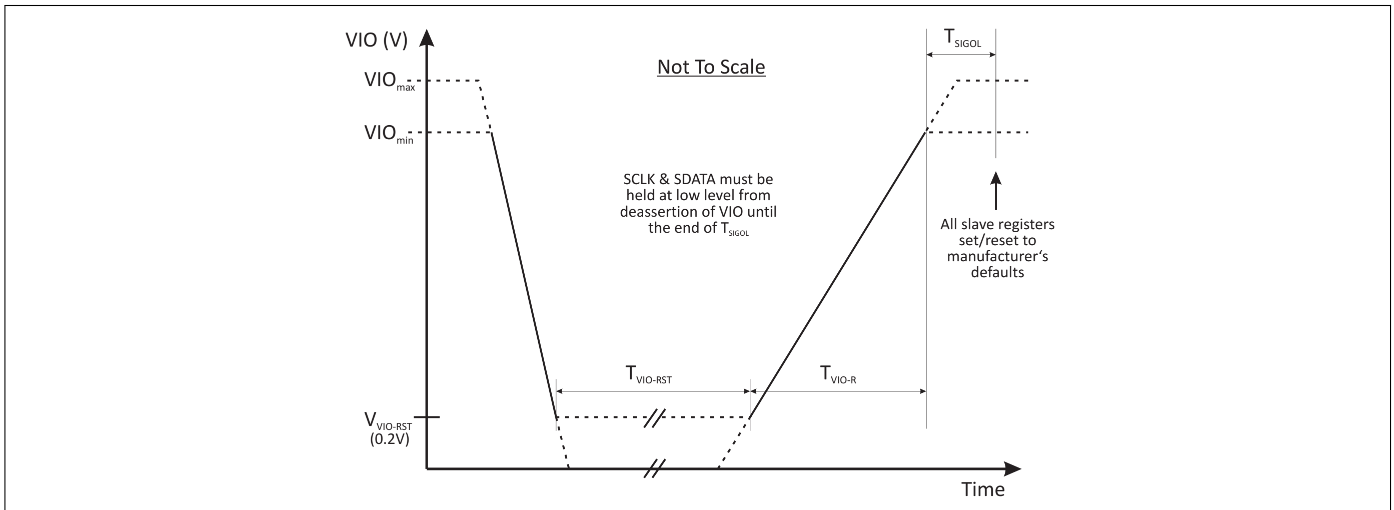


Figure 7: Requirements for VIO-initiated reset

Table 12: Modes of Operation (Truth Table)

		REGISTER_0 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	Isolation	x	0	0	0	0	0	0	0
2	RX01	x	0	0	0	0	0	1	0
3	RX02	x	0	0	0	0	0	0	1
4	RX03	x	0	0	0	0	0	1	1
5	RX04	x	0	0	0	0	1	1	1
6	RX05	x	0	0	0	0	1	0	1
7	RX06	x	0	0	0	0	1	1	0

7 Pin Definition and Package Outline

Table 13: Pin Configuration

No.	Name	Pin Type	Buffer Type	Function
0	GND	GND		RF ground; die pad
1	RX03	I/O		RX port 3
2	RX02	I/O		RX port 2
3	RX01	I/O		RX port 1
4	VDD	PWR		V_{DD} supply
5	VIO	PWR		MIPI RFFE supply
6	SDATA	I/O		MIPI RFFE data
7	SCLK	I		MIPI RFFE clock
8	NC			Not connected
9	RX06	I/O		RX port 6
10	RX05	I/O		RX port 5
11	RX04	I/O		RX port 4
12	NC			Not connected
13	ANT	I/O		Antenna port
14	NC			Not connected

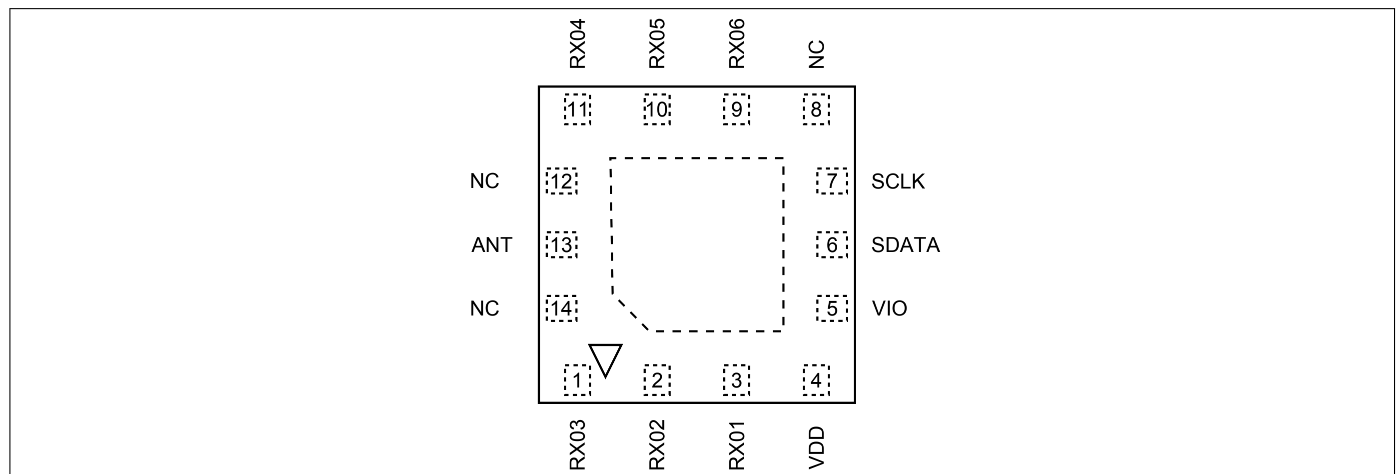


Figure 8: Pin configuration (top view)

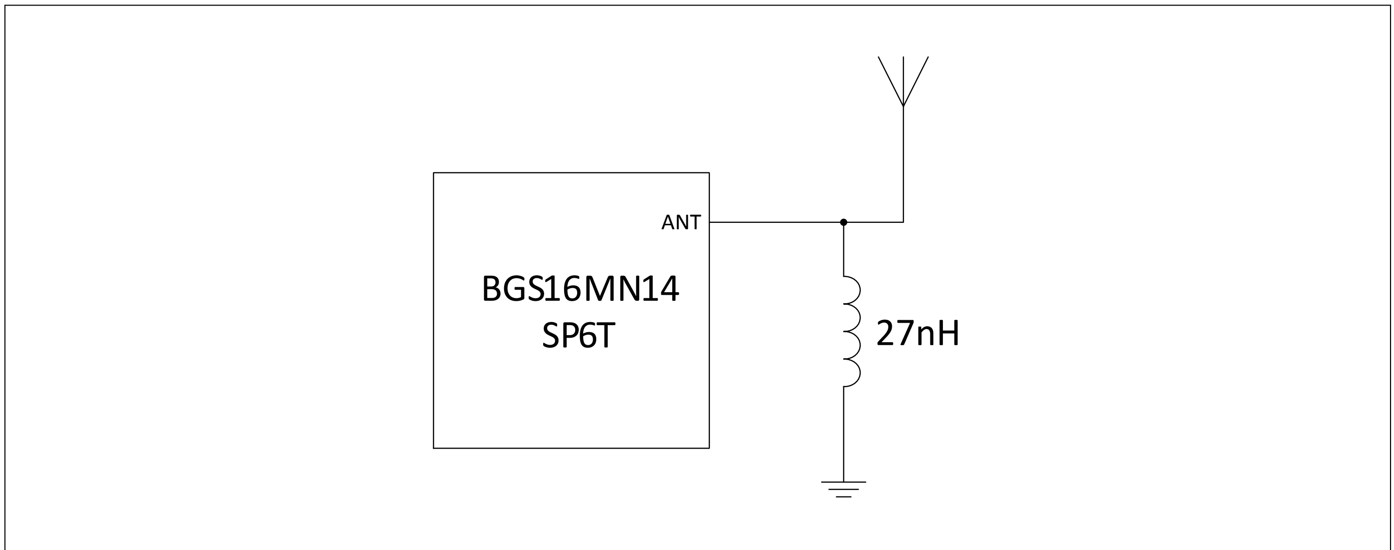


Figure 9: Application circuit

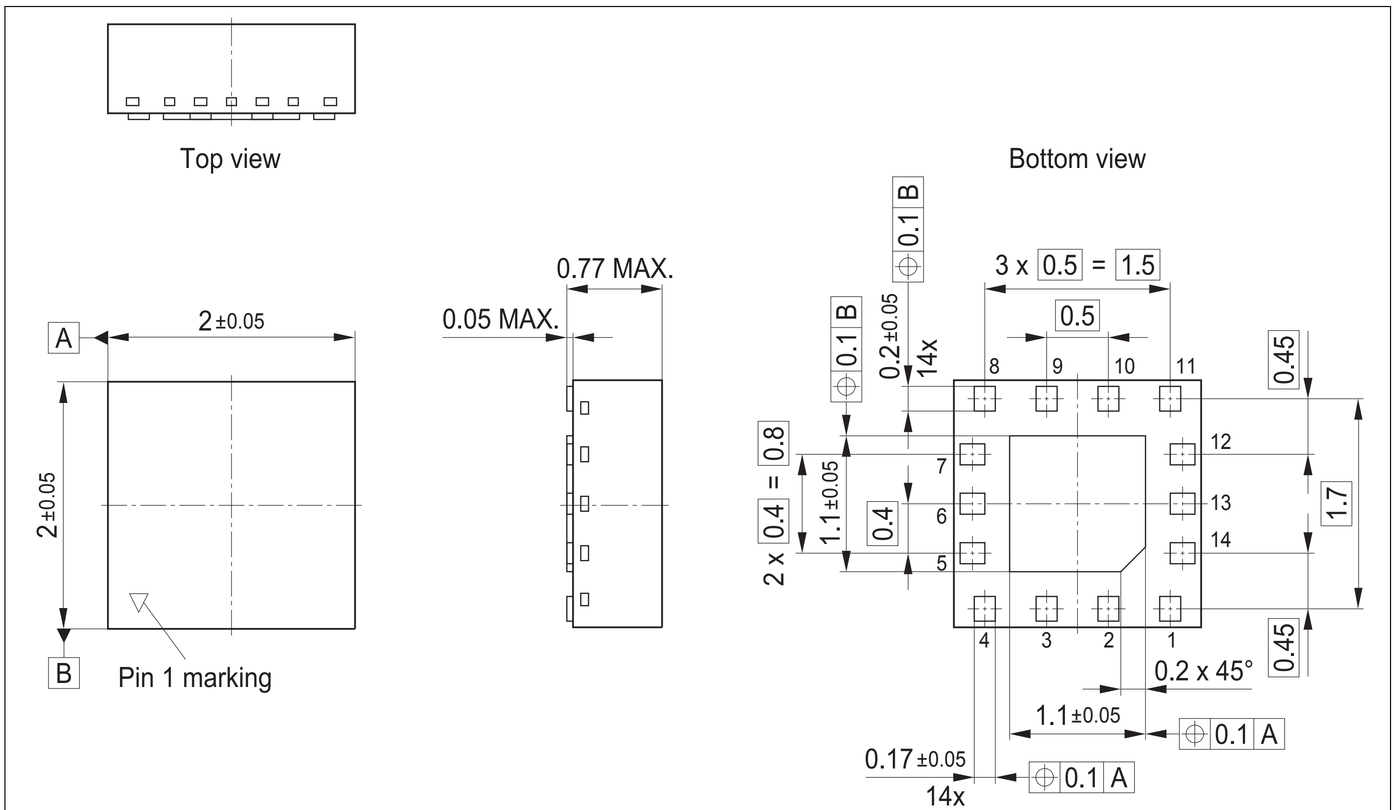


Figure 10: Package outline

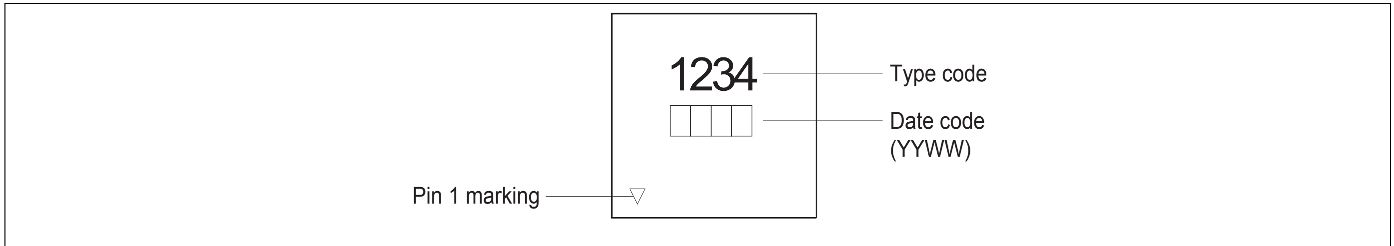


Figure 11: Marking

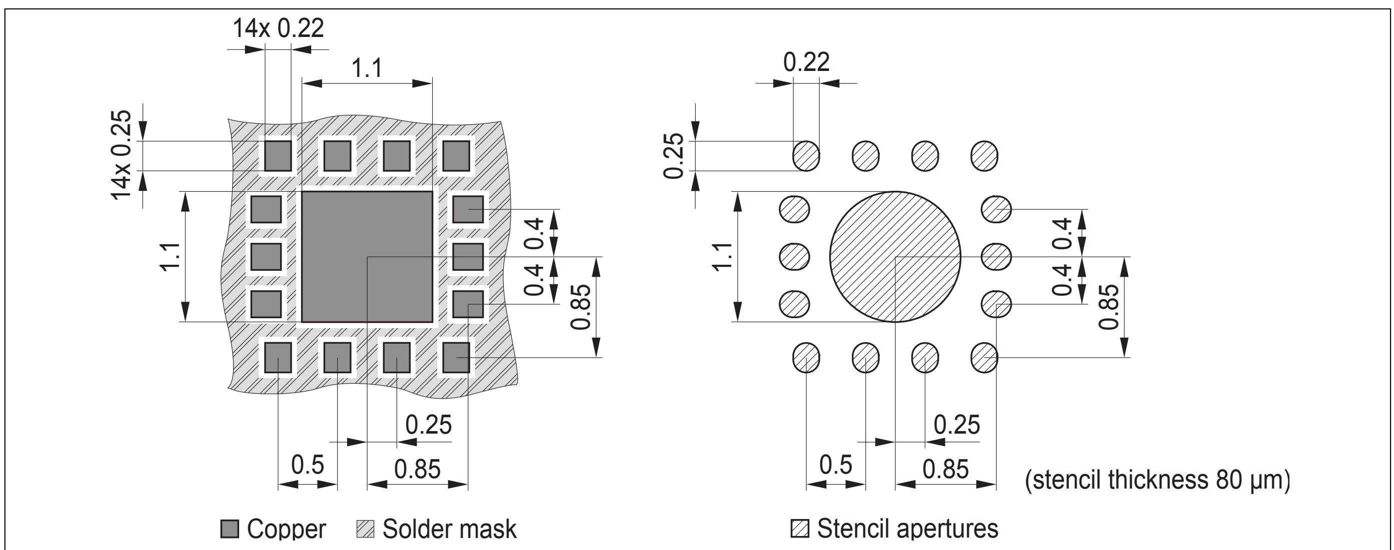


Figure 12: Land pattern and stencil mask

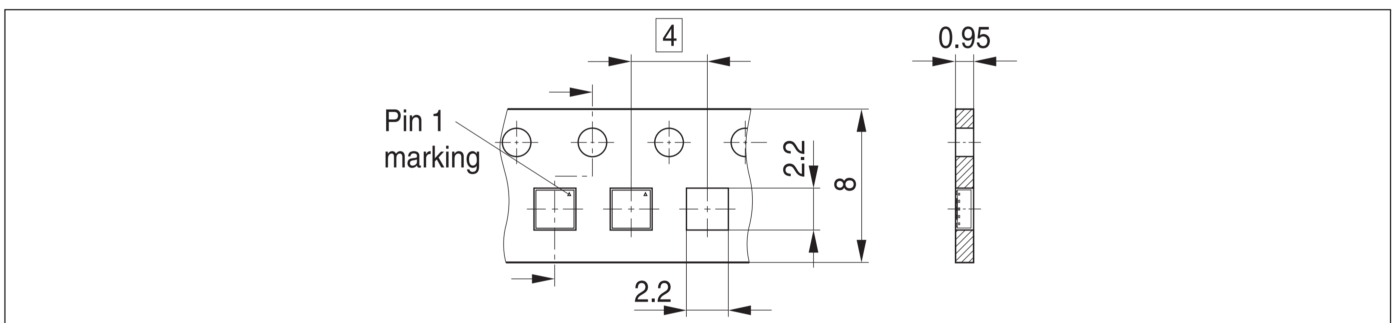


Figure 13: Tape dimensions

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG