NL3HS644

2:1 MIPI D-PHY (1.5 Gbps) 4-Data Lane Switch

The NL3HS644 is a 4−data lane MIPI, D−PHY switch. This single−pole double−throw (SPDT) switch is optimized for switching between 2 high−speed or low−power MIPI sources. The NL3HS644 is designed for MIPI specifications and allows connection to a CSI or DSI module.

Features

- Operating Supply: V_{CC} = 1.65 V to 4.5 V
- Switch Signal Range: 0 to V_{CC}
- Signal Types: MIPI, D−PHY
- ON−Resistance:
  R_{ON} = 8 Ω (Typ) HS MIPI
  R_{ON} = 7.9 Ω (Typ) LP MIPI
- ON−Resistance Mismatch:
  ΔR_{ON} = 0.09 Ω (Typ) HS MIPI
  ΔR_{ON} = 0.17 Ω (Typ) LP MIPI
- ON Resistance Flatness:
  R_{ON_FLAT} = 0.03 Ω (Typ) HS MIPI
  R_{ON_FLAT} = 0.46 Ω (Typ) LP MIPI
- Supply Current: I_{CC} = 55 μA (Max)
- Hi−Z Supply Current: I_{CCZ} = 5 μA (Max)
- Off−Isolation: O_{IRR} = −27 dB (Typ)
- Crosstalk: X_{TALK} = −28 dB (Typ)
- Bandwidth: BW = 1,050 MHz (Typ)
- Channel to Channel Skew: t_{SK} = 63 ps (Typ)
- ON Capacitance: C_{ON} = 12.6 pF
- 36−Ball WLCSP Package, 2.36 mm x 2.36 mm
- This device is Pb−Free, Halogen−Free/BFR−Free and are RoHS−Compliant

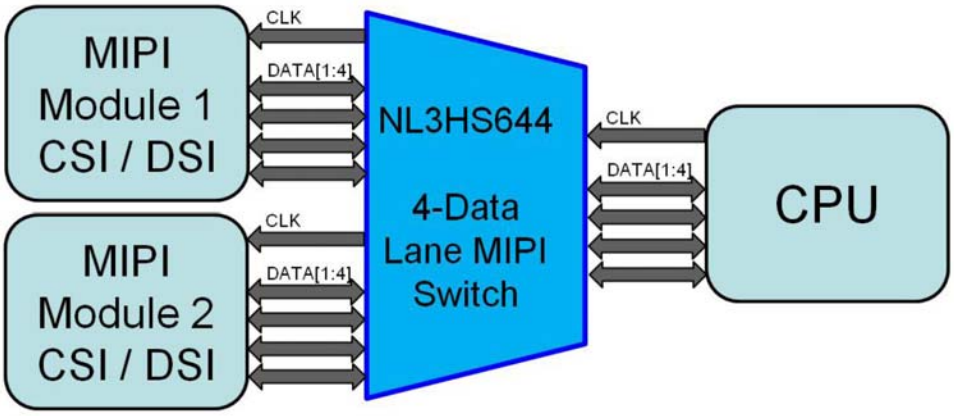


Figure 1. Typical Application – Mobile Phone

ON Semiconductor®

www.onsemi.com

WLCSP36
FC SUFFIX
CASE 567LR

MARKING DIAGRAM

XXXXXX = Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 8 of this data sheet.

FUNCTION TABLE

$\overline{OE}$	SEL	FUNCTION
L	L	CLKP = CLKAP, CLKN = CLKAN, DnP = DAnP, DnN = DAnN
L	H	CLKP = CLKBP, CLKN = CLKBN, DnP = DBnP, DnN = DBnN
H	X	CLKAP/CLKAN, CLKBP/CLKBN, DAnP/DAnN, DBnP/DBnN Ports at High Impedance

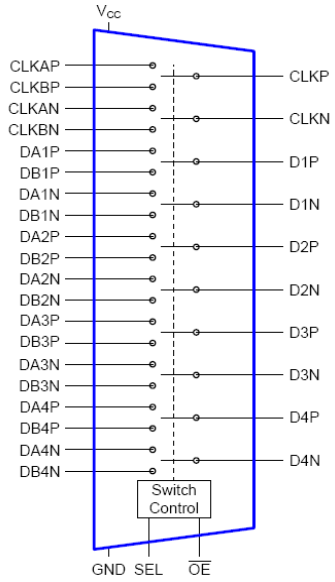


Figure 2. Block Diagram

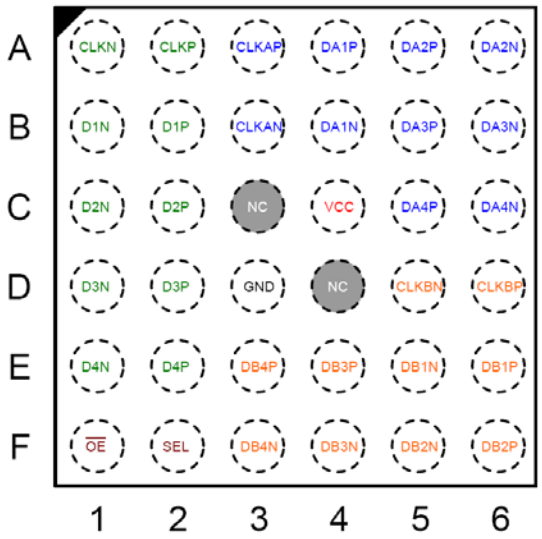


Figure 3. Pinout (Top Through View)

PIN ASSIGNMENT

Pin Name	Ball	Description		
CLKP / CLKN	A2 / A1	Common Clock Path		
D1P / D1N	B2 / B1	Common Data Path 1		
D2P / D2N	C2 / C1	Common Data Path 2		
D3P / D3N	D2 / D1	Common Data Path 3		
D4P / D4N	E2 / E1	Common Data Path 4		
CLKAP / CLKAN	A3 / B3	A−Side Clock Path		
DA1P / DA1N	A4 / B4	A−Side Data Path 1		
DA2P / DA2N	A5 / A6	A−Side Data Path 2		
DA3P / DA3N	B5 / B6	A−Side Data Path 3		
DA4P / DA4N	C5 / C6	A−Side Data Path 4		
CLKBP / CLKBN	D6 / D5	B−Side Clock Path		
DB1P / DB1N	E6 / E5	B−Side Data Path 1		
DB2P / DB2N	F6 / F5	B−Side Data Path 2		
DB3P / DB3N	E4 / F4	B−Side Data Path 3		
DB4P / DB4N	E3 / F3	B−Side Data Path 4		
SEL	F2	Control Pin	SEL = L:	CLKP = CLKAP, CLKN = CLKAN, DnP = DAnP, DnN = DAnN
			SEL = H:	CLKP = CLKBP, CLKN = CLKBN, DnP = DBnP, DnN = DBnN
$\overline{OE}$	F1	Output Enable		
VCC	C4	Power		
GND	D3	Ground		
NC	C3 / D4	No Connect		

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{CC}	Positive DC Supply Voltage	−0.5 to +5.5	V
V_{IS}	Analog Input Voltage	−0.5 to V_{CC} + 0.5	V
V_{IN}	Digital Control Input Voltage (SEL or $\overline{OE}$)	−0.5 to +5.5	V
I_{OS}	Switch Output Current	50	mA
I_{IOK}	Switch Input/Output Diode Current	−50	mA
I_{IK}	Control Input Diode Current	±50	mA
T_s	Storage Temperature	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	1.65	4.5	V
V_{IS}	Switch Input / Output Voltage			V
	HS Mode	0.1	0.3	
	LP Mode	0	1.2	
V_{IN}	Digital Control Input Voltage (SEL or $\overline{OE}$) (Note 1)	GND	V_{CC}	V

1. Control input must be held High or Low. It must not float.

DC ELECTRICAL CHARACTERISTICS

Voltages referenced to GND. All typical values are at T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	T_A = −40°C to +85°C			Unit
				Min	Typ	Max	
DIGITAL CONTROL SECTION (SEL or $\overline{OE}$)							
V_{IK}	Clamp Diode Voltage	I_{IN} = −18 mA	2.8			−1.2	V
V_{IH}	Input Voltage High		1.65 – 4.5	1.0			V
V_{IL}	Input Voltage Low		1.65 – 4.5			0.4	V
I_{IN}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	1.65 – 4.5			±100	nA
SWITCHES							
$R_{ON\_MIPI\_HS}$	Switch ON Resistance for HS MIPI Applications (Note 2)	I_{ON} = −10 mA, $\overline{OE}$ = 0 V, SEL = V_{CC} or 0 V, CLKA, CLKB, DBn or DAn = 0.1, 0.2, 0.3 V	1.8		9	12	Ω
			2.5		8	9	
			3.6		8	9	
			4.5		8	9	
$R_{ON\_MIPI\_LP}$	Switch ON Resistance for LP MIPI Applications (Note 2)	I_{ON} = −10 mA, $\overline{OE}$ = 0 V, SEL = V_{CC} or 0 V, CLKA, CLKB, DBn or DAn = 0, 0.6, 1.2 V	1.8		9.5	12	Ω
			2.5		8.5	10	
			3.6		7.9	9	
			4.5		7.6	9	
$\Delta R_{ON\_MIPI\_HS}$	ON Resistance Matching Between HS MIPI Channels (Note 3)	I_{ON} = −10 mA, $\overline{OE}$ = 0 V, SEL = V_{CC} or 0 V, CLKA, CLKB, DBn or DAn = 0.1, 0.2, 0.3 V	1.8		0.02		Ω
			2.5		0.09		
			3.6		0.09		
			4.5		0.08		

2. Measured by the voltage drop between A and B pins at the indicated current through the switch. ON resistance is determined by the lower of the voltage on the two (A or B ports).
3. Guaranteed by characterization.

DC ELECTRICAL CHARACTERISTICS

Voltages referenced to GND. All typical values are at T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	T_A = −40°C to +85°C			Unit
				Min	Typ	Max	
SWITCHES							
$\Delta R_{ON\_MIPI\_LP}$	ON Resistance Matching Between LP MIPI Channels (Note 3)	I_{ON} = −10 mA, $\overline{OE}$ = 0 V, SEL = V_{CC} or 0 V, CLKA, CLKB, DBn or DAn = 0, 0.6, 1.2 V	1.8		0.17		Ω
			2.5		0.12		
			3.6		0.17		
			4.5		0.09		
$R_{ON\_FLAT\_MIPI\_HS}$	ON Resistance Flatness for HS MIPI Channels (Note 3)	I_{ON} = −10 mA, $\overline{OE}$ = 0 V, SEL = V_{CC} or 0 V, CLKA, CLKB, DBn or DAn = 0.1, 0.2, 0.3 V	1.8		0.23		Ω
			2.5		0.11		
			3.6		0.03		
			4.5		0.02		
$R_{ON\_FLAT\_MIPI\_LP}$	ON Resistance Flatness for LP MIPI Channels (Note 3)	I_{ON} = −10 mA, $\overline{OE}$ = 0 V, SEL = V_{CC} or 0 V, CLKA, CLKB, DBn or DAn = 0, 0.6, 1.2 V	1.8		2.09		Ω
			2.5		1.19		
			3.6		0.46		
			4.5		0.08		
$I_{NO(OFF)}$, $I_{NC(OFF)}$	OFF Leakage Current (CLKAn, DAn, CLKBn, DBn)	CLKn, Dn = 0.3 V, V_{CC} – 0.3 V, CLKAn, DAn, or CLKBn; DBn = V_{CC} – 0.3 V, 0.3 V or Floating; $\overline{OE}$ = 0 V	1.65 – 4.5			±100	nA
$I_{A(ON)}$	ON Leakage Current of Common Ports (CLKn, Dn)	CLKn, Dn = 0.3 V, V_{CC} – 0.3 V, CLKAn, DAn, or CLKBn; DBn = V_{CC} – 0.3 V, 0.3 V or Floating; $\overline{OE}$ = 0 V	1.65 – 4.5			±100	nA
V_{IK}	Clamp Diode Voltage	I_{IN} = −18 mA	2.8			−1.2	V
I_{OZ}	Off−State Leakage Current	0 ≤ CLKn, Dn, CLKAn, CLKBn, DAn, DBn ≤ 3.6 V; $\overline{OE}$ = High	4.5			±100	nA
SUPPLY CURRENTS							
I_{CCZ}	Quiescent Hi−Z Supply Current	V_{IN} = 0 or V_{CC}, I_{OUT} = 0	4.5			0.5	μA
I_{CC}	Quiescent Supply Current	V_{IN} = 0 or V_{CC}, I_{OUT} = 0	2.5 to 4.5			55	μA
			1.8			30	
I_{CCT}	Increase in I_{CC} Current per Control Voltage and V_{CC}	V_{SEL}, V($\overline{OE}$) = 1.65 V	4.5			4.0	μA
			2.5	0.1		1.0	

2. Measured by the voltage drop between A and B pins at the indicated current through the switch. ON resistance is determined by the lower of the voltage on the two (A or B ports).
3. Guaranteed by characterization.

AC ELECTRICAL CHARACTERISTICS All typical values are for V_{CC} = 3.3 V at T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	V_{CC} (V)	T_A = −40°C to +85°C			Unit
				Min	Typ	Max	
t_{INIT}	Initialization Time	R_L = 50 Ω, C_L = 5 pF, V_{IS} = 1.2 V	2.5 to 4.5	100			μs
	V_{CC} to Output (Notes 4, 5)	Figure 4	1.8	150			
t_{EN}	Enable Turn−On Time	R_L = 50 Ω, C_L = 5 pF, V_{IS} = 1.2 V	2.5 to 4.5		120	200	μs
	$\overline{OE}$ to Output	Figure 5	1.8		250	500	
t_{DIS}	Disable Turn−Off Time	R_L = 50 Ω, C_L = 5 pF, V_{IS} = 1.2 V	2.5 to 4.5		25	50	ns
	$\overline{OE}$ to Output	Figure 5	1.8		50	90	
t_{ON}	Turn−On Time	R_L = 50 Ω, C_L = 5 pF, V_{IS} = 1.2 V	2.5 to 4.5		50	100	ns
	SEL to Output	Figure 5	1.8		75	125	
t_{OFF}	Turn−Off Time	R_L = 50 Ω, C_L = 5 pF, V_{IS} = 1.2 V	2.5 to 4.5		50	200	ns
	SEL to Output	Figure 5	1.8		200	325	
t_{BBM}	Break−Before−Make Time	R_L = 50 Ω, C_L = 5 pF, V_{IS} = 1.2 V Figure 6		10	50		ns
O_{IRR}	Off−Isolation for MIPI (Note 4)	R_L = 50 Ω, f = 750 MHz, $\overline{OE}$ = V_{CC}, V_{IS} = −1 dBm (200 mV_{PP})	1.65 to 4.5		−27		dB
X_{TALK}	Crosstalk for MIPI (Note 4)	R_L = 50 Ω, f = 750 MHz, V_{IS} = −1 dBm (200 mV_{PP})	1.65 to 4.5		−28		dB
BW	−3 dB Bandwidth (Note 4)	R_L = 50 Ω, C_L = 0 pF	3.0	900	1050		MHz
S_{DD21}	Differential Data Rate	Inter−Operability Data Rate	3.0		1.5		Gbps

4. Guaranteed by characterization.
5. Wait time required after V_{CC} power−up to operating level before data access is valid.

HIGH SPEED−RELATED AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = −40°C to +85°C			Unit
				Min	Typ	Max	
$t_{SK(O)}$	Channel−to−Channel Single−Ended Skew (Note 6)	TDR−Based Method (V_{IS} = 0.2 V_{PP}, C_L = C_{ON}) Figure 7	3.3		63	67	ps
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output (Note 6)	TDR−Based Method (V_{IS} = 0.2 V_{PP}, C_L = C_{ON}) Figure 8	3.3		17	31	ps

6. Guaranteed by characterization.

CAPACITANCE

Symbol	Parameter	Condition	V_{CC} (V)	T_A = −40°C to +85°C			Unit
				Min	Typ	Max	
C_{IN}	Control Pin Input Capacitance	V_{CC} = 0 V, f = 1 MHz	3.3		14.9		pF
C_{ON}	Out ON Capacitance	V_{CC} = 3.3 V, $\overline{OE}$ = 0 V, f = 1 MHz	3.3		12.6		pF
C_{OFF}	Out OFF Capacitance	V_{CC} = 3.3 V, $\overline{OE}$ = 3.3 V, f = 1 MHz	3.3		7.4		pF

Timing Diagrams

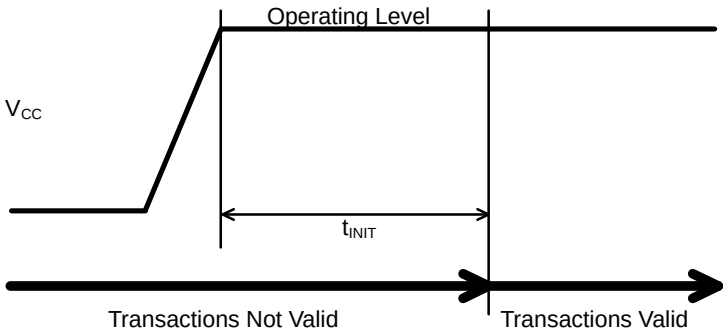


Figure 4. t_{INIT}, Initialization Time

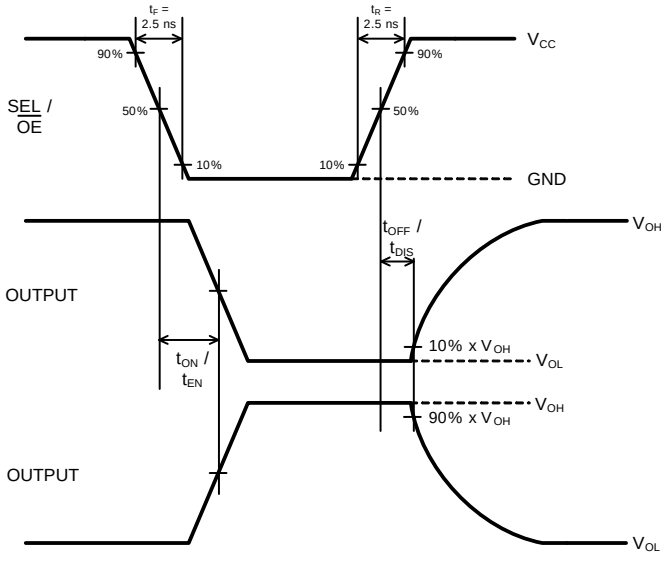


Figure 5. t_{EN}, t_{DIS}, t_{ON}, t_{OFF} Times

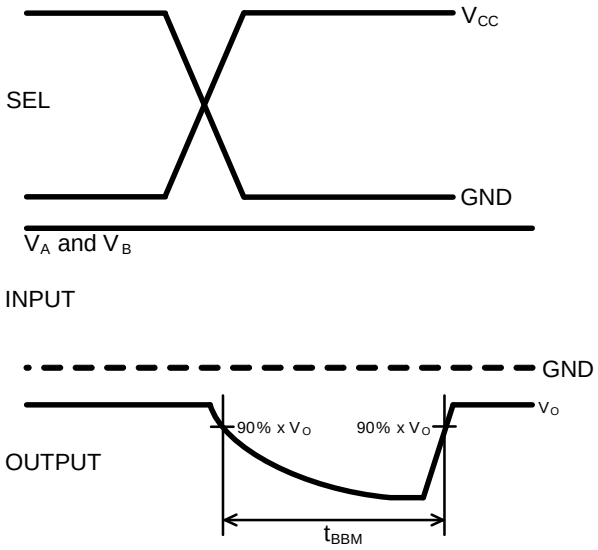


Figure 6. t_{BBM}, Break−Before−Make Time

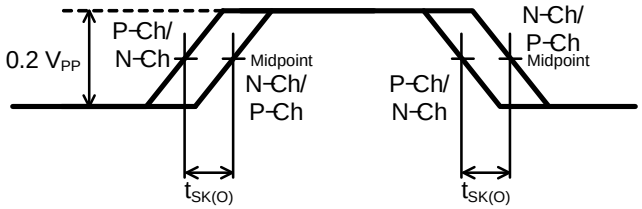


Figure 7. $t_{SK(O)}$, Channel−to−Channel Single−Ended

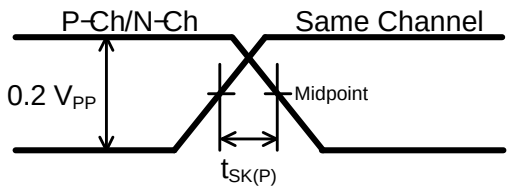


Figure 8. $t_{SK(P)}$, Same Channel Opposite Transitions

Eye Diagrams

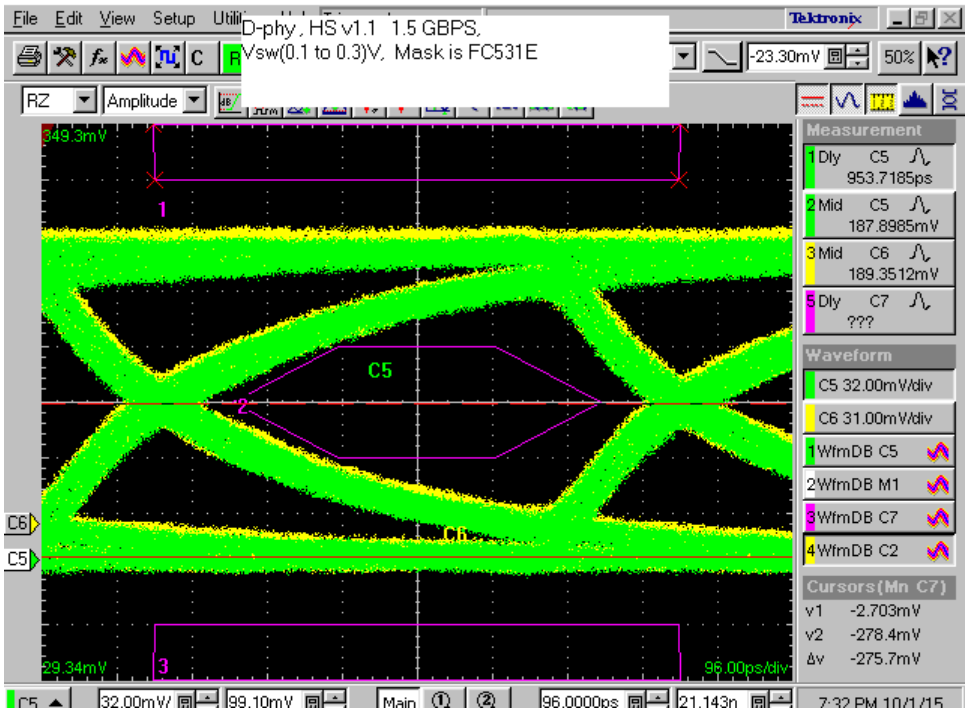


Figure 9. D−PHY HS 1.5 Gbps with Eye Mask

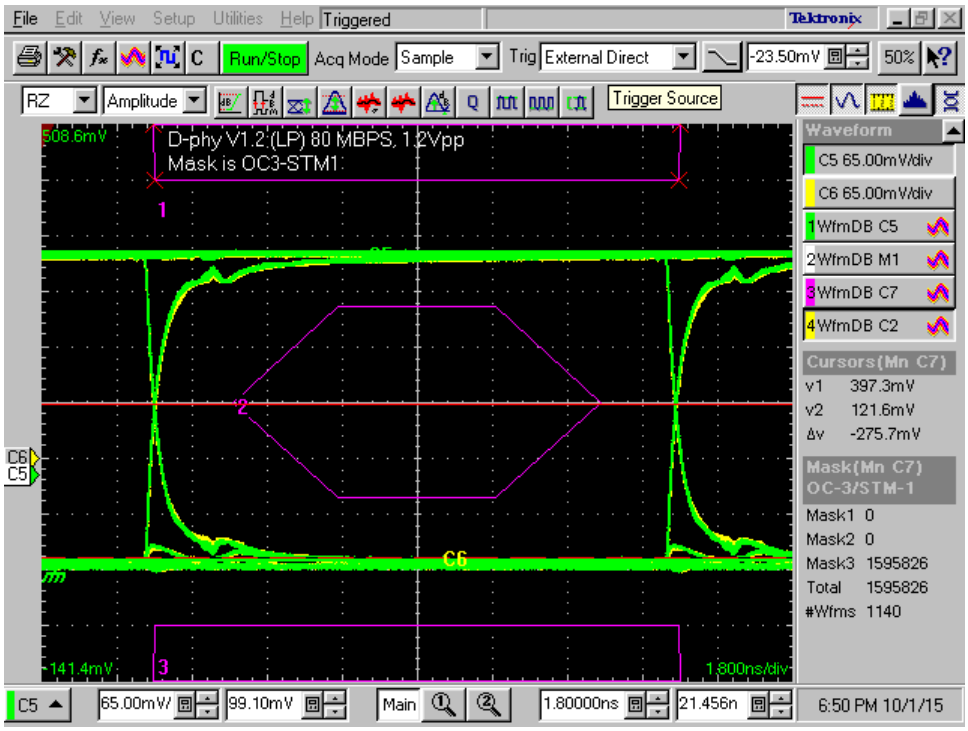


Figure 10. D−PHY LP 80 Mbps with Eye Mask

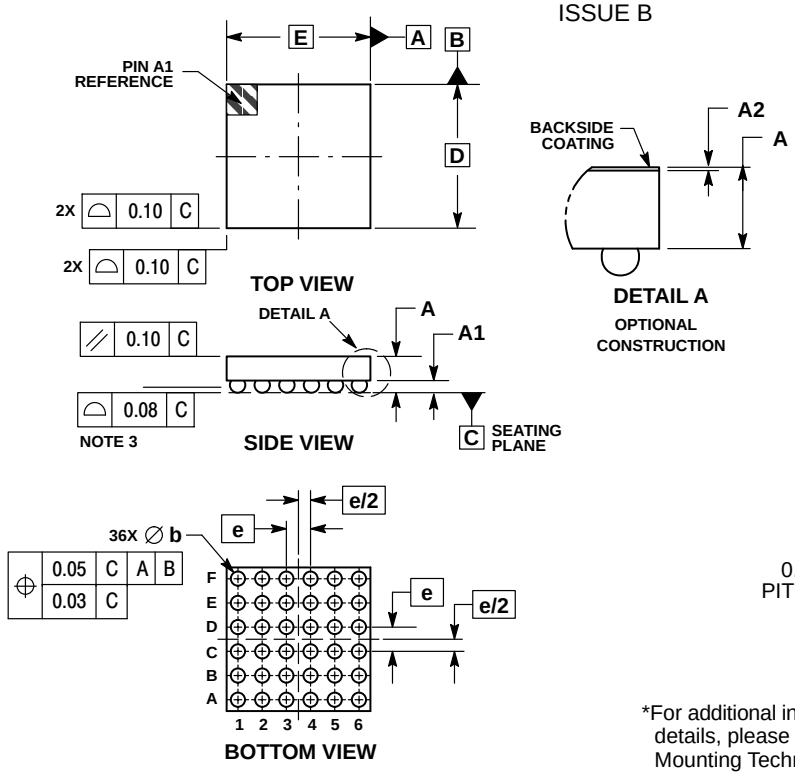
DEVICE ORDERING INFORMATION

Device Order Number	Device Code	Package Type	Tape & Reel Size†
NL3HS644FCTAG	3HS644	36−ball WLCSP (Pb−Free)	3000 / Tape & Reel
NL3HS644BFCTAG (Backside Coated)	HS644B	36−ball WLCSP (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

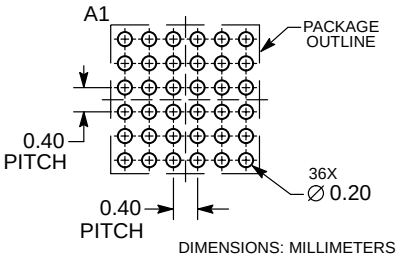
WLCSP36 2.34x2.34
CASE 567LR
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.54
A1	0.17	0.23
A2	0.00	0.027
b	0.24	0.30
D	2.34 BSC	
E	2.34 BSC	
e	0.40 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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