Sitronix

ST7565R

65 x 132 Dot Matrix LCD Controller/Driver

Features

- Directly display RAM data through Display Data RAM.
- RAM capacity : 65 x 132 = 8580 bits
- Display duty selectable by select pin
  1/65 duty : 65 common x 132 segment
  1/49 duty : 49 common x 132 segment
  1/33 duty : 33 common x 132 segment
  1/55 duty : 55 common x 132 segment
  1/53 duty : 53 common x 132 segment
- High-speed 8-bit MPU interface:
  ST7565R can be connected directly to both the 80x86 series MPUs and the 6800 series MPUs.
  Serial interface (SPI-4) is also supported.
- Abundant command functions
  Display data Read/Write, display ON/OFF, Normal/ Reverse display mode, page address set, display start line set, column address set, status read, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction selects, power saver, common output status select, V_0 voltage regulation internal resistor ratio set.
- Embedded analog power supply circuits for Liquid Crystal driving: Booster, Regulator and Follower.
- Embedded Booster circuit:
  2X,3X,4X,5X and 6X boost ratios are supported.
  Independent input (V_{DD2}) for boost reference voltage.
- High-accuracy Regulator circuit:
  Build-in Electronic volume function for the contrast control. Thermal gradient = –0.05%/°C.
- Embedded voltage Follower circuit for LCD driving.
- Embedded R-C oscillator circuit.
  The external clock is also supported.
- Extremely low power consumption: 60uA, bare dice (using the internal power). Settings:
  $V_{DD} – V_{SS} = V_{DD2} – V_{SS}$ =3.0 V, Booster Ratio=4,
  $V_0 – V_{SS}$ = 11.0 V. Display OFF and the normal mode is selected.
- Logic power supply : $V_{DD} – V_{SS}$ = 2.4V to 3.3 V
  Analog Power (Boost reference voltage):
  $V_{DD2} – V_{SS}$ = 2.4V to 3.3V
  Booster maximum voltage limited
  VOUT= 13.5V
  Liquid crystal drive power supply:
  $V_0 – V_{SS}$ = 3.0V to 12.0 V
- Wide range of operating temperatures: –30 to 85°C
- Package type: COG only.
- The chip is not designed to resist the light or to resist the radiation.
- Support LCD Module Size up to 2"

General Description

The ST7565R is a single-chip dot matrix LCD driver that can be connected directly to a microprocessor bus. 8-bit parallel or 4-line SPI display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a LCD drive signal independent of the microprocessor. Because the chips in the ST7565R contain 65x132 bits of display data RAM and there is a 1-to-1 correspondence between the LCD panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom.
The ST7565R chips contain 65 common output circuits and 132 segment output circuits, so that a single chip can drive a 65x132 dot display (capable of displaying 8 columns x4 rows of a 16x16 dot kanji font).

The ST7565R chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power LCD driver power supply, resistors for LCD driver power voltage adjustment and a display clock CR oscillator circuit, the ST7565R can be used to create the lowest power display system with the fewest components for high-performance portable devices.

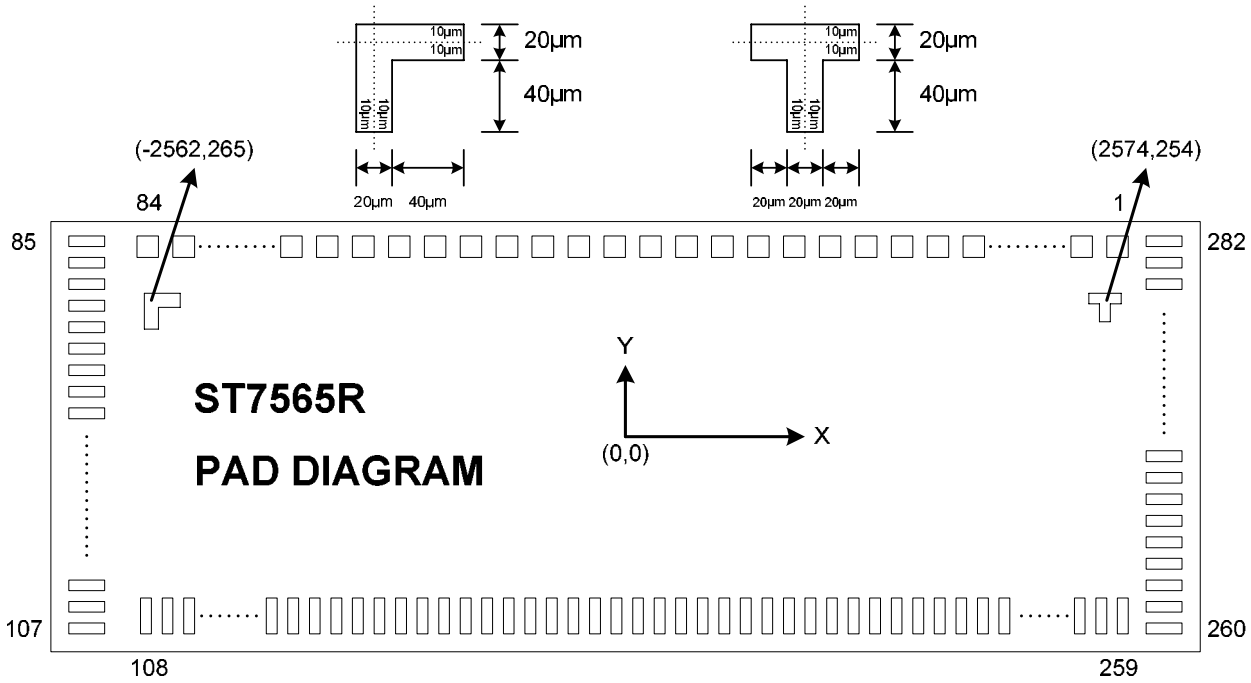
PART NO.	VRS temperature gradient	VRS range
ST7565R	-0.05%/°C	2.1V ±0.03V

ST7565R Pad Arrangement (COG)

Chip Size: 5900µm x 1000µm
Bump Pitch: 34µm(Min.)
Bump Size:

PAD No. 001	067	42µm x 54µm
PAD No. 068	073	56µm x 54µm
PAD No. 074	084	42µm x 54µm
PAD No. 085	282	17µm x 118µm

Bump Height: 15µm
Chip Thickness: 480µm



- **Recommend panel size is small than 1.8" (A.A.).**

Pad Center Coordinates (1/65 Duty)

Units: µm

PAD No.	PIN Name	X	Y
1	TEST[6]	2575	392
2	FR	2515	392
3	CL	2455	392
4	DOF	2395	392
5	VSS	2335	392
6	CS1B	2275	392
7	CS2	2215	392
8	VDD	2155	392
9	RST	2095	392
10	A0	2035	392
11	VSS	1975	392
12	/WR(R/W)	1915	392
13	/RD(E)	1855	392
14	VDD	1795	392
15	D0	1735	392
16	D1	1675	392
17	D2	1615	392
18	D3	1555	392
19	D4	1495	392
20	D5	1435	392
21	D6	1375	392
22	D7	1315	392
23	VDD	1255	392
24	VDD2	1195	392
25	VDD2	1135	392
26	VSS	1075	392
27	VSS	1015	392
28	VSS	955	392
29	VSS	895	392
30	VOUT	821	392
31	VOUT	761	392
32	CAP5P	701	392
33	CAP5P	641	392
34	CAP1N	581	392
35	CAP1N	521	392
36	CAP3P	461	392
37	CAP3P	401	392
38	CAP1N	341	392
39	CAP1N	281	392
40	CAP1P	221	392
41	CAP1P	161	392
42	CAP2P	101	392
43	CAP2P	41	392
44	CAP2N	-19	392
45	CAP2N	-79	392
46	CAP4P	-139	392
47	CAP4P	-199	392
48	VSS	-273	392

PAD No.	PIN Name	X	Y
49	VSS	-333	392
50	VRS	-408	392
51	VRS	-468	392
52	VDD2	-542	392
53	VDD	-602	392
54	V4	-676	392
55	V4	-736	392
56	V3	-796	392
57	V3	-856	392
58	V2	-916	392
59	V2	-976	392
60	V1	-1036	392
61	V1	-1096	392
62	V_0	-1156	392
63	V_0	-1216	392
64	VR	-1276	392
65	VR	-1336	392
66	VDD	-1410	392
67	VDD2	-1470	392
68	TEST[0]	-1537	392
69	TEST[1]	-1611	392
70	TEST[2]	-1685	392
71	TEST[3]	-1759	392
72	TEST[4]	-1833	392
73	TEST[5]	-1907	392
74	VDD	-1974	392
75	TEST[7]	-2034	392
76	CLS	-2094	392
77	C86	-2154	392
78	PSB	-2214	392
79	HPMB	-2274	392
80	IRS	-2334	392
81	SEL1	-2394	392
82	SEL2	-2454	392
83	SEL3	-2514	392
84	VSS	-2574	392
85	COM[31]	-2810	373
86	COM[30]	-2810	339
87	COM[29]	-2810	305
88	COM[28]	-2810	271
89	COM[27]	-2810	237
90	COM[26]	-2810	203
91	COM[25]	-2810	169
92	COM[24]	-2810	135
93	COM[23]	-2810	101
94	COM[22]	-2810	67
95	COM[21]	-2810	33
96	COM[20]	-2810	-1

PAD No.	PIN Name	X	Y
97	COM[19]	-2810	-35
98	COM[18]	-2810	-69
99	COM[17]	-2810	-103
100	COM[16]	-2810	-137
101	COM[15]	-2810	-171
102	COM[14]	-2810	-205
103	COM[13]	-2810	-239
104	COM[12]	-2810	-273
105	COM[11]	-2810	-307
106	COM[10]	-2810	-341
107	COM[9]	-2810	-375
108	COM[8]	-2573	-360
109	COM[7]	-2539	-360
110	COM[6]	-2505	-360
111	COM[5]	-2471	-360
112	COM[4]	-2437	-360
113	COM[3]	-2403	-360
114	COM[2]	-2369	-360
115	COM[1]	-2335	-360
116	COM[0]	-2301	-360
117	COMS2	-2267	-360
118	SEG[0]	-2227	-360
119	SEG[1]	-2193	-360
120	SEG[2]	-2159	-360
121	SEG[3]	-2125	-360
122	SEG[4]	-2091	-360
123	SEG[5]	-2057	-360
124	SEG[6]	-2023	-360
125	SEG[7]	-1989	-360
126	SEG[8]	-1955	-360
127	SEG[9]	-1921	-360
128	SEG[10]	-1887	-360
129	SEG[11]	-1853	-360
130	SEG[12]	-1819	-360
131	SEG[13]	-1785	-360
132	SEG[14]	-1751	-360
133	SEG[15]	-1717	-360
134	SEG[16]	-1683	-360
135	SEG[17]	-1649	-360
136	SEG[18]	-1615	-360
137	SEG[19]	-1581	-360
138	SEG[20]	-1547	-360
139	SEG[21]	-1513	-360
140	SEG[22]	-1479	-360
141	SEG[23]	-1445	-360
142	SEG[24]	-1411	-360
143	SEG[25]	-1377	-360
144	SEG[26]	-1343	-360
145	SEG[27]	-1309	-360
146	SEG[28]	-1275	-360
147	SEG[29]	-1241	-360
148	SEG[30]	-1207	-360

PAD No.	PIN Name	X	Y
149	SEG[31]	-1173	-360
150	SEG[32]	-1139	-360
151	SEG[33]	-1105	-360
152	SEG[34]	-1071	-360
153	SEG[35]	-1037	-360
154	SEG[36]	-1003	-360
155	SEG[37]	-969	-360
156	SEG[38]	-935	-360
157	SEG[39]	-901	-360
158	SEG[40]	-867	-360
159	SEG[41]	-833	-360
160	SEG[42]	-799	-360
161	SEG[43]	-765	-360
162	SEG[44]	-731	-360
163	SEG[45]	-697	-360
164	SEG[46]	-663	-360
165	SEG[47]	-629	-360
166	SEG[48]	-595	-360
167	SEG[49]	-561	-360
168	SEG[50]	-527	-360
169	SEG[51]	-493	-360
170	SEG[52]	-459	-360
171	SEG[53]	-425	-360
172	SEG[54]	-391	-360
173	SEG[55]	-357	-360
174	SEG[56]	-323	-360
175	SEG[57]	-289	-360
176	SEG[58]	-255	-360
177	SEG[59]	-221	-360
178	SEG[60]	-187	-360
179	SEG[61]	-153	-360
180	SEG[62]	-119	-360
181	SEG[63]	-85	-360
182	SEG[64]	-51	-360
183	SEG[65]	-17	-360
184	SEG[66]	17	-360
185	SEG[67]	51	-360
186	SEG[68]	85	-360
187	SEG[69]	119	-360
188	SEG[70]	153	-360
189	SEG[71]	187	-360
190	SEG[72]	221	-360
191	SEG[73]	255	-360
192	SEG[74]	289	-360
193	SEG[75]	323	-360
194	SEG[76]	357	-360
195	SEG[77]	391	-360
196	SEG[78]	425	-360
197	SEG[79]	459	-360
198	SEG[80]	493	-360
199	SEG[81]	527	-360
200	SEG[82]	561	-360

PAD No.	PIN Name	X	Y
201	SEG[83]	595	-360
202	SEG[84]	629	-360
203	SEG[85]	663	-360
204	SEG[86]	697	-360
205	SEG[87]	731	-360
206	SEG[88]	765	-360
207	SEG[89]	799	-360
208	SEG[90]	833	-360
209	SEG[91]	867	-360
210	SEG[92]	901	-360
211	SEG[93]	935	-360
212	SEG[94]	969	-360
213	SEG[95]	1003	-360
214	SEG[96]	1037	-360
215	SEG[97]	1071	-360
216	SEG[98]	1105	-360
217	SEG[99]	1139	-360
218	SEG[100]	1173	-360
219	SEG[101]	1207	-360
220	SEG[102]	1241	-360
221	SEG[103]	1275	-360
222	SEG[104]	1309	-360
223	SEG[105]	1343	-360
224	SEG[106]	1377	-360
225	SEG[107]	1411	-360
226	SEG[108]	1445	-360
227	SEG[109]	1479	-360
228	SEG[110]	1513	-360
229	SEG[111]	1547	-360
230	SEG[112]	1581	-360
231	SEG[113]	1615	-360
232	SEG[114]	1649	-360
233	SEG[115]	1683	-360
234	SEG[116]	1717	-360
235	SEG[117]	1751	-360
236	SEG[118]	1785	-360
237	SEG[119]	1819	-360
238	SEG[120]	1853	-360
239	SEG[121]	1887	-360
240	SEG[122]	1921	-360
241	SEG[123]	1955	-360
242	SEG[124]	1989	-360
243	SEG[125]	2023	-360
244	SEG[126]	2057	-360
245	SEG[127]	2091	-360

PAD No.	PIN Name	X	Y
246	SEG[128]	2125	-360
247	SEG[129]	2159	-360
248	SEG[130]	2193	-360
249	SEG[131]	2227	-360
250	COM[32]	2267	-360
251	COM[33]	2301	-360
252	COM[34]	2335	-360
253	COM[35]	2369	-360
254	COM[36]	2403	-360
255	COM[37]	2437	-360
256	COM[38]	2471	-360
257	COM[39]	2505	-360
258	COM[40]	2539	-360
259	COM[41]	2573	-360
260	COM[42]	2810	-375
261	COM[43]	2810	-341
262	COM[44]	2810	-307
263	COM[45]	2810	-273
264	COM[46]	2810	-239
265	COM[47]	2810	-205
266	COM[48]	2810	-171
267	COM[49]	2810	-137
268	COM[50]	2810	-103
269	COM[51]	2810	-69
270	COM[52]	2810	-35
271	COM[53]	2810	-1
272	COM[54]	2810	33
273	COM[55]	2810	67
274	COM[56]	2810	101
275	COM[57]	2810	135
276	COM[58]	2810	169
277	COM[59]	2810	203
278	COM[60]	2810	237
279	COM[61]	2810	271
280	COM[62]	2810	305
281	COM[63]	2810	339
282	COMS1	2810	373

Pad Center Coordinates (1/49 Duty)

Units: µm

PAD No.	PIN Name	X	Y
1	TEST[6]	2575	392
2	FR	2515	392
3	CL	2455	392
4	DOF	2395	392
5	VSS	2335	392
6	CS1B	2275	392
7	CS2	2215	392
8	VDD	2155	392
9	RST	2095	392
10	A0	2035	392
11	VSS	1975	392
12	/WR(R/W)	1915	392
13	/RD(E)	1855	392
14	VDD	1795	392
15	D0	1735	392
16	D1	1675	392
17	D2	1615	392
18	D3	1555	392
19	D4	1495	392
20	D5	1435	392
21	D6	1375	392
22	D7	1315	392
23	VDD	1255	392
24	VDD2	1195	392
25	VDD2	1135	392
26	VSS	1075	392
27	VSS	1015	392
28	VSS	955	392
29	VSS	895	392
30	VOUT	821	392
31	VOUT	761	392
32	CAP5P	701	392
33	CAP5P	641	392
34	CAP1N	581	392
35	CAP1N	521	392
36	CAP3P	461	392
37	CAP3P	401	392
38	CAP1N	341	392
39	CAP1N	281	392
40	CAP1P	221	392
41	CAP1P	161	392
42	CAP2P	101	392
43	CAP2P	41	392
44	CAP2N	-19	392
45	CAP2N	-79	392
46	CAP4P	-139	392
47	CAP4P	-199	392
48	VSS	-273	392
49	VSS	-333	392

PAD No.	PIN Name	X	Y
50	VRS	-408	392
51	VRS	-468	392
52	VDD2	-542	392
53	VDD	-602	392
54	V4	-676	392
55	V4	-736	392
56	V3	-796	392
57	V3	-856	392
58	V2	-916	392
59	V2	-976	392
60	V1	-1036	392
61	V1	-1096	392
62	V_0	-1156	392
63	V_0	-1216	392
64	VR	-1276	392
65	VR	-1336	392
66	VDD	-1410	392
67	VDD2	-1470	392
68	TEST[0]	-1537	392
69	TEST[1]	-1611	392
70	TEST[2]	-1685	392
71	TEST[3]	-1759	392
72	TEST[4]	-1833	392
73	TEST[5]	-1907	392
74	VDD	-1974	392
75	TEST[7]	-2034	392
76	CLS	-2094	392
77	C86	-2154	392
78	PSB	-2214	392
79	HPMB	-2274	392
80	IRS	-2334	392
81	SEL1	-2394	392
82	SEL2	-2454	392
83	SEL3	-2514	392
84	VSS	-2574	392
85	Reserve	-2810	373
86	Reserve	-2810	339
87	Reserve	-2810	305
88	Reserve	-2810	271
89	Reserve	-2810	237
90	Reserve	-2810	203
91	Reserve	-2810	169
92	Reserve	-2810	135
93	COM[23]	-2810	101
94	COM[22]	-2810	67
95	COM[21]	-2810	33
96	COM[20]	-2810	-1
97	COM[19]	-2810	-35
98	COM[18]	-2810	-69

PAD No.	PIN Name	X	Y
99	COM[17]	-2810	-103
100	COM[16]	-2810	-137
101	COM[15]	-2810	-171
102	COM[14]	-2810	-205
103	COM[13]	-2810	-239
104	COM[12]	-2810	-273
105	COM[11]	-2810	-307
106	COM[10]	-2810	-341
107	COM[9]	-2810	-375
108	COM[8]	-2573	-360
109	COM[7]	-2539	-360
110	COM[6]	-2505	-360
111	COM[5]	-2471	-360
112	COM[4]	-2437	-360
113	COM[3]	-2403	-360
114	COM[2]	-2369	-360
115	COM[1]	-2335	-360
116	COM[0]	-2301	-360
117	COMS2	-2267	-360
118	SEG[0]	-2227	-360
119	SEG[1]	-2193	-360
120	SEG[2]	-2159	-360
121	SEG[3]	-2125	-360
122	SEG[4]	-2091	-360
123	SEG[5]	-2057	-360
124	SEG[6]	-2023	-360
125	SEG[7]	-1989	-360
126	SEG[8]	-1955	-360
127	SEG[9]	-1921	-360
128	SEG[10]	-1887	-360
129	SEG[11]	-1853	-360
130	SEG[12]	-1819	-360
131	SEG[13]	-1785	-360
132	SEG[14]	-1751	-360
133	SEG[15]	-1717	-360
134	SEG[16]	-1683	-360
135	SEG[17]	-1649	-360
136	SEG[18]	-1615	-360
137	SEG[19]	-1581	-360
138	SEG[20]	-1547	-360
139	SEG[21]	-1513	-360
140	SEG[22]	-1479	-360
141	SEG[23]	-1445	-360
142	SEG[24]	-1411	-360
143	SEG[25]	-1377	-360
144	SEG[26]	-1343	-360
145	SEG[27]	-1309	-360
146	SEG[28]	-1275	-360
147	SEG[29]	-1241	-360
148	SEG[30]	-1207	-360
149	SEG[31]	-1173	-360
150	SEG[32]	-1139	-360

PAD No.	PIN Name	X	Y
151	SEG[33]	-1105	-360
152	SEG[34]	-1071	-360
153	SEG[35]	-1037	-360
154	SEG[36]	-1003	-360
155	SEG[37]	-969	-360
156	SEG[38]	-935	-360
157	SEG[39]	-901	-360
158	SEG[40]	-867	-360
159	SEG[41]	-833	-360
160	SEG[42]	-799	-360
161	SEG[43]	-765	-360
162	SEG[44]	-731	-360
163	SEG[45]	-697	-360
164	SEG[46]	-663	-360
165	SEG[47]	-629	-360
166	SEG[48]	-595	-360
167	SEG[49]	-561	-360
168	SEG[50]	-527	-360
169	SEG[51]	-493	-360
170	SEG[52]	-459	-360
171	SEG[53]	-425	-360
172	SEG[54]	-391	-360
173	SEG[55]	-357	-360
174	SEG[56]	-323	-360
175	SEG[57]	-289	-360
176	SEG[58]	-255	-360
177	SEG[59]	-221	-360
178	SEG[60]	-187	-360
179	SEG[61]	-153	-360
180	SEG[62]	-119	-360
181	SEG[63]	-85	-360
182	SEG[64]	-51	-360
183	SEG[65]	-17	-360
184	SEG[66]	17	-360
185	SEG[67]	51	-360
186	SEG[68]	85	-360
187	SEG[69]	119	-360
188	SEG[70]	153	-360
189	SEG[71]	187	-360
190	SEG[72]	221	-360
191	SEG[73]	255	-360
192	SEG[74]	289	-360
193	SEG[75]	323	-360
194	SEG[76]	357	-360
195	SEG[77]	391	-360
196	SEG[78]	425	-360
197	SEG[79]	459	-360
198	SEG[80]	493	-360
199	SEG[81]	527	-360
200	SEG[82]	561	-360
201	SEG[83]	595	-360
202	SEG[84]	629	-360

PAD No.	PIN Name	X	Y
203	SEG[85]	663	-360
204	SEG[86]	697	-360
205	SEG[87]	731	-360
206	SEG[88]	765	-360
207	SEG[89]	799	-360
208	SEG[90]	833	-360
209	SEG[91]	867	-360
210	SEG[92]	901	-360
211	SEG[93]	935	-360
212	SEG[94]	969	-360
213	SEG[95]	1003	-360
214	SEG[96]	1037	-360
215	SEG[97]	1071	-360
216	SEG[98]	1105	-360
217	SEG[99]	1139	-360
218	SEG[100]	1173	-360
219	SEG[101]	1207	-360
220	SEG[102]	1241	-360
221	SEG[103]	1275	-360
222	SEG[104]	1309	-360
223	SEG[105]	1343	-360
224	SEG[106]	1377	-360
225	SEG[107]	1411	-360
226	SEG[108]	1445	-360
227	SEG[109]	1479	-360
228	SEG[110]	1513	-360
229	SEG[111]	1547	-360
230	SEG[112]	1581	-360
231	SEG[113]	1615	-360
232	SEG[114]	1649	-360
233	SEG[115]	1683	-360
234	SEG[116]	1717	-360
235	SEG[117]	1751	-360
236	SEG[118]	1785	-360
237	SEG[119]	1819	-360
238	SEG[120]	1853	-360
239	SEG[121]	1887	-360
240	SEG[122]	1921	-360
241	SEG[123]	1955	-360
242	SEG[124]	1989	-360
243	SEG[125]	2023	-360
244	SEG[126]	2057	-360
245	SEG[127]	2091	-360

PAD No.	PIN Name	X	Y
246	SEG[128]	2125	-360
247	SEG[129]	2159	-360
248	SEG[130]	2193	-360
249	SEG[131]	2227	-360
250	Reserve	2267	-360
251	Reserve	2301	-360
252	Reserve	2335	-360
253	Reserve	2369	-360
254	Reserve	2403	-360
255	Reserve	2437	-360
256	Reserve	2471	-360
257	Reserve	2505	-360
258	COM[24]	2539	-360
259	COM[25]	2573	-360
260	COM[26]	2810	-375
261	COM[27]	2810	-341
262	COM[28]	2810	-307
263	COM[29]	2810	-273
264	COM[30]	2810	-239
265	COM[31]	2810	-205
266	COM[32]	2810	-171
267	COM[33]	2810	-137
268	COM[34]	2810	-103
269	COM[35]	2810	-69
270	COM[36]	2810	-35
271	COM[37]	2810	-1
272	COM[38]	2810	33
273	COM[39]	2810	67
274	COM[40]	2810	101
275	COM[41]	2810	135
276	COM[42]	2810	169
277	COM[43]	2810	203
278	COM[44]	2810	237
279	COM[45]	2810	271
280	COM[46]	2810	305
281	COM[47]	2810	339
282	COMS1	2810	373

Pad Center Coordinates (1/33 Duty)

Units: µm

PAD No.	PIN Name	X	Y
1	TEST[6]	2575	392
2	FR	2515	392
3	CL	2455	392
4	DOF	2395	392
5	VSS	2335	392
6	CS1B	2275	392
7	CS2	2215	392
8	VDD	2155	392
9	RST	2095	392
10	A0	2035	392
11	VSS	1975	392
12	/WR(R/W)	1915	392
13	/RD(E)	1855	392
14	VDD	1795	392
15	D0	1735	392
16	D1	1675	392
17	D2	1615	392
18	D3	1555	392
19	D4	1495	392
20	D5	1435	392
21	D6	1375	392
22	D7	1315	392
23	VDD	1255	392
24	VDD2	1195	392
25	VDD2	1135	392
26	VSS	1075	392
27	VSS	1015	392
28	VSS	955	392
29	VSS	895	392
30	VOUT	821	392
31	VOUT	761	392
32	CAP5P	701	392
33	CAP5P	641	392
34	CAP1N	581	392
35	CAP1N	521	392
36	CAP3P	461	392
37	CAP3P	401	392
38	CAP1N	341	392
39	CAP1N	281	392
40	CAP1P	221	392
41	CAP1P	161	392
42	CAP2P	101	392
43	CAP2P	41	392
44	CAP2N	-19	392
45	CAP2N	-79	392
46	CAP4P	-139	392
47	CAP4P	-199	392
48	VSS	-273	392
49	VSS	-333	392

PAD No.	PIN Name	X	Y
50	VRS	-408	392
51	VRS	-468	392
52	VDD2	-542	392
53	VDD	-602	392
54	V4	-676	392
55	V4	-736	392
56	V3	-796	392
57	V3	-856	392
58	V2	-916	392
59	V2	-976	392
60	V1	-1036	392
61	V1	-1096	392
62	V_0	-1156	392
63	V_0	-1216	392
64	VR	-1276	392
65	VR	-1336	392
66	VDD	-1410	392
67	VDD2	-1470	392
68	TEST[0]	-1537	392
69	TEST[1]	-1611	392
70	TEST[2]	-1685	392
71	TEST[3]	-1759	392
72	TEST[4]	-1833	392
73	TEST[5]	-1907	392
74	VDD	-1974	392
75	TEST[7]	-2034	392
76	CLS	-2094	392
77	C86	-2154	392
78	PSB	-2214	392
79	HPMB	-2274	392
80	IRS	-2334	392
81	SEL1	-2394	392
82	SEL2	-2454	392
83	SEL3	-2514	392
84	VSS	-2574	392
85	Reserve	-2810	373
86	Reserve	-2810	339
87	Reserve	-2810	305
88	Reserve	-2810	271
89	Reserve	-2810	237
90	Reserve	-2810	203
91	Reserve	-2810	169
92	Reserve	-2810	135
93	Reserve	-2810	101
94	Reserve	-2810	67
95	RESERVED	-2810	33
96	RESERVED	-2810	-1
97	RESERVED	-2810	-35
98	RESERVED	-2810	-69

PAD No.	PIN Name	X	Y
99	RESERVED	-2810	-103
100	RESERVED	-2810	-137
101	COM[15]	-2810	-171
102	COM[14]	-2810	-205
103	COM[13]	-2810	-239
104	COM[12]	-2810	-273
105	COM[11]	-2810	-307
106	COM[10]	-2810	-341
107	COM[9]	-2810	-375
108	COM[8]	-2573	-360
109	COM[7]	-2539	-360
110	COM[6]	-2505	-360
111	COM[5]	-2471	-360
112	COM[4]	-2437	-360
113	COM[3]	-2403	-360
114	COM[2]	-2369	-360
115	COM[1]	-2335	-360
116	COM[0]	-2301	-360
117	COMS2	-2267	-360
118	SEG[0]	-2227	-360
119	SEG[1]	-2193	-360
120	SEG[2]	-2159	-360
121	SEG[3]	-2125	-360
122	SEG[4]	-2091	-360
123	SEG[5]	-2057	-360
124	SEG[6]	-2023	-360
125	SEG[7]	-1989	-360
126	SEG[8]	-1955	-360
127	SEG[9]	-1921	-360
128	SEG[10]	-1887	-360
129	SEG[11]	-1853	-360
130	SEG[12]	-1819	-360
131	SEG[13]	-1785	-360
132	SEG[14]	-1751	-360
133	SEG[15]	-1717	-360
134	SEG[16]	-1683	-360
135	SEG[17]	-1649	-360
136	SEG[18]	-1615	-360
137	SEG[19]	-1581	-360
138	SEG[20]	-1547	-360
139	SEG[21]	-1513	-360
140	SEG[22]	-1479	-360
141	SEG[23]	-1445	-360
142	SEG[24]	-1411	-360
143	SEG[25]	-1377	-360
144	SEG[26]	-1343	-360
145	SEG[27]	-1309	-360
146	SEG[28]	-1275	-360
147	SEG[29]	-1241	-360
148	SEG[30]	-1207	-360
149	SEG[31]	-1173	-360
150	SEG[32]	-1139	-360

PAD No.	PIN Name	X	Y
151	SEG[33]	-1105	-360
152	SEG[34]	-1071	-360
153	SEG[35]	-1037	-360
154	SEG[36]	-1003	-360
155	SEG[37]	-969	-360
156	SEG[38]	-935	-360
157	SEG[39]	-901	-360
158	SEG[40]	-867	-360
159	SEG[41]	-833	-360
160	SEG[42]	-799	-360
161	SEG[43]	-765	-360
162	SEG[44]	-731	-360
163	SEG[45]	-697	-360
164	SEG[46]	-663	-360
165	SEG[47]	-629	-360
166	SEG[48]	-595	-360
167	SEG[49]	-561	-360
168	SEG[50]	-527	-360
169	SEG[51]	-493	-360
170	SEG[52]	-459	-360
171	SEG[53]	-425	-360
172	SEG[54]	-391	-360
173	SEG[55]	-357	-360
174	SEG[56]	-323	-360
175	SEG[57]	-289	-360
176	SEG[58]	-255	-360
177	SEG[59]	-221	-360
178	SEG[60]	-187	-360
179	SEG[61]	-153	-360
180	SEG[62]	-119	-360
181	SEG[63]	-85	-360
182	SEG[64]	-51	-360
183	SEG[65]	-17	-360
184	SEG[66]	17	-360
185	SEG[67]	51	-360
186	SEG[68]	85	-360
187	SEG[69]	119	-360
188	SEG[70]	153	-360
189	SEG[71]	187	-360
190	SEG[72]	221	-360
191	SEG[73]	255	-360
192	SEG[74]	289	-360
193	SEG[75]	323	-360
194	SEG[76]	357	-360
195	SEG[77]	391	-360
196	SEG[78]	425	-360
197	SEG[79]	459	-360
198	SEG[80]	493	-360
199	SEG[81]	527	-360
200	SEG[82]	561	-360
201	SEG[83]	595	-360
202	SEG[84]	629	-360

PAD No.	PIN Name	X	Y
203	SEG[85]	663	-360
204	SEG[86]	697	-360
205	SEG[87]	731	-360
206	SEG[88]	765	-360
207	SEG[89]	799	-360
208	SEG[90]	833	-360
209	SEG[91]	867	-360
210	SEG[92]	901	-360
211	SEG[93]	935	-360
212	SEG[94]	969	-360
213	SEG[95]	1003	-360
214	SEG[96]	1037	-360
215	SEG[97]	1071	-360
216	SEG[98]	1105	-360
217	SEG[99]	1139	-360
218	SEG[100]	1173	-360
219	SEG[101]	1207	-360
220	SEG[102]	1241	-360
221	SEG[103]	1275	-360
222	SEG[104]	1309	-360
223	SEG[105]	1343	-360
224	SEG[106]	1377	-360
225	SEG[107]	1411	-360
226	SEG[108]	1445	-360
227	SEG[109]	1479	-360
228	SEG[110]	1513	-360
229	SEG[111]	1547	-360
230	SEG[112]	1581	-360
231	SEG[113]	1615	-360
232	SEG[114]	1649	-360
233	SEG[115]	1683	-360
234	SEG[116]	1717	-360
235	SEG[117]	1751	-360
236	SEG[118]	1785	-360
237	SEG[119]	1819	-360
238	SEG[120]	1853	-360
239	SEG[121]	1887	-360
240	SEG[122]	1921	-360
241	SEG[123]	1955	-360
242	SEG[124]	1989	-360
243	SEG[125]	2023	-360
244	SEG[126]	2057	-360
245	SEG[127]	2091	-360

PAD No.	PIN Name	X	Y
246	SEG[128]	2125	-360
247	SEG[129]	2159	-360
248	SEG[130]	2193	-360
249	SEG[131]	2227	-360
250	Reserve	2267	-360
251	Reserve	2301	-360
252	Reserve	2335	-360
253	Reserve	2369	-360
254	Reserve	2403	-360
255	Reserve	2437	-360
256	Reserve	2471	-360
257	Reserve	2505	-360
258	Reserve	2539	-360
259	Reserve	2573	-360
260	Reserve	2810	-375
261	Reserve	2810	-341
262	Reserve	2810	-307
263	Reserve	2810	-273
264	Reserve	2810	-239
265	Reserve	2810	-205
266	COM[16]	2810	-171
267	COM[17]	2810	-137
268	COM[18]	2810	-103
269	COM[19]	2810	-69
270	COM[20]	2810	-35
271	COM[21]	2810	-1
272	COM[22]	2810	33
273	COM[23]	2810	67
274	COM[24]	2810	101
275	COM[25]	2810	135
276	COM[26]	2810	169
277	COM[27]	2810	203
278	COM[28]	2810	237
279	COM[29]	2810	271
280	COM[30]	2810	305
281	COM[31]	2810	339
282	COMS1	2810	373

Pad Center Coordinates (1/55 Duty)

Units: µm

PAD No.	PIN Name	X	Y
1	TEST[6]	2575	392
2	FR	2515	392
3	CL	2455	392
4	DOF	2395	392
5	VSS	2335	392
6	CS1B	2275	392
7	CS2	2215	392
8	VDD	2155	392
9	RST	2095	392
10	A0	2035	392
11	VSS	1975	392
12	/WR(R/W)	1915	392
13	/RD(E)	1855	392
14	VDD	1795	392
15	D0	1735	392
16	D1	1675	392
17	D2	1615	392
18	D3	1555	392
19	D4	1495	392
20	D5	1435	392
21	D6	1375	392
22	D7	1315	392
23	VDD	1255	392
24	VDD2	1195	392
25	VDD2	1135	392
26	VSS	1075	392
27	VSS	1015	392
28	VSS	955	392
29	VSS	895	392
30	VOUT	821	392
31	VOUT	761	392
32	CAP5P	701	392
33	CAP5P	641	392
34	CAP1N	581	392
35	CAP1N	521	392
36	CAP3P	461	392
37	CAP3P	401	392
38	CAP1N	341	392
39	CAP1N	281	392
40	CAP1P	221	392
41	CAP1P	161	392
42	CAP2P	101	392
43	CAP2P	41	392
44	CAP2N	-19	392
45	CAP2N	-79	392
46	CAP4P	-139	392
47	CAP4P	-199	392
48	VSS	-273	392
49	VSS	-333	392

PAD No.	PIN Name	X	Y
50	VRS	-408	392
51	VRS	-468	392
52	VDD2	-542	392
53	VDD	-602	392
54	V4	-676	392
55	V4	-736	392
56	V3	-796	392
57	V3	-856	392
58	V2	-916	392
59	V2	-976	392
60	V1	-1036	392
61	V1	-1096	392
62	V_0	-1156	392
63	V_0	-1216	392
64	VR	-1276	392
65	VR	-1336	392
66	VDD	-1410	392
67	VDD2	-1470	392
68	TEST[0]	-1537	392
69	TEST[1]	-1611	392
70	TEST[2]	-1685	392
71	TEST[3]	-1759	392
72	TEST[4]	-1833	392
73	TEST[5]	-1907	392
74	VDD	-1974	392
75	TEST[7]	-2034	392
76	CLS	-2094	392
77	C86	-2154	392
78	PSB	-2214	392
79	HPMB	-2274	392
80	IRS	-2334	392
81	SEL1	-2394	392
82	SEL2	-2454	392
83	SEL3	-2514	392
84	VSS	-2574	392
85	Reserve	-2810	373
86	Reserve	-2810	339
87	Reserve	-2810	305
88	Reserve	-2810	271
89	Reserve	-2810	237
90	COM[26]	-2810	203
91	COM[25]	-2810	169
92	COM[24]	-2810	135
93	COM[23]	-2810	101
94	COM[22]	-2810	67
95	COM[21]	-2810	33
96	COM[20]	-2810	-1
97	COM[19]	-2810	-35
98	COM[18]	-2810	-69

PAD No.	PIN Name	X	Y
99	COM[17]	-2810	-103
100	COM[16]	-2810	-137
101	COM[15]	-2810	-171
102	COM[14]	-2810	-205
103	COM[13]	-2810	-239
104	COM[12]	-2810	-273
105	COM[11]	-2810	-307
106	COM[10]	-2810	-341
107	COM[9]	-2810	-375
108	COM[8]	-2573	-360
109	COM[7]	-2539	-360
110	COM[6]	-2505	-360
111	COM[5]	-2471	-360
112	COM[4]	-2437	-360
113	COM[3]	-2403	-360
114	COM[2]	-2369	-360
115	COM[1]	-2335	-360
116	COM[0]	-2301	-360
117	COMS2	-2267	-360
118	SEG[0]	-2227	-360
119	SEG[1]	-2193	-360
120	SEG[2]	-2159	-360
121	SEG[3]	-2125	-360
122	SEG[4]	-2091	-360
123	SEG[5]	-2057	-360
124	SEG[6]	-2023	-360
125	SEG[7]	-1989	-360
126	SEG[8]	-1955	-360
127	SEG[9]	-1921	-360
128	SEG[10]	-1887	-360
129	SEG[11]	-1853	-360
130	SEG[12]	-1819	-360
131	SEG[13]	-1785	-360
132	SEG[14]	-1751	-360
133	SEG[15]	-1717	-360
134	SEG[16]	-1683	-360
135	SEG[17]	-1649	-360
136	SEG[18]	-1615	-360
137	SEG[19]	-1581	-360
138	SEG[20]	-1547	-360
139	SEG[21]	-1513	-360
140	SEG[22]	-1479	-360
141	SEG[23]	-1445	-360
142	SEG[24]	-1411	-360
143	SEG[25]	-1377	-360
144	SEG[26]	-1343	-360
145	SEG[27]	-1309	-360
146	SEG[28]	-1275	-360
147	SEG[29]	-1241	-360
148	SEG[30]	-1207	-360
149	SEG[31]	-1173	-360
150	SEG[32]	-1139	-360

PAD No.	PIN Name	X	Y
151	SEG[33]	-1105	-360
152	SEG[34]	-1071	-360
153	SEG[35]	-1037	-360
154	SEG[36]	-1003	-360
155	SEG[37]	-969	-360
156	SEG[38]	-935	-360
157	SEG[39]	-901	-360
158	SEG[40]	-867	-360
159	SEG[41]	-833	-360
160	SEG[42]	-799	-360
161	SEG[43]	-765	-360
162	SEG[44]	-731	-360
163	SEG[45]	-697	-360
164	SEG[46]	-663	-360
165	SEG[47]	-629	-360
166	SEG[48]	-595	-360
167	SEG[49]	-561	-360
168	SEG[50]	-527	-360
169	SEG[51]	-493	-360
170	SEG[52]	-459	-360
171	SEG[53]	-425	-360
172	SEG[54]	-391	-360
173	SEG[55]	-357	-360
174	SEG[56]	-323	-360
175	SEG[57]	-289	-360
176	SEG[58]	-255	-360
177	SEG[59]	-221	-360
178	SEG[60]	-187	-360
179	SEG[61]	-153	-360
180	SEG[62]	-119	-360
181	SEG[63]	-85	-360
182	SEG[64]	-51	-360
183	SEG[65]	-17	-360
184	SEG[66]	17	-360
185	SEG[67]	51	-360
186	SEG[68]	85	-360
187	SEG[69]	119	-360
188	SEG[70]	153	-360
189	SEG[71]	187	-360
190	SEG[72]	221	-360
191	SEG[73]	255	-360
192	SEG[74]	289	-360
193	SEG[75]	323	-360
194	SEG[76]	357	-360
195	SEG[77]	391	-360
196	SEG[78]	425	-360
197	SEG[79]	459	-360
198	SEG[80]	493	-360
199	SEG[81]	527	-360
200	SEG[82]	561	-360
201	SEG[83]	595	-360
202	SEG[84]	629	-360

PAD No.	PIN Name	X	Y
203	SEG[85]	663	-360
204	SEG[86]	697	-360
205	SEG[87]	731	-360
206	SEG[88]	765	-360
207	SEG[89]	799	-360
208	SEG[90]	833	-360
209	SEG[91]	867	-360
210	SEG[92]	901	-360
211	SEG[93]	935	-360
212	SEG[94]	969	-360
213	SEG[95]	1003	-360
214	SEG[96]	1037	-360
215	SEG[97]	1071	-360
216	SEG[98]	1105	-360
217	SEG[99]	1139	-360
218	SEG[100]	1173	-360
219	SEG[101]	1207	-360
220	SEG[102]	1241	-360
221	SEG[103]	1275	-360
222	SEG[104]	1309	-360
223	SEG[105]	1343	-360
224	SEG[106]	1377	-360
225	SEG[107]	1411	-360
226	SEG[108]	1445	-360
227	SEG[109]	1479	-360
228	SEG[110]	1513	-360
229	SEG[111]	1547	-360
230	SEG[112]	1581	-360
231	SEG[113]	1615	-360
232	SEG[114]	1649	-360
233	SEG[115]	1683	-360
234	SEG[116]	1717	-360
235	SEG[117]	1751	-360
236	SEG[118]	1785	-360
237	SEG[119]	1819	-360
238	SEG[120]	1853	-360
239	SEG[121]	1887	-360
240	SEG[122]	1921	-360
241	SEG[123]	1955	-360
242	SEG[124]	1989	-360
243	SEG[125]	2023	-360
244	SEG[126]	2057	-360
245	SEG[127]	2091	-360

PAD No.	PIN Name	X	Y
246	SEG[128]	2125	-360
247	SEG[129]	2159	-360
248	SEG[130]	2193	-360
249	SEG[131]	2227	-360
250	Reserve	2267	-360
251	Reserve	2301	-360
252	Reserve	2335	-360
253	Reserve	2369	-360
254	Reserve	2403	-360
255	COM[27]	2437	-360
256	COM[28]	2471	-360
257	COM[29]	2505	-360
258	COM[30]	2539	-360
259	COM[31]	2573	-360
260	COM[32]	2810	-375
261	COM[33]	2810	-341
262	COM[34]	2810	-307
263	COM[35]	2810	-273
264	COM[36]	2810	-239
265	COM[37]	2810	-205
266	COM[38]	2810	-171
267	COM[39]	2810	-137
268	COM[40]	2810	-103
269	COM[41]	2810	-69
270	COM[42]	2810	-35
271	COM[43]	2810	-1
272	COM[44]	2810	33
273	COM[45]	2810	67
274	COM[46]	2810	101
275	COM[47]	2810	135
276	COM[48]	2810	169
277	COM[49]	2810	203
278	COM[50]	2810	237
279	COM[51]	2810	271
280	COM[52]	2810	305
281	COM[53]	2810	339
282	COMS1	2810	373

Pad Center Coordinates (1/53 Duty)

Units: µm

PAD No.	PIN Name	X	Y
1	TEST[6]	2575	392
2	FR	2515	392
3	CL	2455	392
4	DOF	2395	392
5	VSS	2335	392
6	CS1B	2275	392
7	CS2	2215	392
8	VDD	2155	392
9	RST	2095	392
10	A0	2035	392
11	VSS	1975	392
12	/WR(R/W)	1915	392
13	/RD(E)	1855	392
14	VDD	1795	392
15	D0	1735	392
16	D1	1675	392
17	D2	1615	392
18	D3	1555	392
19	D4	1495	392
20	D5	1435	392
21	D6	1375	392
22	D7	1315	392
23	VDD	1255	392
24	VDD2	1195	392
25	VDD2	1135	392
26	VSS	1075	392
27	VSS	1015	392
28	VSS	955	392
29	VSS	895	392
30	VOUT	821	392
31	VOUT	761	392
32	CAP5P	701	392
33	CAP5P	641	392
34	CAP1N	581	392
35	CAP1N	521	392
36	CAP3P	461	392
37	CAP3P	401	392
38	CAP1N	341	392
39	CAP1N	281	392
40	CAP1P	221	392
41	CAP1P	161	392
42	CAP2P	101	392
43	CAP2P	41	392
44	CAP2N	-19	392
45	CAP2N	-79	392
46	CAP4P	-139	392
47	CAP4P	-199	392
48	VSS	-273	392
49	VSS	-333	392

PAD No.	PIN Name	X	Y
50	VRS	-408	392
51	VRS	-468	392
52	VDD2	-542	392
53	VDD	-602	392
54	V4	-676	392
55	V4	-736	392
56	V3	-796	392
57	V3	-856	392
58	V2	-916	392
59	V2	-976	392
60	V1	-1036	392
61	V1	-1096	392
62	V_0	-1156	392
63	V_0	-1216	392
64	VR	-1276	392
65	VR	-1336	392
66	VDD	-1410	392
67	VDD2	-1470	392
68	TEST[0]	-1537	392
69	TEST[1]	-1611	392
70	TEST[2]	-1685	392
71	TEST[3]	-1759	392
72	TEST[4]	-1833	392
73	TEST[5]	-1907	392
74	VDD	-1974	392
75	TEST[7]	-2034	392
76	CLS	-2094	392
77	C86	-2154	392
78	PSB	-2214	392
79	HPMB	-2274	392
80	IRS	-2334	392
81	SEL1	-2394	392
82	SEL2	-2454	392
83	SEL3	-2514	392
84	VSS	-2574	392
85	Reserve	-2810	373
86	Reserve	-2810	339
87	Reserve	-2810	305
88	Reserve	-2810	271
89	Reserve	-2810	237
90	Reserve	-2810	203
91	COM[25]	-2810	169
92	COM[24]	-2810	135
93	COM[23]	-2810	101
94	COM[22]	-2810	67
95	COM[21]	-2810	33
96	COM[20]	-2810	-1
97	COM[19]	-2810	-35
98	COM[18]	-2810	-69

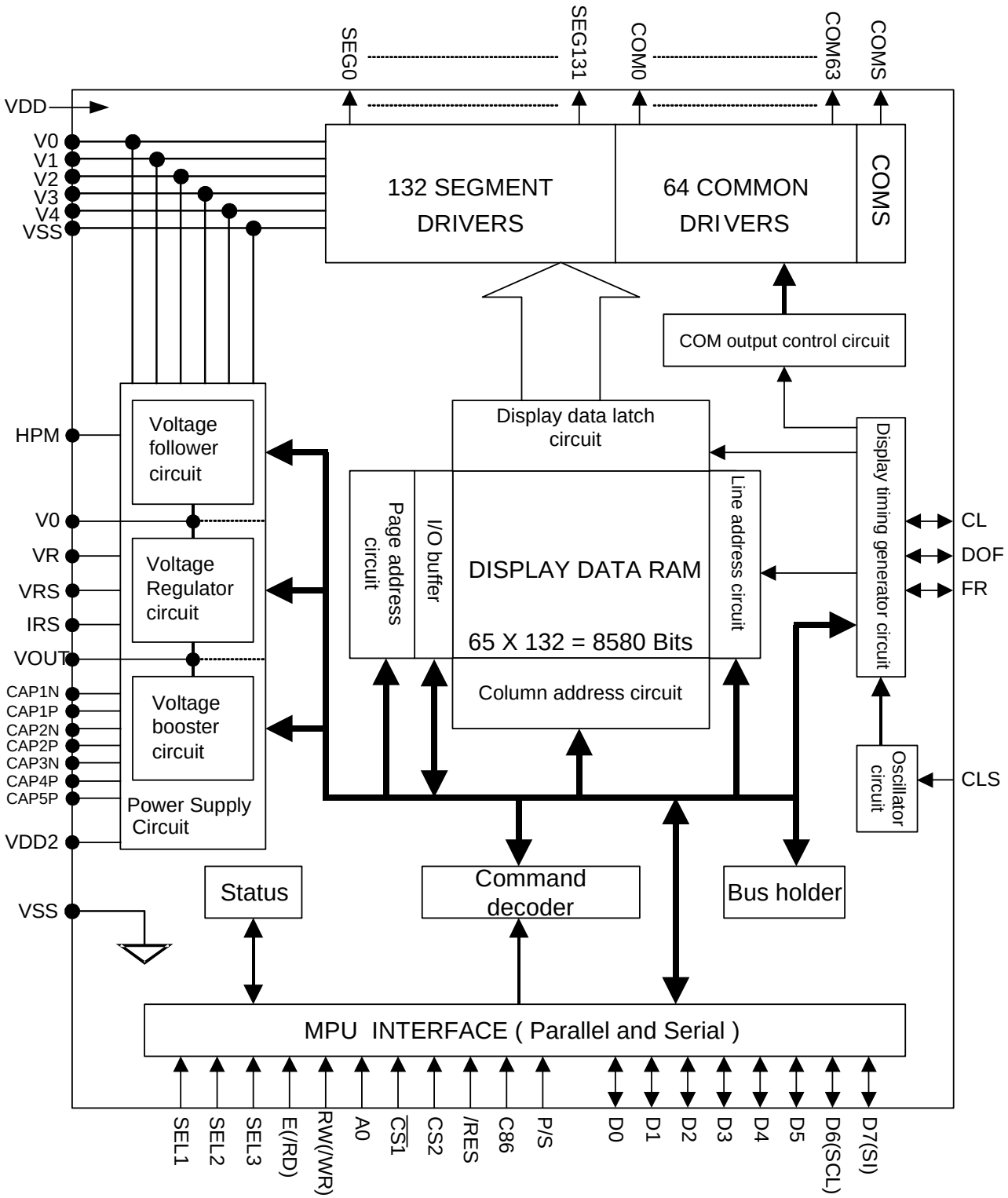
PAD No.	PIN Name	X	Y
99	COM[17]	-2810	-103
100	COM[16]	-2810	-137
101	COM[15]	-2810	-171
102	COM[14]	-2810	-205
103	COM[13]	-2810	-239
104	COM[12]	-2810	-273
105	COM[11]	-2810	-307
106	COM[10]	-2810	-341
107	COM[9]	-2810	-375
108	COM[8]	-2573	-360
109	COM[7]	-2539	-360
110	COM[6]	-2505	-360
111	COM[5]	-2471	-360
112	COM[4]	-2437	-360
113	COM[3]	-2403	-360
114	COM[2]	-2369	-360
115	COM[1]	-2335	-360
116	COM[0]	-2301	-360
117	COMS2	-2267	-360
118	SEG[0]	-2227	-360
119	SEG[1]	-2193	-360
120	SEG[2]	-2159	-360
121	SEG[3]	-2125	-360
122	SEG[4]	-2091	-360
123	SEG[5]	-2057	-360
124	SEG[6]	-2023	-360
125	SEG[7]	-1989	-360
126	SEG[8]	-1955	-360
127	SEG[9]	-1921	-360
128	SEG[10]	-1887	-360
129	SEG[11]	-1853	-360
130	SEG[12]	-1819	-360
131	SEG[13]	-1785	-360
132	SEG[14]	-1751	-360
133	SEG[15]	-1717	-360
134	SEG[16]	-1683	-360
135	SEG[17]	-1649	-360
136	SEG[18]	-1615	-360
137	SEG[19]	-1581	-360
138	SEG[20]	-1547	-360
139	SEG[21]	-1513	-360
140	SEG[22]	-1479	-360
141	SEG[23]	-1445	-360
142	SEG[24]	-1411	-360
143	SEG[25]	-1377	-360
144	SEG[26]	-1343	-360
145	SEG[27]	-1309	-360
146	SEG[28]	-1275	-360
147	SEG[29]	-1241	-360
148	SEG[30]	-1207	-360
149	SEG[31]	-1173	-360
150	SEG[32]	-1139	-360

PAD No.	PIN Name	X	Y
151	SEG[33]	-1105	-360
152	SEG[34]	-1071	-360
153	SEG[35]	-1037	-360
154	SEG[36]	-1003	-360
155	SEG[37]	-969	-360
156	SEG[38]	-935	-360
157	SEG[39]	-901	-360
158	SEG[40]	-867	-360
159	SEG[41]	-833	-360
160	SEG[42]	-799	-360
161	SEG[43]	-765	-360
162	SEG[44]	-731	-360
163	SEG[45]	-697	-360
164	SEG[46]	-663	-360
165	SEG[47]	-629	-360
166	SEG[48]	-595	-360
167	SEG[49]	-561	-360
168	SEG[50]	-527	-360
169	SEG[51]	-493	-360
170	SEG[52]	-459	-360
171	SEG[53]	-425	-360
172	SEG[54]	-391	-360
173	SEG[55]	-357	-360
174	SEG[56]	-323	-360
175	SEG[57]	-289	-360
176	SEG[58]	-255	-360
177	SEG[59]	-221	-360
178	SEG[60]	-187	-360
179	SEG[61]	-153	-360
180	SEG[62]	-119	-360
181	SEG[63]	-85	-360
182	SEG[64]	-51	-360
183	SEG[65]	-17	-360
184	SEG[66]	17	-360
185	SEG[67]	51	-360
186	SEG[68]	85	-360
187	SEG[69]	119	-360
188	SEG[70]	153	-360
189	SEG[71]	187	-360
190	SEG[72]	221	-360
191	SEG[73]	255	-360
192	SEG[74]	289	-360
193	SEG[75]	323	-360
194	SEG[76]	357	-360
195	SEG[77]	391	-360
196	SEG[78]	425	-360
197	SEG[79]	459	-360
198	SEG[80]	493	-360
199	SEG[81]	-207	-374
200	SEG[82]	-149	-374
201	SEG[83]	-91	-374
202	SEG[84]	-33	-374

PAD No.	PIN Name	X	Y
203	SEG[85]	25	-374
204	SEG[86]	83	-374
205	SEG[87]	141	-374
206	SEG[88]	199	-374
207	SEG[89]	257	-374
208	SEG[90]	315	-374
209	SEG[91]	373	-374
210	SEG[92]	431	-374
211	SEG[93]	489	-374
212	SEG[94]	547	-374
213	SEG[95]	605	-374
214	SEG[96]	663	-374
215	SEG[97]	721	-374
216	SEG[98]	779	-374
217	SEG[99]	837	-374
218	SEG[100]	895	-374
219	SEG[101]	953	-374
220	SEG[102]	1011	-374
221	SEG[103]	1069	-374
222	SEG[104]	1127	-374
223	SEG[105]	1185	-374
224	SEG[106]	1243	-374
225	SEG[107]	1301	-374
226	SEG[108]	1359	-374
227	SEG[109]	1417	-374
228	SEG[110]	1475	-374
229	SEG[111]	1533	-374
230	SEG[112]	1591	-374
231	SEG[113]	1649	-374
232	SEG[114]	1707	-374
233	SEG[115]	1765	-374
234	SEG[116]	1823	-374
235	SEG[117]	1881	-374
236	SEG[118]	1939	-374
237	SEG[119]	1997	-374
238	SEG[120]	2055	-374
239	SEG[121]	2113	-374
240	SEG[122]	2171	-374
241	SEG[123]	2229	-374
242	SEG[124]	2287	-374
243	SEG[125]	2345	-374
244	SEG[126]	2403	-374
245	SEG[127]	2461	-374

PAD No.	PIN Name	X	Y
246	SEG[128]	2519	-374
247	SEG[129]	2577	-374
248	SEG[130]	2635	-374
249	SEG[131]	2693	-374
250	Reserve	2751	-374
251	Reserve	2809	-374
252	Reserve	2867	-374
253	Reserve	2925	-374
254	Reserve	2983	-374
255	Reserve	3041	-374
256	COM[26]	3099	-374
257	COM[27]	3157	-374
258	COM[28]	3215	-374
259	COM[29]	3273	-374
260	COM[30]	3331	-374
261	COM[31]	3389	-374
262	COM[32]	3447	-374
263	COM[33]	3505	-374
264	COM[34]	3563	-374
265	COM[35]	3621	-374
266	COM[36]	3679	-374
267	COM[37]	3737	-374
268	COM[38]	3795	-374
269	COM[39]	3853	-374
270	COM[40]	3911	-374
271	COM[41]	3969	-374
272	COM[42]	4027	-374
273	COM[43]	4085	-374
274	COM[44]	4143	-374
275	COM[45]	4201	-374
276	COM[46]	4259	-374
277	COM[47]	4542	-345
278	COM[48]	4542	-287
279	COM[49]	4542	-229
280	COM[50]	4542	-171
281	COM[51]	4542	-113
282	COMS1	4542	-55

Block Diagram



Pin Descriptions

Power Supply Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>VDD</td><td>Power Supply</td><td>Power supply</td><td>13</td></tr>
<tr><td>VDD2</td><td>Power Supply</td><td>Power supply</td><td>10</td></tr>
<tr><td>VSS</td><td>Power Supply</td><td>Ground</td><td>2</td></tr>
<tr><td>VRS</td><td>Power Supply</td><td>This is the internal-output VREG power supply for the LCD power supply voltage regulator.</td><td>2</td></tr>
<tr><td>V_0, V1, V2, V3, V4,Vss</td><td>Power Supply</td><td>This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on Vss, and must maintain the relative magnitudes shown below.

$V_0 \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq Vss$

When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.
<table>
<tr><th></th><th>1/65 DUTY</th><th>1/49 DUTY</th><th>1/33 DUTY</th><th>1/55 DUTY</th><th>1/53 DUTY</th></tr>
<tr><td>V1</td><td>$8/9*V_0,6/7*V_0$</td><td>$7/8*V_0,5/6*V_0$</td><td>$5/6*V_0,4/5*V_0$</td><td>$7/8*V_0,5/6*V_0$</td><td>$7/8*V_0,5/6*V_0$</td></tr>
<tr><td>V2</td><td>$7/9*V_0,5/7*V_0$</td><td>$6/8*V_0,4/6*V_0$</td><td>$4/6*V_0,3/5*V_0$</td><td>$6/8*V_0,4/6*V_0$</td><td>$6/8*V_0,4/6*V_0$</td></tr>
<tr><td>V3</td><td>$2/9*V_0,2/7*V_0$</td><td>$2/8*V_0,2/6*V_0$</td><td>$2/6*V_0,2/5*V_0$</td><td>$2/8*V_0,2/6*V_0$</td><td>$2/8*V_0,2/6*V_0$</td></tr>
<tr><td>V4</td><td>$1/9*V_0,1/7*V_0$</td><td>$1/8*V_0,1/6*V_0$</td><td>$1/6*V_0,1/5*V_0$</td><td>$1/8*V_0,1/6*V_0$</td><td>$1/8*V_0,1/6*V_0$</td></tr>
</table></td><td>10</td></tr>
</table>

LCD Power Supply Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>CAP1P</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.</td><td>4</td></tr>
<tr><td>CAP1N</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.</td><td>2</td></tr>
<tr><td>CAP2P</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.</td><td>2</td></tr>
<tr><td>CAP2N</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.</td><td>2</td></tr>
<tr><td>CAP3P</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.</td><td>2</td></tr>
<tr><td>CAP4P</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.</td><td>2</td></tr>
<tr><td>CAP5P</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.</td><td>2</td></tr>
<tr><td>VOUT</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and VSS or VDD terminal.</td><td>2</td></tr>
<tr><td>VR</td><td>I</td><td>Output voltage regulator terminal. Provides the voltage between VSS and V_0 through a resistive voltage divider.
IRS = “L” : the V_0 voltage regulator internal resistors are not used.
IRS = “H” : the V_0 voltage regulator internal resistors are used.</td><td>2</td></tr>
</table>

System Bus Connection Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>D5 to D0
D6 (SCL)
D7 (SI)</td><td>I/O</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.
When the serial interface (SPI-4) is selected (P/S = “L”) :
D7 : serial data input (SI) ; D6 : the serial clock input (SCL).
D0 to D5 should be connected to VDD or floating.
When the chip select is not active, D0 to D7 are set to high impedance.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or command.
A0 = “H”: Indicates that D0 to D7 are display data.
A0 = “L”: Indicates that D0 to D7 are control data.</td><td>1</td></tr>
<tr><td>/RES</td><td>I</td><td>When /RES is set to “L”, the register settings are initialized (cleared).
The reset operation is performed by the /RES signal level.</td><td>1</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>This is the chip select signal. When CS1B = “L” and CS2 = “H”, then the chip select becomes active, and data/command I/O is enabled.</td><td>2</td></tr>
<tr><td>/RD
(E)</td><td>I</td><td>• When connected to 8080 series MPU, this pin is treated as the “/RD” signal of the 8080 MPU and is LOW-active.
The data bus is in an output status when this signal is “L”.
• When connected to 6800 series MPU, this pin is treated as the “E” signal of the 6800 MPU and is HIGH-active.
This is the enable clock input terminal of the 6800 Series MPU.</td><td>1</td></tr>
<tr><td>/WR
(R/W)</td><td>I</td><td>• When connected to 8080 series MPU, this pin is treated as the “/WR” signal of the 8080 MPU and is LOW-active.
The signals on the data bus are latched at the rising edge of the /WR signal.
• When connected to 6800 series MPU, this pin is treated as the “R/W” signal of the 6800 MPU and decides the access type :
When R/W = “H”: Read.
When R/W = “L”: Write.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>This is the MPU interface selection pin.
C86 = “H”: 6800 Series MPU interface.
C86 = “L”: 8080 Series MPU interface.</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>This pin configures the interface to be parallel mode or serial mode.
P/S = “H”: Parallel data input/output.
P/S = “L”: Serial data input.
The following applies depending on the P/S status:
<table><tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>4-line SPI Clock</th></tr><tr><td>“H”</td><td>A0</td><td>D0 to D7</td><td>/RD, /WR</td><td>X</td></tr><tr><td>“L”</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr></table>When P/S = “L”, D0 to D5 must be fixed to “H”.
/RD (E) and /WR (R/W) are fixed to either “H” or “L”.
The serial access mode does NOT support read operation.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>CLS</td><td>I</td><td>Selection pin to enable or disable the internal display clock oscillator circuit.
CLS = “H” : use internal oscillator circuit .
CLS = “L” : use external clock input (internal oscillator is disabled).
When CLS = “L”, input the external display clock through the CL terminal.</td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>This is the display clock input terminal
The following is true depending on the CLS status.
<table>
<tr><th>CLS</th><th>CL</th></tr>
<tr><td>“H”
“L”</td><td>Output
Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>FR</td><td>O</td><td>This is the liquid crystal alternating current signal terminal.</td><td>1</td></tr>
<tr><td>/DOF</td><td>O</td><td>This is the LCD blanking control terminal.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V_0 voltage level adjustment.
IRS = “H”: Use the internal resistors
IRS = “L”: Do not use the internal resistors. The V_0 voltage level is
regulated by an external resistive voltage divider attached to the VR terminal</td><td>1</td></tr>
<tr><td>/HPM</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
/HPM = “H”: Normal mode
/HPM = “L”: High power mode (suggested)</td><td>1</td></tr>
<tr><td>SEL3
SEL2
SEL1</td><td>I</td><td>These pins are DUTY selection.
<table>
<tr><th>SEL 3, 2, 1</th><th>DUTY</th><th>BIAS</th></tr>
<tr><td>0, 0, 0</td><td>1/65</td><td>1/9 or 1/7</td></tr>
<tr><td>0, 0, 1</td><td>1/49</td><td>1/8 or 1/6</td></tr>
<tr><td>0, 1, 0</td><td>1/33</td><td>1/6 or 1/5</td></tr>
<tr><td>0, 1, 1</td><td>1/55</td><td>1/8 or 1/6</td></tr>
<tr><td>1, 0, 0</td><td>1/53</td><td>1/8 or 1/6</td></tr>
<tr><td>1, X, X</td><td>-----</td><td>-----</td></tr>
</table></td><td>3</td></tr>
<tr><td>TEST0 ~ 7</td><td>I</td><td>These are terminals for IC testing.
TEST0 ~ 6: left them open.
TEST7 must connected to VDD.</td><td>6</td></tr>
</table>

LCD Driver Pins

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>SEG0
to
SEG131</td><td>O</td><td>These are the LCD segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from Vss, V3, V2, and V_0.
<table>
<tr><th rowspan="2">RAM DATA</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr>
<tr><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td>H</td><td>H</td><td>V_0</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>Vss</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>V_0</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>Vss</td></tr>
<tr><td>Power save</td><td></td><td colspan="2">Vss</td></tr>
</table></td><td>132</td></tr>
<tr><td>COM0
to
COMn</td><td>O</td><td>Through a combination of the contents of the scan data and with the FR signal, a single level is selected from Vss, V_4, V_1, and V_0.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>Vss</td></tr>
<tr><td>H</td><td>L</td><td>V_0</td></tr>
<tr><td>L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td></tr>
<tr><td>Power save</td><td></td><td>Vss</td></tr>
</table></td><td>67</td></tr>
<tr><td>COMS</td><td>O</td><td>These are the COM output terminals for the indicator. Both terminals output the same signal.
Leave these open if they are not used.</td><td>2</td></tr>
</table>

ST7565R I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
CL, FR, /DOF, C86, PSB, HPMB, SEL1…SEL3, CLS, IRS, TEST7	**No Limitation**
TEST0 ~6, VRS	**Floating**
VDD, VDD2, VSS, VOUT, VR	**<100Ω**
V_0, V1, V2, V3, V4, CAP1P, CAP1N, CAP2P, CAP2N, CAP3P, CAP4P, CAP5P	**<300Ω**
CS1B, CS2, /RD, /WR, A0, D0 …D7	**<1KΩ**
RST	**<10KΩ**

Description Of Functions

The MPU Interface

Selecting the Interface Type

With the ST7565R chips, data transfers are done through an 8-bit parallel data bus (D7 to D0) or through a 4-line SPI data input (SI). Through selecting the P/ S terminal polarity to the “H” or “L” it is possible to select either parallel data input or 4-line SPI data input as shown in Table 1.

Table 1

P/S	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
H: Parallel Input	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D5~D0
L: 4-line SPI Input	/CS1	CS2	A0	—	—	—	SI	SCL	(HZ)

“—” indicates fixed to “H”

The Parallel Interface

When the parallel interface has been selected (P/S =“H”), then it is possible to connect directly to either an 8080-system MPU or a 6800 Series MPU (shown in Table 2) by selecting the C86 terminal to either “H” or to “L”.

Table 2

C86 (P/S=H)	/CS1	CS2	A0	E(/RD)	R/W(/WR)	D7~D0
H: 6800 Series	/CS1	CS2	A0	E	R/W	D7~D0
L: 8080 Series	/CS1	CS2	A0	/RD	/WR	D7~D0

Moreover, data bus signals are recognized by a combination of A0, /RD (E), /WR (R/W) signals, as shown in Table 3.

Table 3

Shared	6800 Series	8080 Series		Function
A0	R/W	/RD	/WR	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

The 4-line SPI Interface

When the 4-line SPI interface has been selected (P/S = “L”) then when the chip is in active state (/CS1 = “L” and CS2 = “H”) the 4-line SPI data input (SI) and the 4-line SPI clock input (SCL) can be received. The 4-line SPI data is read from the 4-line SPI data input pin in the rising edge of the 4-line SPI clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth 4-line SPI clock for the processing. The A0 input is used to determine whether or the 4-line SPI data input is display data or command data; when A0 = “H”, the data is display data, and when A0 = “L” then the data is command data. The A0 input is read and used for detection every 8th rising edge of the 4-line SPI clock after the chip becomes active. Figure 1 is a 4-line SPI interface signal chart.

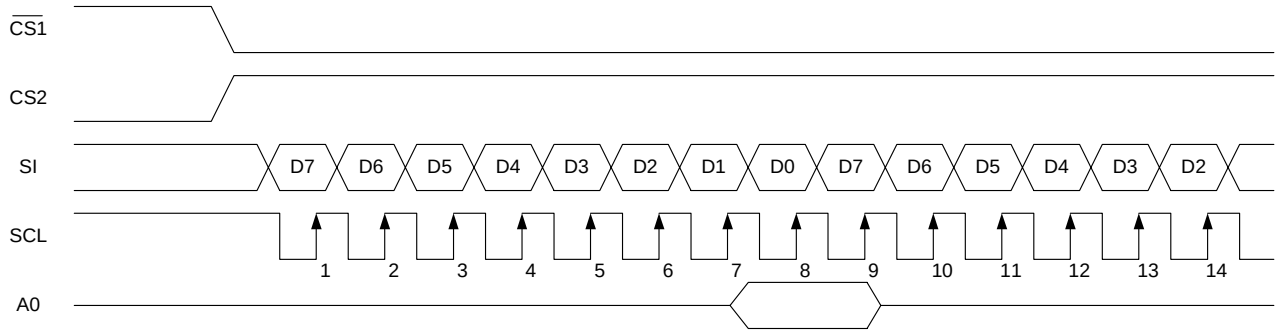


Figure 1

* When the chip is not active, the shift registers and the counter are reset to their initial states.
* Reading is not possible while in 4-line SPI interface mode.
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

The Chip Select

The ST7565R have two chip select terminals: /CS1 and CS2. The MPU interface or the 4-line SPI interface is enabled only when /CS1 = “L” and CS2 = “H”.

When the chip select is inactive, D0 to D7 enter a high impedance state, and the A0, /RD, and /WR inputs are inactive. When the 4-line SPI interface is selected, the shift register and the counter are reset.

The Accessing the Display Data RAM and the Internal Registers

Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (t_{CYC}) requirement alone in accessing the ST7565R. Wait time may not be considered.
And, in the ST7565R, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus. Internal data bus.
For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.
There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted.
This relationship is shown in Figure 2.

The Busy Flag

When the busy flag is “1” it indicates that the ST7565R is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pin with the read instruction. If the cycle time (t_{CYC}) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

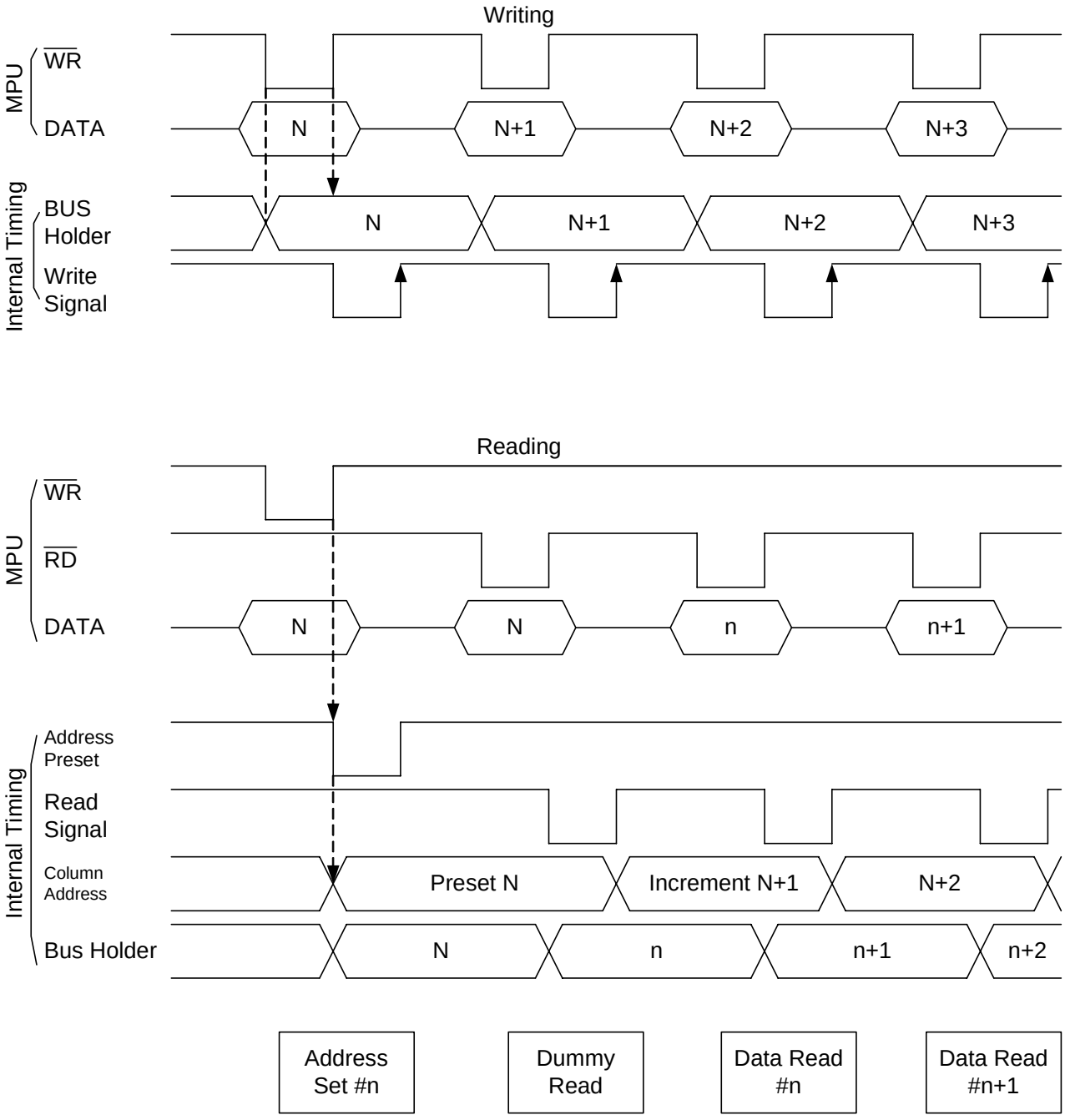

Writing
MPU
WR
DATA
N
N+1
N+2
N+3
Internal Timing
BUS Holder
Write Signal
N
N+1
N+2
N+3
Reading
MPU
WR
RD
DATA
N
N
n
n+1
Internal Timing
Address Preset
Read Signal
Column Address
Bus Holder
Preset N
Increment N+1
N+2
N
n
n+1
n+2
Address Set #n
Dummy Read
Data Read #n
Data Read #n+1

Figure 2

Display Data RAM

The display data RAM stores the dot data for the LCD. It has a 65 (8 page x 8 bit +1) x 132 bit structure.
As is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the LCD display common direction; there are few constraints at the time of display data transfer when multiple ST7565R are used, thus and display structures can be created easily and with a high degree of freedom.
Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

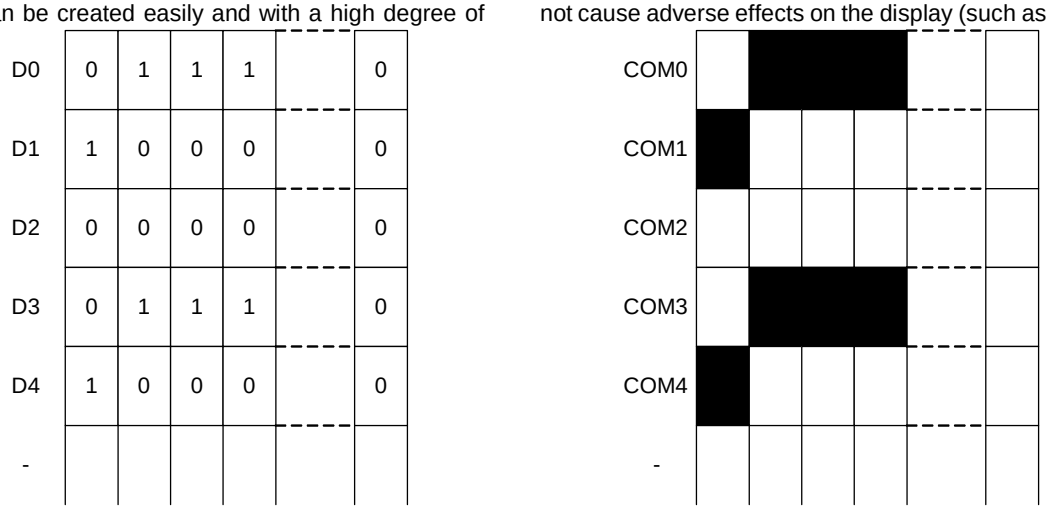


Figure 3

The Page Address Circuit

Page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

Page address 8 (D3, D2, D1, D0 = 1, 0, 0, 0) is a special RAM for icons, and only display data D0 is used.
(see Figure 4)

The Column Addresses

The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the incrementing of column addresses stops with 83H. Because the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to respective both the page address and the column address.
Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized. As is shown in Figure 4,

Table 4

SEG Output ADC	SEG0		SEG 131
(D0) "0"	0 (H)	→ Column Address →	83 (H)
(D0) "1"	83 (H)	← Column Address ←	0 (H)

The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for ST7565R, the detail is shown page.11 The display area is a 65 line area for the ST7565R.
If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

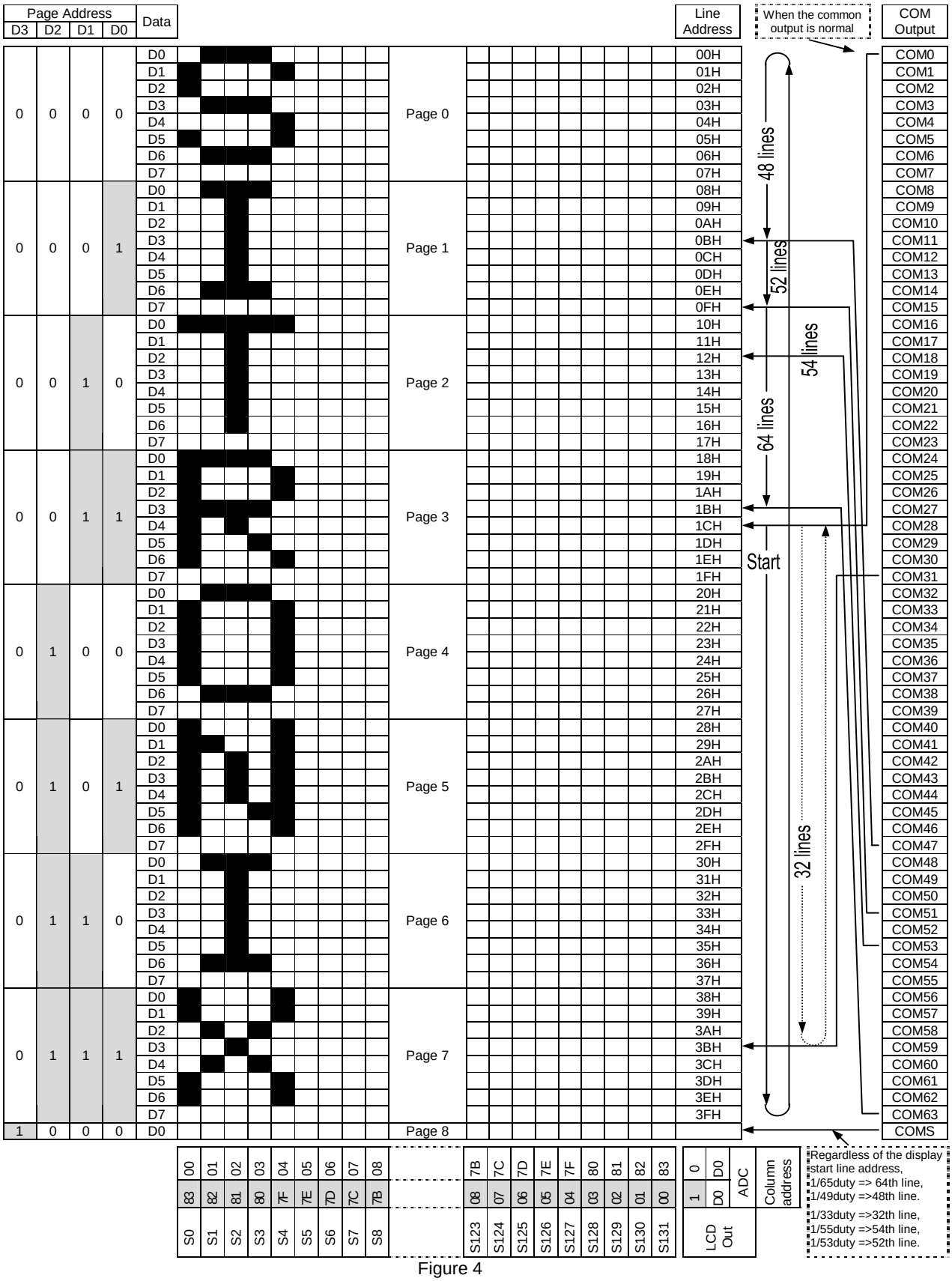

Page Address
D3 D2 D1 D0
Data
Line Address
When the common output is normal
COM Output
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Page 6
Page 7
Page 8
48 lines
52 lines
54 lines
64 lines
32 lines
Start
COM0 COM1 COM2 COM3 COM4 COM5 COM6 COM7 COM8 COM9 COM10 COM11 COM12 COM13 COM14 COM15 COM16 COM17 COM18 COM19 COM20 COM21 COM22 COM23 COM24 COM25 COM26 COM27 COM28 COM29 COM30 COM31 COM32 COM33 COM34 COM35 COM36 COM37 COM38 COM39 COM40 COM41 COM42 COM43 COM44 COM45 COM46 COM47 COM48 COM49 COM50 COM51 COM52 COM53 COM54 COM55 COM56 COM57 COM58 COM59 COM60 COM61 COM62 COM63 COMS
00 01 02 03 04 05 06 07 08
83 82 81 80 7F 7E 7D 7C 7B
S0 S1 S2 S3 S4 S5 S6 S7 S8
7B 7C 7D 7E 7F 80 81 82 83
08 07 06 05 04 03 02 01 00
S123 S124 S125 S126 S127 S128 S129 S130 S131
0 D0 ADC
1 D0
LCD Out
Column address
Regardless of the display start line address,
1/65duty => 64th line,
1/49duty =>48th line.
1/33duty =>32th line,
1/55duty =>54th line,
1/53duty =>52th line.

Figure 4

The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.
Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when CLS = “H”.

When CLS = “L” the oscillation stops, and the external clock is input through the CL terminal.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.
Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave form using a 2 frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

Two-frame alternating current drive waveform

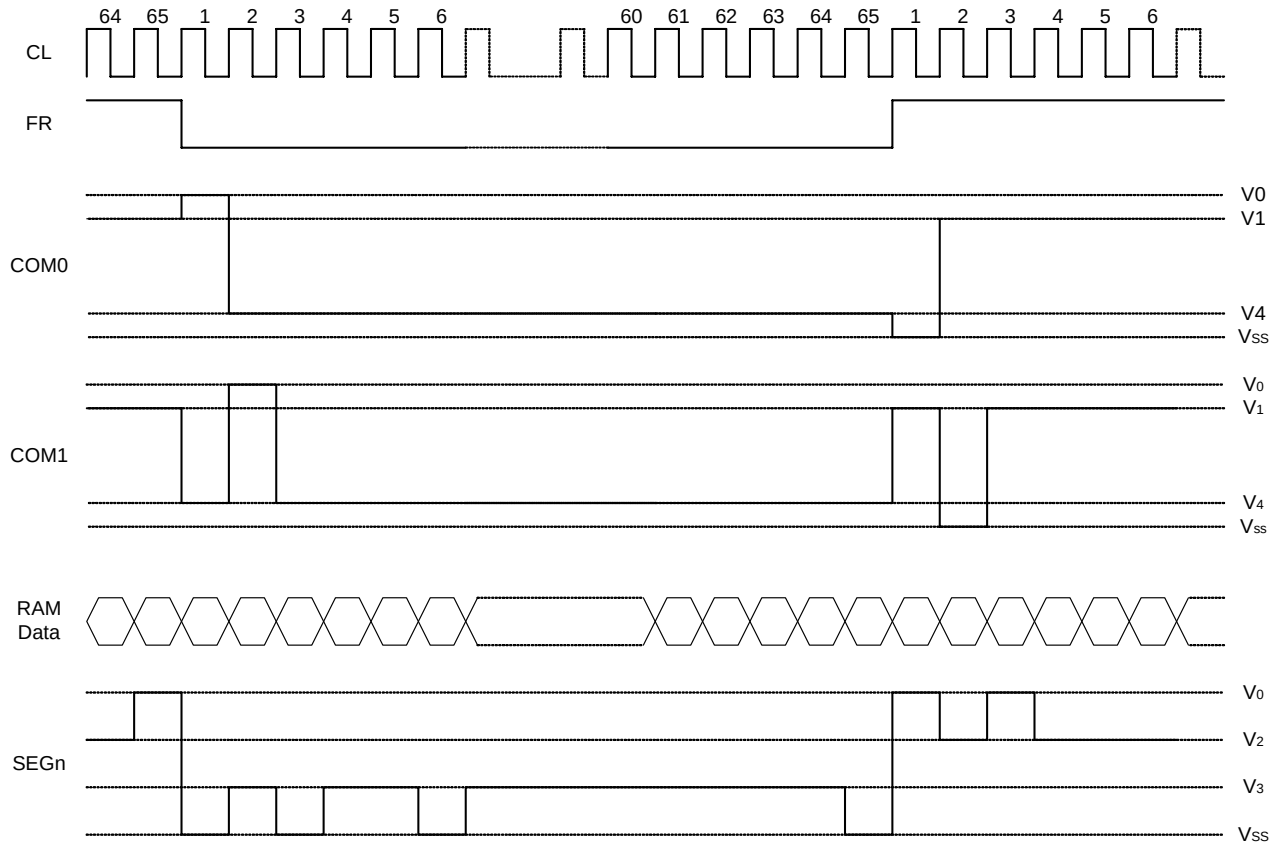


Figure 5

The Common Output Status Select Circuit

In the ST7565R chips, the COM output scan direction can be selected by the common output status select command. (See Table 6.) Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Table 6

Status	COM Scan Direction				
	1/65 DUTY	**1/49 DUTY**	**1/33 DUTY**	**1/55 DUTY**	**1/53 DUTY**
Normal	COM0 → COM63	COM0 → COM47	COM0 → COM31	COM0 → COM53	COM0 → COM51
Reverse	COM63 → COM0	COM47 → COM0	COM31 → COM0	COM53 → COM0	COM51 → COM0

Duty	COM dir	Common output pins						
		COM[0:15]	**COM[16:23]**	**COM[24:26]**	**COM[27:36]**	**COM[37:39]**	**COM[40:47]**	**COM[48:63]**
1/65	0	COM[0:63]						
	1	COM[63:0]						
1/49	0	COM[0:23]		Reserved			COM[24:47]	
	1	COM[47:24]		Reserved			COM[23:0]	
1/33	0	COM[0:15]	Reserved					COM[16:31]
	1	COM[31:16]	Reserved					COM[15:0]
1/55	0	COM[0:26]			Reserved	COM[27:53]		
	1	COM[53:27]			Reserved	COM[26:0]		
1/53	0	COM[0:25]			Reserved	COM[26:51]		
	1	COM[51:26]			Reserved	COM[25:0]		

The LCD Driver Circuits

These are a 187-channel that generates four voltage levels for driving the LCD . The combination of the display data, the COM scan signal, and the FR signal produces the liquid crystal drive voltage output.

Figure 6 shows examples of the SEG and COM output wave form.

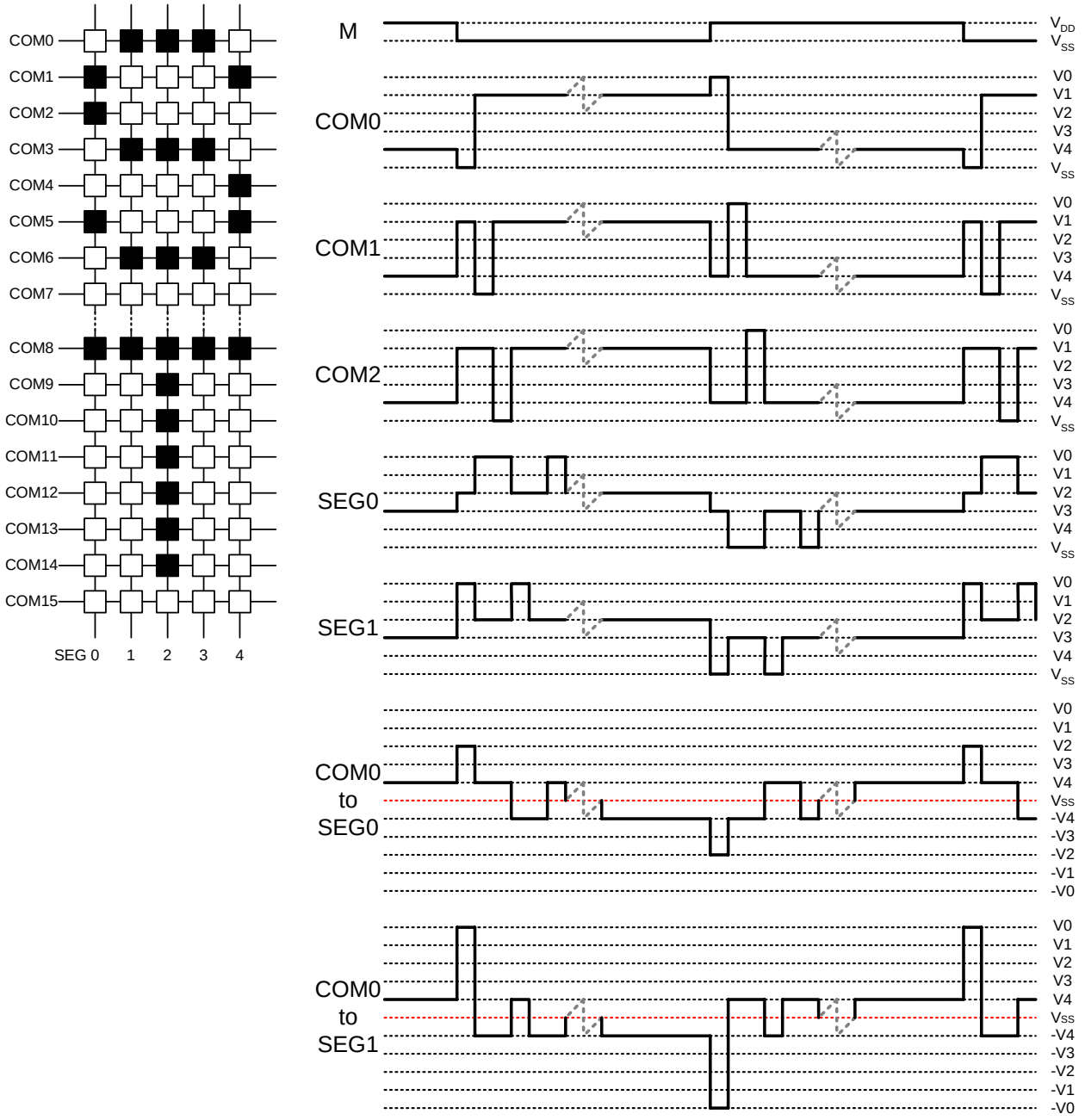


Figure 6

The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the LCD drivers. They are Booster circuits, voltage regulator circuits, and voltage follower circuits. The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 7 shows the Power Control Set Command 3-bit data control function, and Table 8 shows reference combinations.

Table 7

bit	function	Status "1" "0"
D2	Booster circuit control bit	ON OFF
D1	Voltage regulator circuit control bit (V/R circuit)	ON OFF
D0	Voltage follower circuit control bit (V/F circuit)	ON OFF

The Control Details of Each Bit of the Power Control Set Command

Table 8

Use Settings	D2	D1	D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Step-up voltage
Only the internal power supply is used	1	1	1	ON	ON	ON	V_{DD2}	Used
Only the voltage regulator circuit and the voltage follower circuit are used	0	1	1	OFF	ON	ON	V_{OUT}, V_{DD2}	Open
Only the V/F circuit is used	0	0	1	OFF	OFF	ON	V_0, V_{DD2}	Open
Only the external power supply is used	0	0	0	OFF	OFF	OFF	V_0 to V_4	Open

Reference Combinations

* The "step-up system terminals" refer CAP1N, CAP1P, CAP2N, CAP2P, and CAP3N.
* While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

The Step-up Voltage Circuits

Using the step-up voltage circuits equipped within the ST7565R chips it is possible to product a 2X,3X,4X,5X or 6X step-up of the V_{SS} – V_{DD2} voltage levels.

6X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, between CAP2N and CAP4P,between CAP1N and CAP5P, and between V_{DD2} and V_{OUT}, to produce a voltage level in the positive direction at the V_{OUT} terminal that is 6 times the voltage level between V_{SS} and $V_{DD}2$.

5X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, between CAP2N and CAP4P,and between V_{DD2} and V_{OUT}, to produce a voltage level in the positive direction at the V_{OUT} terminal that is 5 times the voltage level between V_{SS} and $V_{DD}2$.

4X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, and between V_{DD2} and V_{OUT}, to produce a voltage level in the positive direction at the V_{OUT} terminal that is 4 times the voltage level between V_{SS} and $V_{DD}2$.

3X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P and between V_{DD2} and V_{OUT}, and short between CAP3P and V_{OUT} to produce voltages level in the positive direction at the V_{OUT} terminal that is 3 times the voltage difference between V_{SS} and $V_{DD}2$.

2X step-up: Connect capacitor C1 between CAP1N and CAP1P, and between V_{DD2} and V_{OUT}, leave CAP2N open, and short between CAP2P, CAP3P and V_{OUT} to produce a voltage in the positive direction at the V_{OUT} terminal that Is twice the voltage between V_{SS} and $V_{DD}2$.

The step-up voltage relationships are shown in Figure 7.

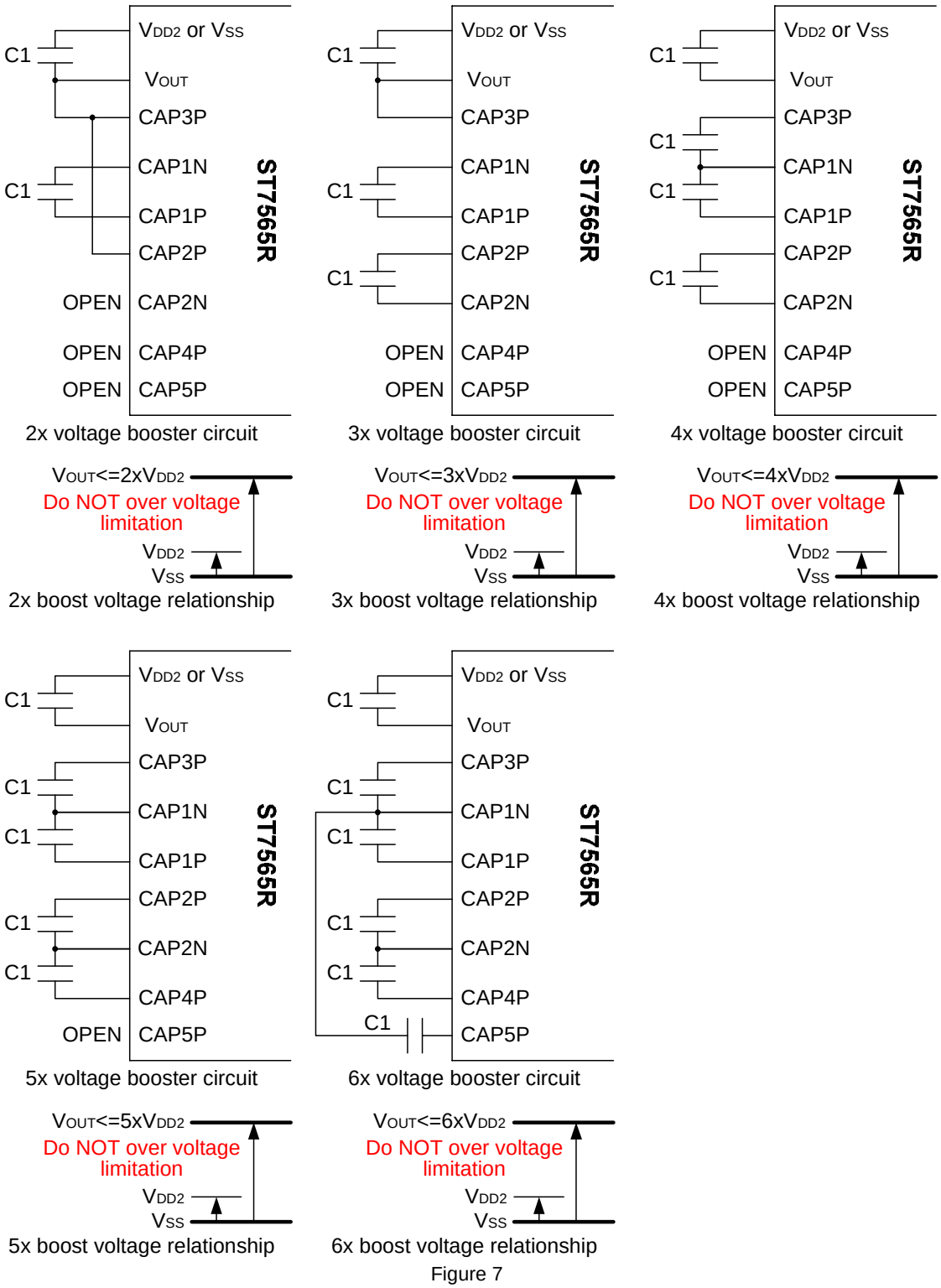


Figure 7

* The V_{DD2} voltage range must be set so that the V_{OUT} terminal voltage does not exceed the absolute maximum rated value.
* The maximum voltage of the booster capacitor terminals are :
  V_{MAX}: CAP5P > CAP4P > CAP3P > CAP2P > CAP1P > CAP2N = CAP1N.

The Voltage Regulator Circuit

The step-up voltage generated at VOUT outputs the LCD driver voltage V_0 through the voltage regulator circuit. Because the ST7565R chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V_0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components. (VREG thermal gradients approximate -0.05%/°C)

(A) When the V_0 Voltage Regulator Internal Resistors Are Used

Through the use of the V_0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V_0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V_0 voltage can be calculated using equation A-1 over the range where $|V_0| < |V_{OUT}|$.

$$V_0 = \left(1 + \frac{Rb}{Ra}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{Rb}{Ra}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$

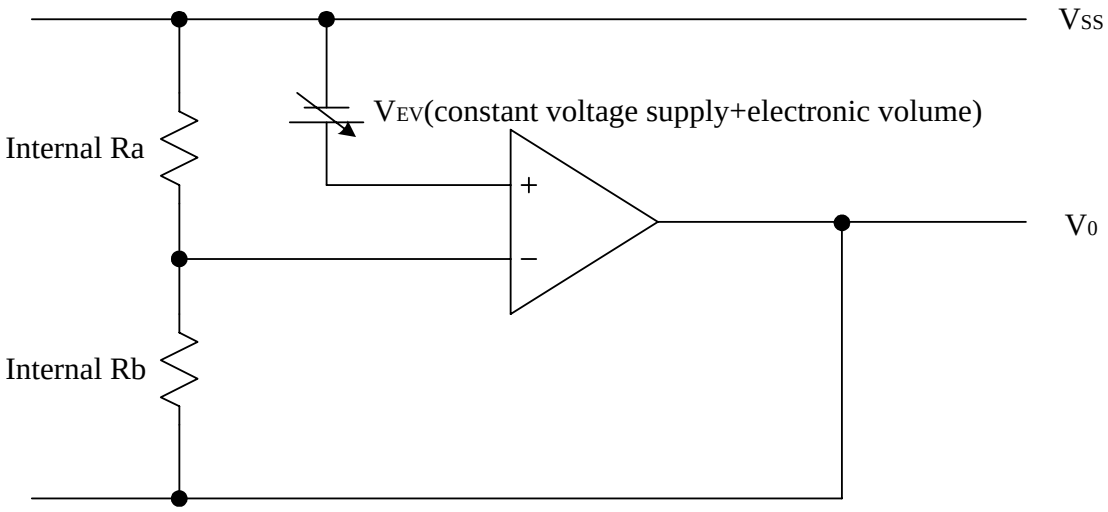


Figure 8

VREG is the IC-internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 9.

Table 9

Part no.	Equipment Type	Thermal Gradient	VREG
ST7565R	Internal Power Supply	–0.05 %/°C	2.1V

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume registers. Table 10 shows the value for α depending on the electronic volume register settings.
Rb/Ra is the V_0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V_0 voltage regulator internal resistor ratio set command. The (1 + Rb/Ra) ratio assumes the values shown in Table 11 depending on the 3-bit data settings in the V_0 voltage regulator internal resistor ratio register.

Table 10

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			:			:
			:			:
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

V_0 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table 11

Register			ST7565R
D2	D1	D0	(1) –0.05 %/°C
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

Figures 9, 10 show V_0 voltage measured by values of the internal resistance ratio resistor for V_0 voltage adjustment and electric volume resister for each temperature grade model.

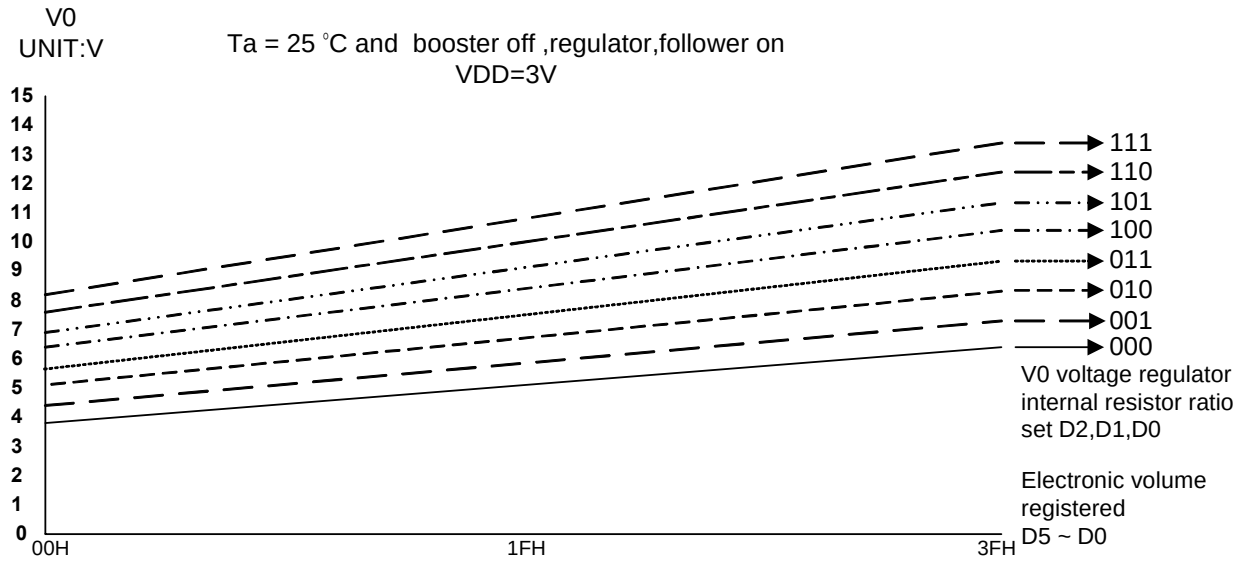


Figure 9 : (1) For ST7565R the Thermal Gradient = -0.05%/°C

The V_0 voltage as a function of the V_0 voltage regulator internal resistor ratio register and the electronic volume register.

Setup example: When selecting Ta = 25°C and V_0 = 7V for an ST7565R on which Temperature gradient = –0.05%/°C.
Using Figure 9 and the equation A-1, the following setup is enabled.
At this time, the variable range and the notch width of the V_0 voltage is, as shown Table 13, as dependent on the electronic volume.

Table 12

Contents	Register					
	D5	D4	D3	D2	D1	D0
For V_0 voltage regulator	—	—	—	0	1	0
Electronic Volume	1	0	0	1	0	1

Table 13

V_0	Min	Typ	Max	Units
Variable Range	5.1 (63 levels)	7.0 (central value)	8.4 (0 level)	[V]
Notch width		51		[mV]

(B) When an External Resistance is Used (The V_0 Voltage Regulator Internal Resistors Are Not Used) (1)

The liquid crystal power supply voltage V_0 can also be set without using the V_0 voltage regulator internal resistors (IRS terminal = "L") by adding resistors Ra' and Rb' between V_{DD} and V_R, and between V_R and V_0, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal power supply voltage V_0 through commands.

In the range where $|V_0| < |V_{OUT}|$, the V_0 voltage can be calculated using equation B-1 based on the external resistances Ra' and Rb'.

$$V_0 = \left(1 + \frac{Rb'}{Ra'}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$

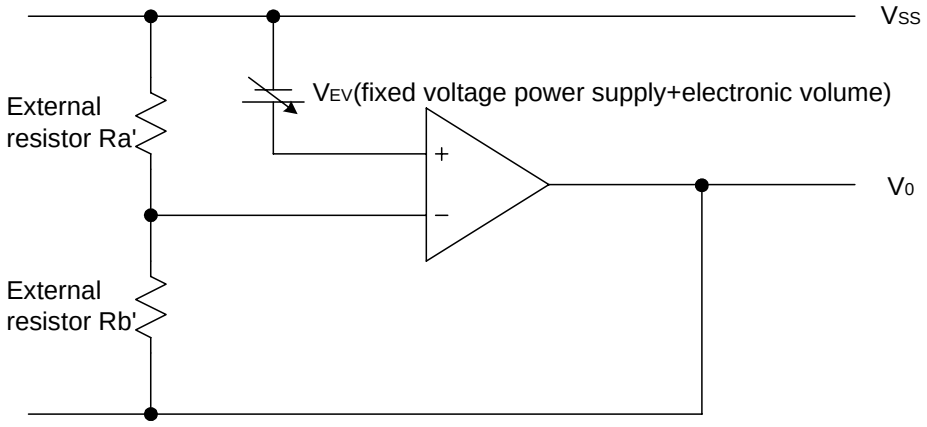


Figure 11

Setup example: When selecting Ta = 25°C and V_0 = 7 V for ST7565R the temperature gradient = –0.05%/°C.

When the central value of the electron volume register is (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then α = 31 and V_{REG} = 2.1V so, according to equation B-1,

$$V_0 = \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$7V = \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet (2.1)$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5 uA,

$$Ra' + Rb' = 1.4M\Omega \qquad \text{(Equation B-3)}$$

Consequently, by equations B-2 and B-3,

$$\frac{Rb'}{Ra'} = 3.12$$

$$Ra' = 340k\Omega$$

$$Rb' = 1060k\Omega$$

At this time, the V0 voltage variable range and notch width, based on the electron volume function, is as given in Table 14.

Table 14

V_0	Min	Typ	Max	Units
Variable Range	5.3 (63 levels)	7.0 (central value)	8.6 (0 level)	[V]
Notch width		52		[mV]

(C) When External Resistors are Used (The V_0 Voltage Regulator Internal Resistors Are Not Used) (2)

When the external resistor described above are used, adding a variable resistor as well makes it possible to perform fine adjustments on Ra' and Rb', to set the liquid crystal drive voltage V_0. In this case, the use of the electronic volume function makes it possible to control the liquid crystal power supply voltage V_0 by commands to adjust the liquid crystal display brightness.

In the range where $|V_0| < |V_{OUT}|$ the V_0 voltage can be calculated by equation C-1 below based on the R_1 and R_2 (variable resistor) and R_3 settings, where R_2 can be subjected to fine adjustments (ΔR_2).

$$V_0 = \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$

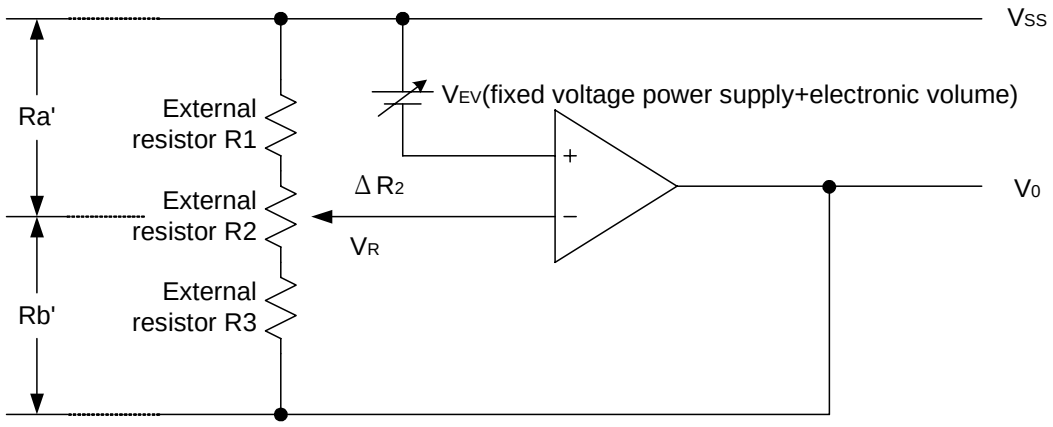


Figure 12

Setup example: When selecting Ta = 25°C and V_0= 5 to 9 V (using R2) for an ST7565R the temperature gradient = –0.05%/°C.

When the central value for the electronic volume register is set at (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then α = 31 and V_{REG} = 2.1 V so, according to equation C-1, when ΔR_2 = 0 Ω, in order to make V_0 = 9 V,

$$9V = \left(1 + \frac{R3+R2}{R1}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet (2.1)$$

When $\Delta R_2 = R_2$, in order to make V = –5 V,

$$5V = \left(1 + \frac{R3}{R1+R2}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet (2.1)$$

When the current flowing V_{DD} and V_0 is set to 5 uA,

$$R_1 + R_2 + R_3 = 1.4M\Omega \qquad \text{(Equation C-4)}$$

With this, according to equation C-2, C-3 and C-4,

$$R1 = 264k\Omega$$

$$R2 = 211k\Omega$$

$$R3 = 925k\Omega$$

The V_0 voltage variable range and notch width based on the electron volume function is as shown in Table 15.

Table 15

V_0	Min	Typ	Max	Units
Variable Range	5.3 (63 levels)	7.0 (central value)	8.7 (0 level)	[V]
Notch width		53		[mV]

* When the V_0 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from V_{OUT} when the Booster circuit is OFF.
* The V_R terminal is enabled only when the V_0 voltage regulator internal resistors are not used (i.e. the IRS terminal = "L"). When the V_0 voltage regulator internal resistors are used (i.e. when the IRS terminal = "H"), then the V_R terminal is left open.
* Because the input impedance of the V_R terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

The LCD Voltage Generator Circuit

The V_0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V_1, V_2, V_3, and V_4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V_1, V_2, V_3 and V_4 to the liquid crystal drive circuit.

High Power Mode

The power supply circuit equipped in the ST7565R chips has very low power consumption (normal mode: HPM = "H"). **However, for LCD panels with large loads (size), this low-power power supply may cause display quality to degrade. When this occurs, set the HPM terminal to "L" (high power mode) can improve the display quality.** SITRONIX recommends that the display be checked on actual equipment to determine whether or not to use this mode. Moreover, if the improvement to the display is inadequate even after high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally.

The Internal Power Supply Shutdown Command Sequence

The sequence shown in Figure 13 is recommended for shutting down the internal power supply, first placing the internal power supply in power saver mode and then turning the internal power supply OFF. The power consumption can be reduced by this sequence. Please refer to the "Sleep Mode Set" section for the detailed power saving information.

Sequence	Details (Command, status)	Command address D7 D6 D5 D4 D3 D2 D1 D0	
Step1	Display OFF	1 0 1 0 1 1 1 0	Power saver
Step2	Display all points ON	1 0 1 0 0 1 0 1	commands
End	Internal power supply OFF		(compound)

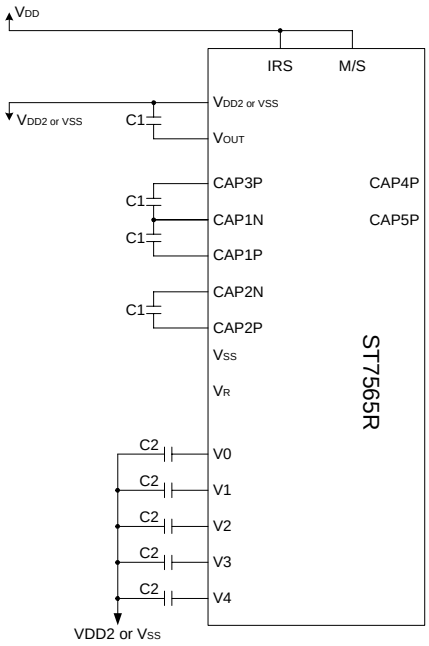
Figure 13

Reference Circuit Examples

1. When used all of the step-up circuit, voltage regulating circuit and V/F circuit

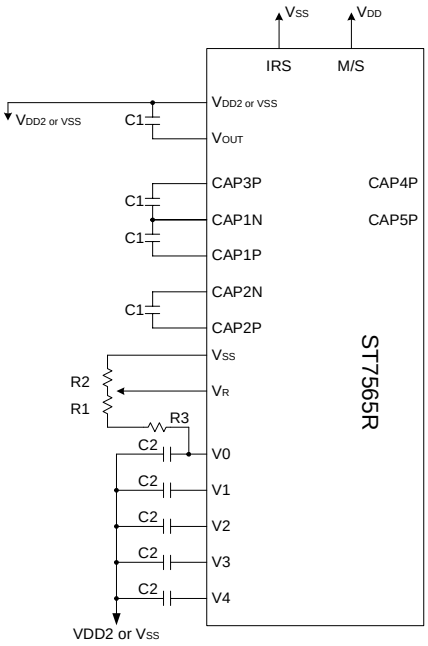
(1) When the voltage regulator internal resistor is used.

(Example where $V_{DD}2 = V_{DD}$, with 4x step-up)



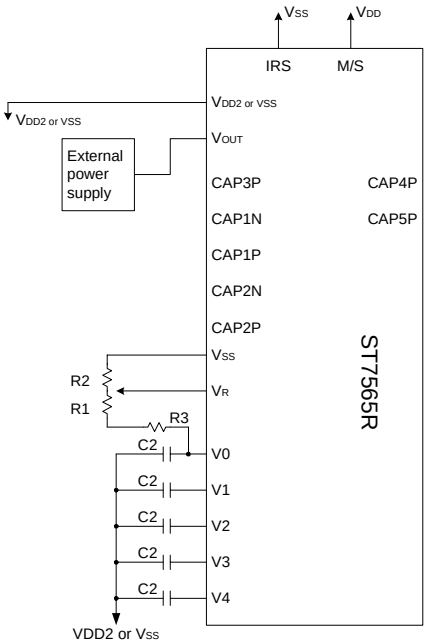
(2) When the voltage regulator internal resistor is not used.

(Example where $V_{DD}2 = V_{DD}$, with 4x step-up)

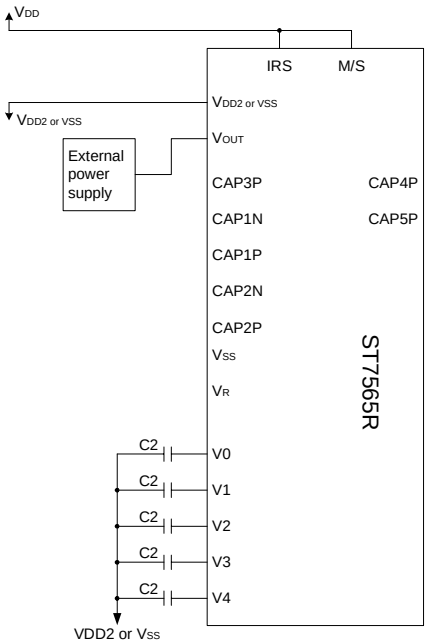


2. When the voltage regulator circuit and V/F circuit alone are used

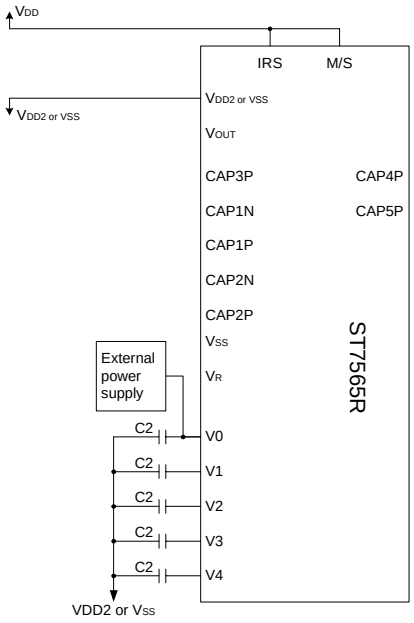
(1) When the V_0 voltage regulator internal resistor is not used.



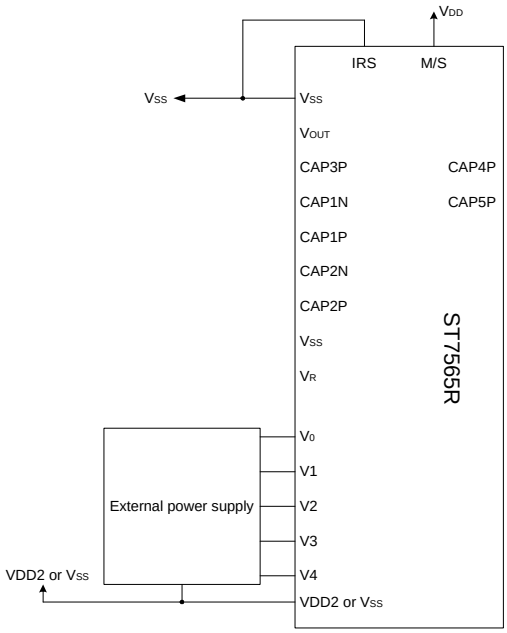
(2) When the V_0 voltage regulator internal resistor is used.



(3) When the V/F circuit alone is used



(4) When the built-in power is not used



Item	Set value	unit
C1	1 ~ 2.2	uF
C2	0.1 ~ 1	uF

Note:

- C1 ~ C2 are determined by the size of the LCD being driven.
- The recommended panel size is smaller than 1.8".
- If the panel loading is too heavy and cause poor display quality, adding V0 capacitor can improve display quality.

* 1. Because the VR terminal input impedance is high, use short leads and shielded lines.
* 2. C1 ~ C2 are determined by the LCD loading (size). Select a suitable value that matches the module.

Example of the Process by which to Determine the Settings:

• Turn the voltage regulator circuit and voltage follower circuit ON and supply a voltage to VOUT from the outside.
• Determine C2 by displaying an LCD pattern with a heavy load (such as horizontal stripes) and selecting the capacitor that stabilizes the liquid crystal drive voltages (V_0 to V_4). Note that all C2 capacitors must have the same capacitance value.
• Next, remove external VOUT and turn all internal power supplies ON and then select C1.

The Reset Circuit

When the /RES input comes to the “L” level, these LSIs return to the default state. Their default states are as follows:

1. Display OFF
2. Normal display
3. ADC select: Normal (ADC command D0 = “L”)
4. Power control register: (D2, D1, D0) = (0, 0, 0)
5. 4-line SPI interface internal register data clear
6. LCD power supply bias rate:
   1/65 DUTY = 1/9 bias
   1/49,1/55,1/53 DUTY = 1/8 bias
   1/33 DUTY = 1/6 bias
7. Power saving clear
8. V_0 voltage regulator internal resistors Ra and Rb separation
9. Output conditions of SEG and COM terminals SEG=VSS, COM=VSS
10. Read modify write OFF
11. Display start line set to first line
12. Column address set to Address 0
13. Page address set to Page 0
14. Common output status normal
15. V_0 voltage regulator internal resistor ratio set mode clear
16. Electronic volume register set mode clear Electronic volume register :
(D5, D4, D3, D2, D1, D0) = (1, 0. 0, 0, 0,0)
17. Test mode clear

On the other hand, when the reset command is used, the above default settings from 11 to 17 are only executed. When the power is turned on, the IC internal state becomes unstable, and it is necessary to initialize it using the /RES terminal. After the initialization, each input terminal should be controlled normally.

Moreover, when the control signal from the MPU is in the high impedance, an over current may flow to the IC. After applying a current, it is necessary to take proper measures to prevent the input terminal from getting into the high impedance state.

If the internal liquid crystal power supply circuit is not used on ST7565R,it is necessary that /RES is “H” when the external liquid crystal power supply is turned on. This IC has the function to discharge V_0 when /RES is “L,” and the external power supply short-circuits to V_{SS} when /RES is “L.” While /RES is “L,” the oscillator and the display timing generator stop, and the CL, FR and /DOF terminals are fixed to “H.” The terminals D0 to D7 are not affected. The V_{SS} level is output from the SEG and COM output terminals. This means that an internal resistor is connected between V_{SS} and V_0.

When the internal liquid crystal power supply circuit is not used on other models of ST7565R series, it is necessary that /RES is “L” when the external liquid crystal power supply is turned on.

While /RES is “L,” the oscillator works but the display timing generator stops, and the CL, FR and /DOF terminals are fixed to “H.” The terminals D0 to D7 are not affected.

Commands

The ST7565R identify the data bus signals by a combination of A0, /RD (E), /WR(R/W) signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.
In the 8080 MPU interface, commands are launched by inputting a low pulse to the RD terminal for reading, and inputting a low pulse to the /WR terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an "H" signal is input to the R/W terminal and placed in a write mode when a "L" signal is input to the R/W terminal and then the command is launched by inputting a high pulse to the E terminal. Consequently, the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that in the explanation of commands and the display commands the status read and display data read /RD (E) becomes "1(H)". In the explanations below the commands are explained using the 8080 Series MPU interface as the example.
When the 4-line SPI interface is selected, the data is input in sequence starting with D7.
<Explanation of Commands>

Display ON/OFF

This command turns the display ON and OFF.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1 0	Display ON Display OFF

When the display OFF command is executed when in the display all points ON mode, sleep mode is entered. See the section on the Sleep Mode Set for details.

Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. For further details see the explanation of this function in "The Line Address Circuit".

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0 0 0 1 1	0 0 0 ↓ 1 1	0 0 0 1 1	0 0 0 1 1	0 0 1 1 1	0 1 0 0 1	0 1 2 ↓ 62 63

Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 4). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0 0 0 ↓ 0 1	0 0 0 1 0	0 0 1 1 0	0 1 0 1 0	0 1 2 ↓ 7 8

Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not change the page address continuously. See the function explanation in "The Column Address Circuit," for details.

	A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column address
High bits →	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
															↓					↓
												1	0	0	0	0	0	1	0	130
												1	0	0	0	0	0	1	1	131

Status Read

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	BUSY = 1: it indicates that either processing is occurring internally or a reset condition is in process. BUSY = 0: A new command can be accepted . if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Normal (column address n ↔ SEG n) 1: Reverse (column address 131-n ↔ SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a /RES signal or because of a reset command. 0: Operating state 1: Reset in progress

Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by "1" after the write, the MPU can write the display data.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by "1" after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the function explanation in "Display Data RAM" for the explanation of accessing the internal registers. When the 4-line SPI interface is used, reading of the display data becomes unavailable.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit for the detail. Increment of the column address (by "1") accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data "H" LCD ON voltage (normal)
										1	RAM Data "L" LCD ON voltage (reverse)

Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in sleep mode. For details, see the Sleep Mode Set section.

LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Select Status				
											1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/8 bias	1/6 bias	1/8 bias	1/8 bias
										1	1/7 bias	1/6 bias	1/5 bias	1/6 bias	1/6 bias

Read-Modify-Write

This command is used paired with the "END" command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the Read-Modify-Write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used.

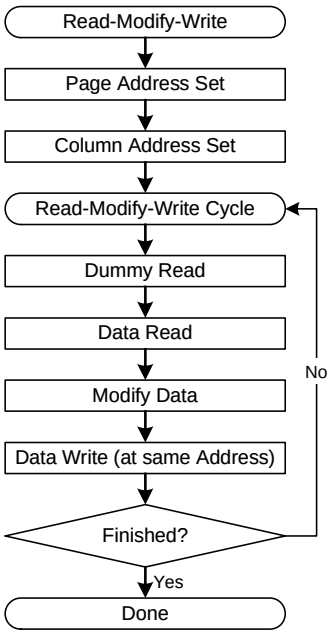


Figure 24 Command Sequence For read modify write

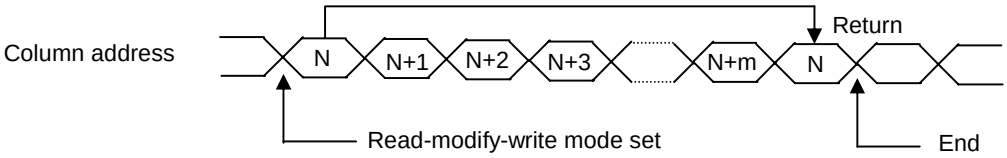


Figure 25

End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

Reset

This command initializes the display start line, the column address, the page address, the common output mode, the V_0 voltage regulator internal resistor ratio, and the electronic volume are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in “Reset” for details. The reset operation is performed after the reset command is entered.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the /RES terminal. The reset command must not be used instead.

Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation in "Common Output Mode Select Circuit."

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode					
												1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0	1	0	1	1	0	0	0	*	*	*	Normal	COM0→COM63	COM0→COM47	COM0→COM31	COM0→COM53	COM0→COM51
							1				Reverse	COM63→COM0	COM47→COM0	COM31→COM0	COM53→COM0	COM51→COM0

* Disabled bit

Power Controller Set

This command sets the power supply circuit functions. See the function explanation in "The Power Supply Circuit," for details

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
								1			Booster circuit: ON
									0		Voltage regulator circuit: OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

V_0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V_0 voltage regulator internal resistor ratio. For details, see the function explanation is "The Voltage Regulator circuit " and table 11 .

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
						↓					↓
								1	1	1	
								1	1	1	Large

The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the LCD drive voltage V_0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V_0 assumes one of the 64 voltage levels.
When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	| V0 |
			*	*	0	0	0	0	0	1	Small
			*	*	0	0	0	0	1	0	
0	1	0	*	*	0	0	0	0	1	1	
									↓		↓
			*	*	1	1	1	1	1	0	
			*	*	1	1	1	1	1	1	Large

* Inactive bit (set “0”)
When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

The Electronic Volume Register Set Sequence

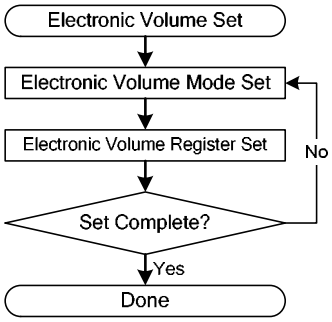


Figure 26

Sleep Mode Set (Double Byte Command)

This command is a two byte command used as a pair with preceding command and following command, and both commands must issued one after the other.
This command stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:
1. The oscillator circuit and the LCD power supply circuit are halted.
2. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a Vss level.

	A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Status
Preceding Command	0	1	0	1	0	1	0	1	1	0	0 1	Sleep Mode Normal Mode
Following Command				*	*	*	*	*	*	0	0	

*Disable bit (set “0”)

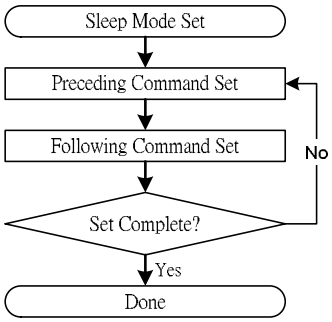


Figure 27

In the sleep mode, the MPU is still able to access the display data RAM.
Refer to figure 28 for sleep mode sequence.

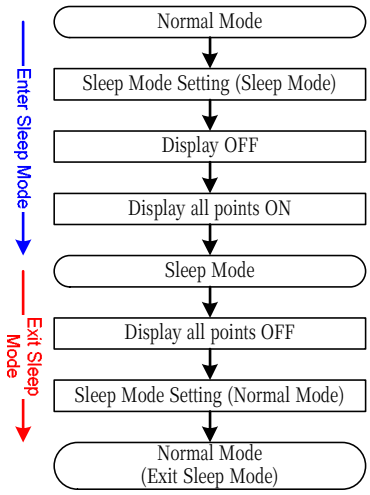


Figure 28

The Booster Ratio (Double Byte Command)

This command makes it possible to select step-up ratio. It is used when the power control set have turn on the internal booster circuit. This command is a two byte command used as a pair with the booster ratio select mode set command and the booster ratio register set command, and both commands must be issued one after the other.

Booster Ratio Select Mode Set

When this command is input, the Booster ratio register set command becomes enabled. Once the booster ratio select mode has been set, no other command except for the booster ratio register command can be used. Once the booster ratio register set command has been used to set data into the register, then the booster ratio select mode is released.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	0	0	0

Booster Ratio Register Set

By using this command to set two bits of data to the booster ratio register, it can be select what kind of the booster ratio can be used.
When this command is input, the booster ratio select mode is released after the booster ratio register has been set.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Booster ratio select
0	1	0	*	*	*	*	*	*	0	0	2x,3x,4x
			*	*	*	*	*	*	0	1	5x
			*	*	*	*	*	*	1	1	6x

* Inactive bit (set “0”)
When the booster ratio select function is not used, set this to (0, 0) 2x,3x,4x step-up mode

The booster ratio Register Set Sequence

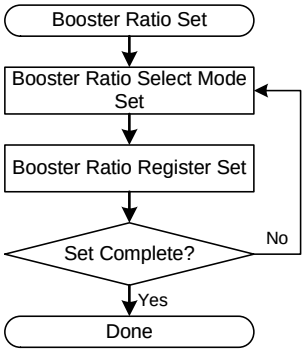


Figure 29

NOP

Non-Operation Command

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

Test

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a “L” signal to the /RES input by the reset command or by using an NOP.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	1	*	*

* Inactive bit

Note: The ST7565R maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the ST7565R . Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

Table 16: Table of ST7565R Commands (Note) *: ignored data

Command	Command Code											Function
	A0	**/RD**	**/WR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0	1	0	0 0	0 0	0 0	1 0	Most significant column address Least significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565R)
(12) Read-modify-write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V_0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0	0	0 Electronic volume value	0	0	1	Set the V_0 output voltage electronic volume register
(19) Sleep mode set	0	1	0	1 * *	0 * *	1 * *	0 * *	1 * *	1 * *	0 0 0	0 1 0	0: Sleep mode, 1: Normal mode
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

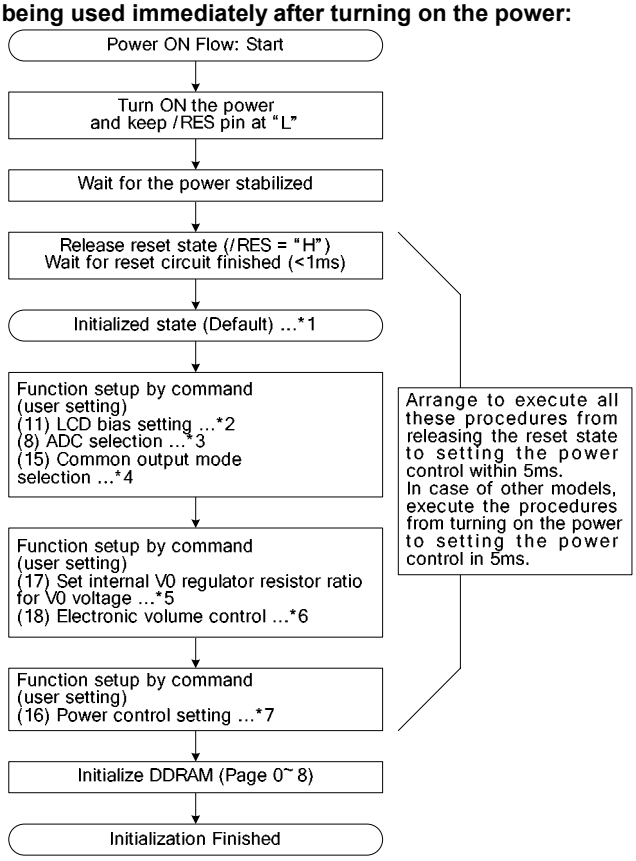
Command Description

Instruction Setup: Reference

(1) Initialization

Note: With this IC, when the power is applied, LCD driving non-selective potentials V_2 and V_3 (SEG pin) and V_1 and V_4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V_0 ~ V_4) and the V_{SS} pin, the picture on the display may become totally dark instantaneously when the power is turned on. To avoid occurrence of such a failure, we recommend the following flow when turning on the power.

1. When the built-in power is being used immediately after turning on the power:

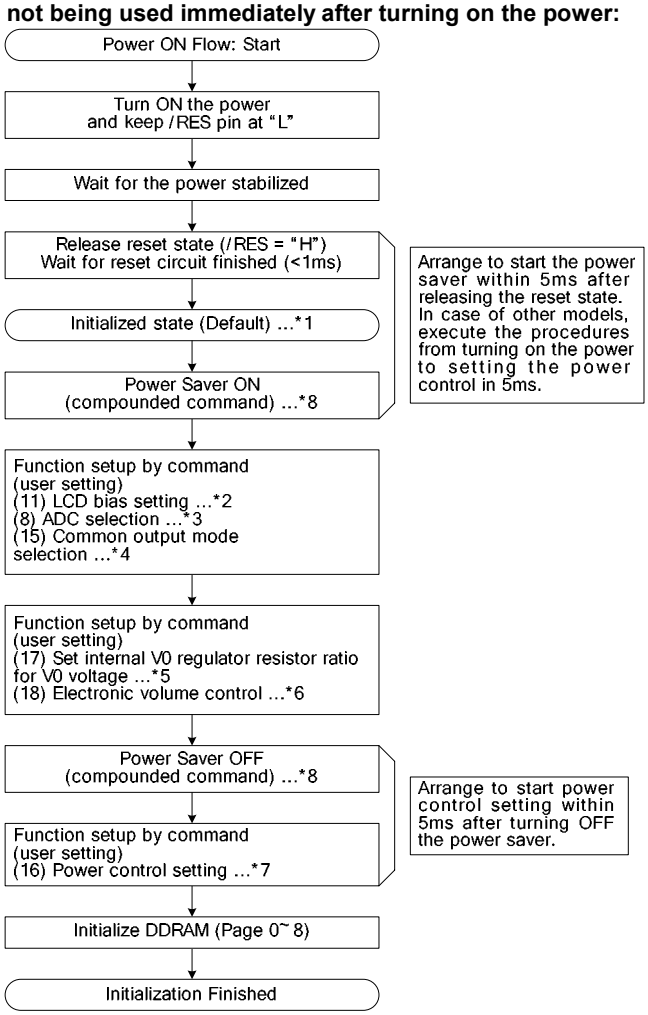


* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: Description of functions; Resetting circuit
*2: Command description; LCD bias setting
*3: Command description; ADC selection
*4: Command description; Common output state selection
*5: Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V_0 voltage
*6: Description of functions; Power circuit & Command description; Electronic volume control
*7: Description of functions; Power circuit & Command description; Power control setting

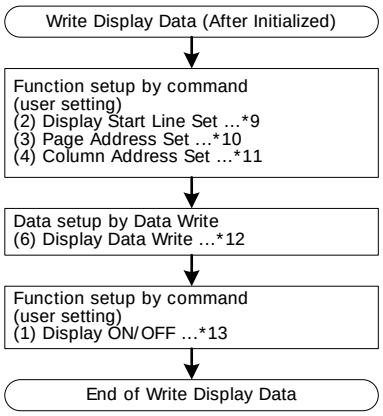
2. When the built-in power is not being used immediately after turning on the power:



* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.
*1: Description of functions; Resetting circuit
*2: Command description; LCD bias setting
*3: Command description; ADC selection
*4: Command description; Common output state selection
*5: Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V_0 voltage
*6: Description of functions; Power circuit & Command description; Electronic volume control
*7: Description of functions; Power circuit & Command description; Power control setting
*8: Command description; Sleep mode (multiple commands)

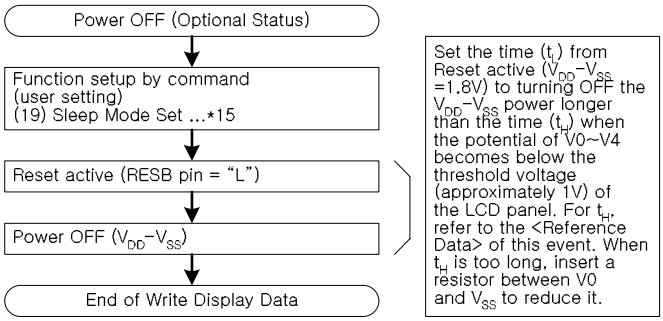
(2) Data Display



Notes: Reference items

*9: Command Description; Display start line set
*10: Command Description; Page address set
*11: Command Description; Column address set
*12: Command Description; Display data write
*13: Command Description; Display ON/OFF
Avoid displaying all the data at the data display start (when the display is ON) in white.

(3) Power OFF *14

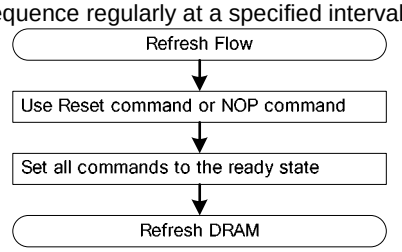


Notes: Reference items

*14: The logic circuit of this IC's power supply V_{DD} - V_{SS} controls the driver of the LCD power supply V_{SS} –V_0. So, if the power supply V_{DD} - V_{SS} is cut off when the LCD power supply V_{SS} –V_0 has still any residual voltage, the driver (COM. SEG) may output any uncontrolled voltage. When turning off the power, observe the following basic procedures:
• After turning off the internal power supply, make sure that the potential V_0 ~ V_4 has become below the threshold voltage of the LCD panel, and then turn off this IC's power supply (V_{DD} - V_{SS}). 6. Description of Function, 6.7 Power Circuit
*15: After inputting the power save command, be sure to reset the function using the /RES terminal until the power supply V_{DD} - V_{SS} is turned off. 7. Command Description (19) Sleep Mode Set
*16: After inputting the power save command, do not reset the function using the /RES terminal until the power supply V_{DD} - V_{SS} is turned off. 7. Command Description (19) Sleep Mode Set

Refresh

It is recommended to turn on the refresh sequence regularly at a specified interval.



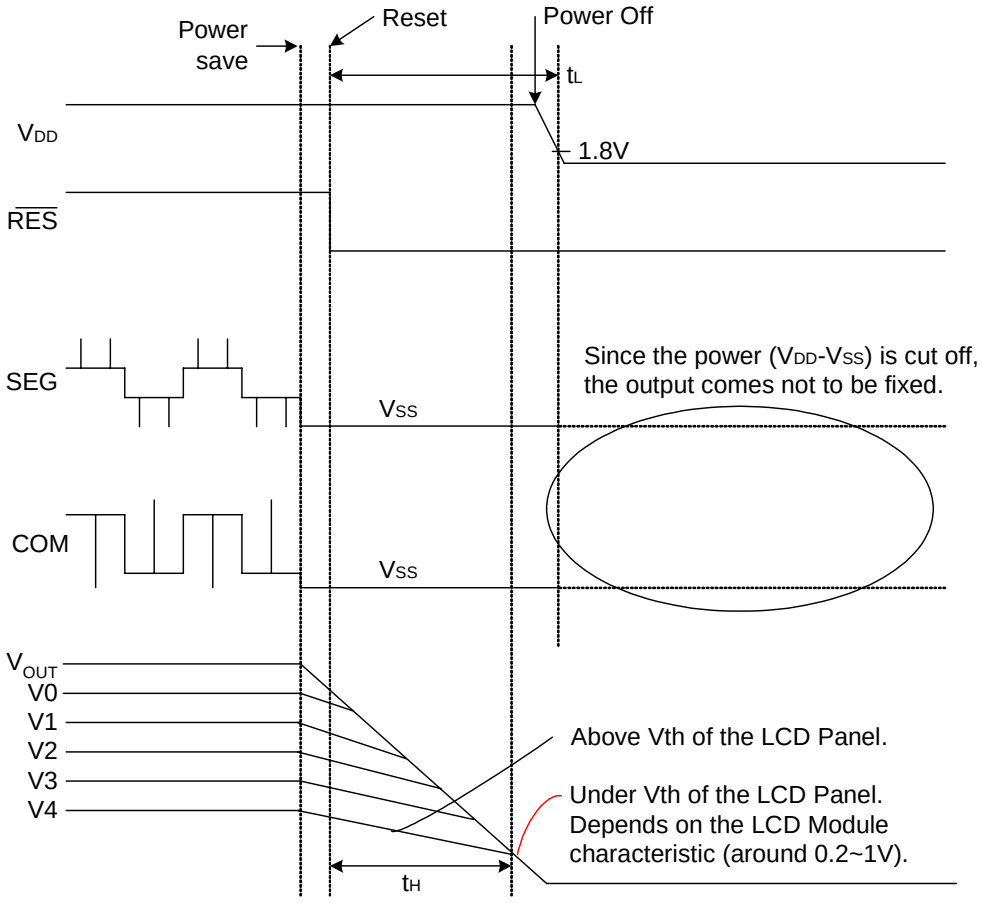
Precautions on Turning off the power

<Turning the power (V_{DD} - V_{SS}) off>
1) Power Save (The LCD powers (V_0 - V_{SS}) are off.) → Reset input → Power (V_{DD} - V_{SS}) OFF

• Observe $t_L > t_H$.

• When $t_L < t_H$, an irregular display may occur.

Set t_L on the MPU according to the software. t_H is determined according to the external capacity C2 (smoothing capacity of V_0 ~ V_4) and the driver's discharging capacity.



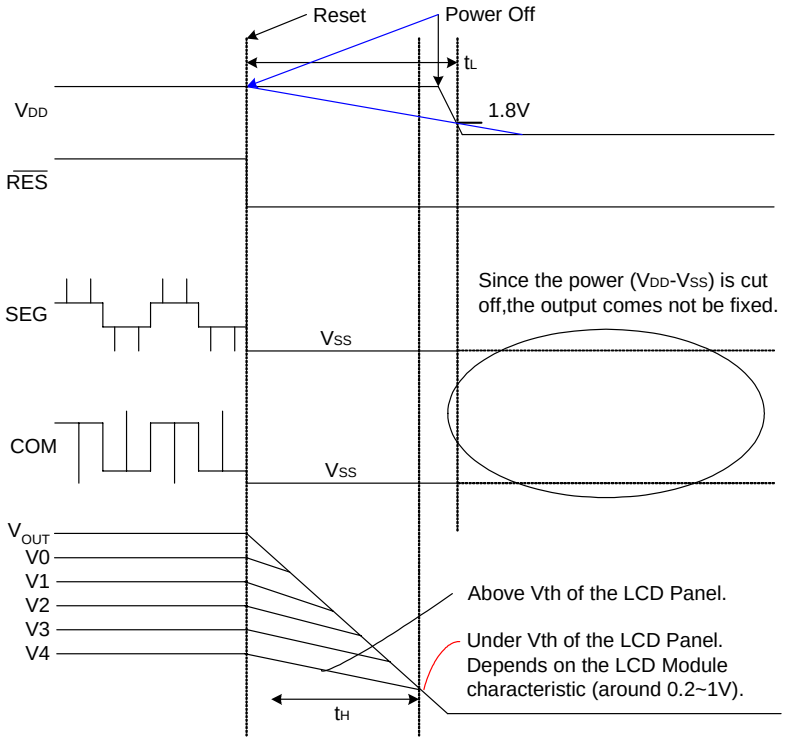
<Turning the power (V_{DD} - V_{SS}) off : When command control is not possible.>
2) Reset (The LCD powers (V_{DD} - V_{SS}) are off.) → Power (V_{DD} - V_{SS}) OFF

• Observe $t_L > t_H$.

• **When $t_L < t_H$, an irregular display may occur.**

For t_L, make the power (V_{DD} - V_{SS}) falling characteristics longer or consider any other method.

t_H is determined according to the external capacity C2 (smoothing capacity of V_0 to V_4) and the driver's discharging capacity.



<Reference Data>

V_0 voltage falling (discharge) time (t_H) after the process of operation → power save → reset.

V_0 voltage falling (discharge) time (t_H) after the process of operation → reset.

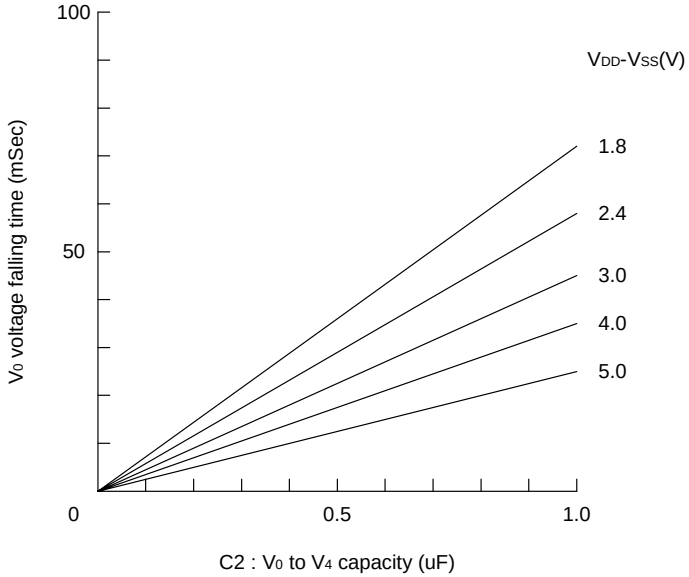


Figure 31

Absolute Maximum Ratings

Unless otherwise noted, V_{SS} = 0V

Table 17

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		V_{DD}	-0.3 ~ 3.6	V
Power supply voltage (V_{DD} standard)		VDD2	-0.3 ~ 3.6	V
Power supply voltage (V_{DD} standard)		V_0, V_{OUT}	-0.3 ~ 13.5	V
Power supply voltage (V_{DD} standard)		V_1, V_2, V_3, V_4	-0.3 to V_0	V
Operating temperature		T_{OPR}	–30 to +85	°C
Storage temperature	Bare chip	T_{STR}	–65 to +150	°C

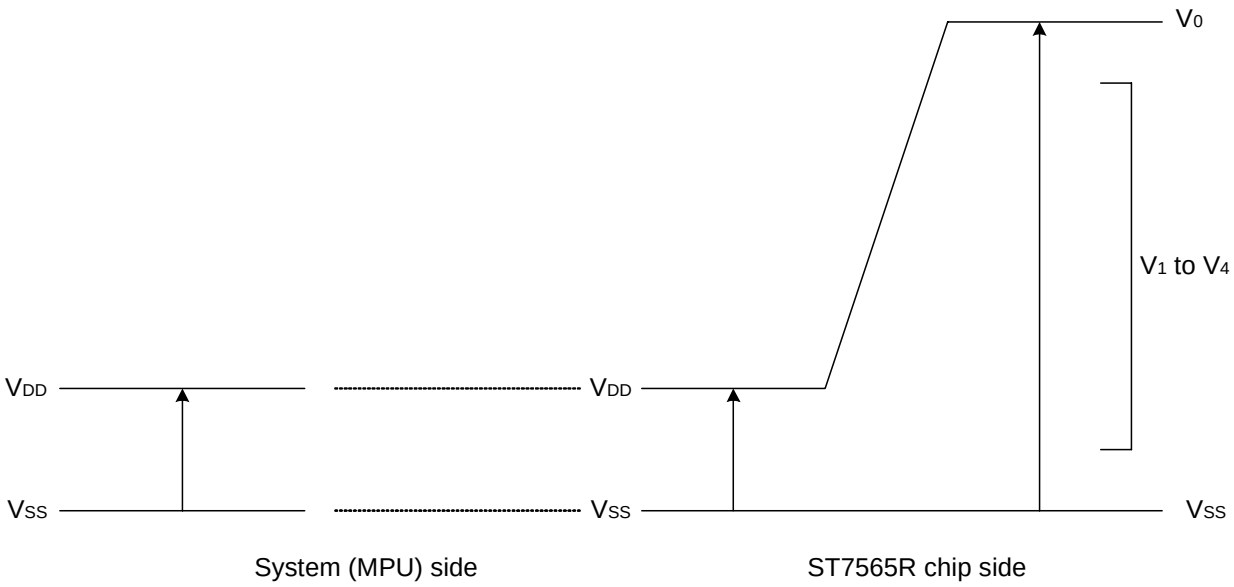


Figure 30

Notes and Cautions

1. The V_{DD2}, V_0 to V_4 and V_{OUT} are relative to the V_{SS} = 0V reference.
2. Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that $V_{OUT} \geqq V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4$.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

DC Characteristics

Unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3.0 V, Ta = –30 to 85°C

Table 18

Item		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Units	Applicable Pin
Operating Voltage (1)		V_{DD}			2.4	—	3.3	V	V_{DD}*1
Operating Voltage (2)		V_{DD2}	(Relative to V_{SS})		2.4	—	3.3	V	V_{DD}
High-level Input Voltage		V_{IHC}			0.8 x V_{DD}	—	V_{DD}	V	*3
Low-level Input Voltage		V_{ILC}			V_{SS}	—	0.2 x V_{DD}	V	*3
High-level Output Voltage		V_{OHC}	I_{OH} = –0.5 mA		0.8 x V_{DD}	—	V_{DD}	V	*4
Low-level Output Voltage		V_{OLC}	I_{OL} = 0.5 mA		V_{SS}	—	0.2 x V_{DD}	V	*4
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		–1.0	—	1.0	µA	*5
Output leakage current		I_{LO}	V_{IN} = V_{DD} or V_{SS}		–3.0	—	3.0	µA	*6
Liquid Crystal Driver ON Resistance		R_{ON}	Ta = 25°C (Relative to V_{SS})	V_0 = 13.0 V	—	2.0	3.5	KΩ	SEGn COMn *7
				V_0 = 8.0 V	—	3.2	5.4		
Static Consumption Current		I_{SSQ}	V_0 = 13.0 V (Relative To V_{SS})		—	0.01	2	µA	V_{DD}, V_{DD2}
Output Leakage Current		I_{0Q}			—	0.01	10	µA	V_0
Input Terminal Capacitance		C_{IN}	Ta = 25°C, f = 1 MHz		—	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	f_{OSC}	1/65 duty 1/33 duty	Ta = 25°C	17	20	24	kHz	*8
	External Input	f_{CL}			17	20	24	kHz	CL
	Internal Oscillator	f_{OSC}	1/49 duty 1/53 duty 1/55 duty	Ta = 25°C	25	30	35	kHz	*8
	External Input	f_{CL}			25	30	35	kHz	CL

Table 19

Item		Symbol	Condition	Rating Min.	Rating Typ.	Rating Max.	Units	Applicable Pin
Internal Power	Input voltage	V_{DD2}	(Relative To V_{SS})	2.4	—	3.3	V	V_{DD}
	Supply Step-up output voltage Circuit	V_{OUT}	(Relative To V_{SS})	—	—	13.5	V	V_{OUT}
	Voltage regulator Circuit Operating Voltage	V_{OUT}	(Relative To V_{SS})	6.0	—	13.5	V	V_{OUT}
	Voltage Follower Circuit Operating Voltage	V_0	(Relative To V_{SS})	4.0	—	13.5	V	V_0 * 9
	Base Voltage	VRS	Ta = 25°C, (Relative To V_{SS}) –0.05%/°C	2.07	2.10	2.13	V	*10

• Dynamic Consumption Current : During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used .

Table 20

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern OFF	I_{DD}	V_{DD} = 3.0 V, $V_0 – V_{SS}$ = 11.0 V	—	16	27	µA	*11
Display Pattern Checker	I_{DD}	V_{DD} = 3.0 V, $V_0 – V_{SS}$ = 11.0 V	—	19	32	µA	*11

• Dynamic Consumption Current : During Display, with the Internal Power Supply ON

Table 21

Test pattern	Symbol	Condition		Rating			Units	Notes
				Min.	Typ.	Max.		
Display Pattern OFF	I_{DD}	V_{DD} = 3.0 V, Quad step-up voltage. $V_0 – V_{SS}$ = 11.0 V	Normal Mode	—	90	130	µA	*12
			High-Power Mode	—	128	193		
Display Pattern Checker	I_{DD}	V_{DD} = 3.0 V, Quad step-up voltage. $V_0 – V_{SS}$ = 11.0 V	Normal Mode	—	100	147	µA	*12
			High-Power Mode	—	135	205		

• Consumption Current at Time of Power Saver Mode : VDD = 3.0 V

Table 22

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Sleep mode	I_{DD}	Ta = 25°C	—	0.1	4	µA	

• The Relationship Between Oscillator Frequency f_{OSC}, Display Clock Frequency f_{CL} and the Liquid Crystal Frame Rate Frequency f_{FR}

Table 23

Item		f_{CL}	f_{FR}
1/65 DUTY	Used internal oscillator circuit	f_{OSC} / 4	f_{OSC} / (4*65)
	Used **externa**l display clock	External input (f_{CL})	f_{CL} / 260
1/49 DUTY	Used internal oscillator circuit	f_{OSC} / 4	f_{OSC} / (4*49)
	Used **external** display clock	External input (f_{CL})	f_{CL} / 196
1/33 DUTY	Used internal oscillator circuit	f_{OSC} / 8	f_{OSC} / (8*33)
	Used **external** display clock	External input (f_{CL})	f_{CL} / 264
1/55 DUTY	Used internal oscillator circuit	f_{OSC} / 4	f_{OSC} / (4*55)
	Used **external** display clock	External input (f_{CL})	f_{CL} / 220
1/53 DUTY	Used internal oscillator circuit	f_{OSC} / 4	f_{OSC} / (4*53)
	Used **external** display clock	External input (f_{CL})	f_{CL} / 212

(f_{FR} is the liquid crystal alternating current period, and not the FR signal period.)

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The operating voltage range for the V_{SS} system and the V_0 system is. This applies when the external power supply is being used.

*3 The A0, D0 to D5, D6 (SCL), D7 (SI), /RD (E), /WR (R/W), /CS1, CS2, CLS, CL, FR, C86, P/S, /DOF, /RES, IRS, and /HPM terminals.

*4 The D0 to D7, FR, /DOF, and CL terminals.

*5 The A0, /RD (E), /WR (R/W), /CS1, CS2, CLS, C86, P/S, /RES, IRS, and /HPM terminals.

*6 Applies when the D0 to D5, D6 (SCL), D7 (SI), CL, FR, and /DOF terminals are in a high impedance state.

*7 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V_1, V_2, V_3, and V_4). These are specified for the operating voltage (3) range. R_{ON} = 0.1 V / ΔI (Where ΔI is the current that flows when 0.1 V is applied while the power supply is ON.)

*8 See Table 23 for the relationship between the oscillator frequency and the frame rate frequency.

*9 The V_0 voltage regulator circuit regulates within the operating voltage range of the voltage follower.

*10 This is the internal voltage reference supply for the V_0 voltage regulator circuit. In the ST7565R, the temperature range approximately –0.05%/°C.

*11, 12 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on. The ST7565R is 1/9 biased. Does not include the current due to the LCD panel capacity and wiring capacity. Applicable only when there is no access from the MPU.

*12 It is the value on a ST7565R having the V_{REG} temperature gradient is –0.05%/°C when the V_0 voltage regulator internal resistor is used.

Timing Characteristics

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

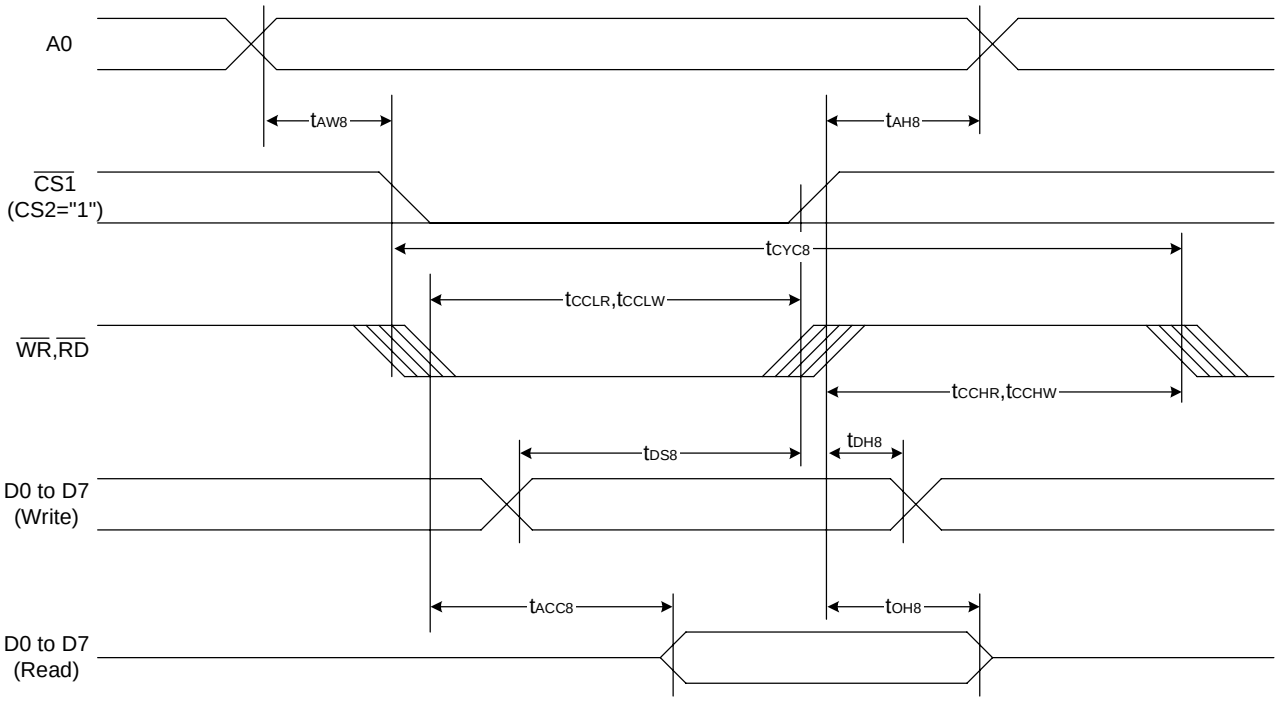


Figure 37

Table 24

(V_{DD} = 3.3V, Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	Ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		240	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		80	—	
Enable H pulse width (WRITE)		t_{CCHW}		80	—	
Enable L pulse width (READ)	RD	t_{CCLR}		140	—	
Enable H pulse width (READ)		t_{CCHR}		80		
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH8}	C_L = 100 pF	5	50	

Table 25

(V_{DD} = 2.7V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		400	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		220	—	
Enable H pulse width (WRITE)		t_{CCHW}		180	—	
Enable L pulse width (READ)	RD	t_{CCLR}		220	—	
Enable H pulse width (READ)		t_{CCHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	100	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) $\leqq$ ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for ($t_r + t_f$) $\leqq$ ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{CCLW} and t_{CCLR} are specified as the overlap between /CS1 being “L” (CS2 = “H”) and /WR and /RD being at the “L” level.

System Bus Read/Write Characteristics 2 (For the 6800 Series MPU)

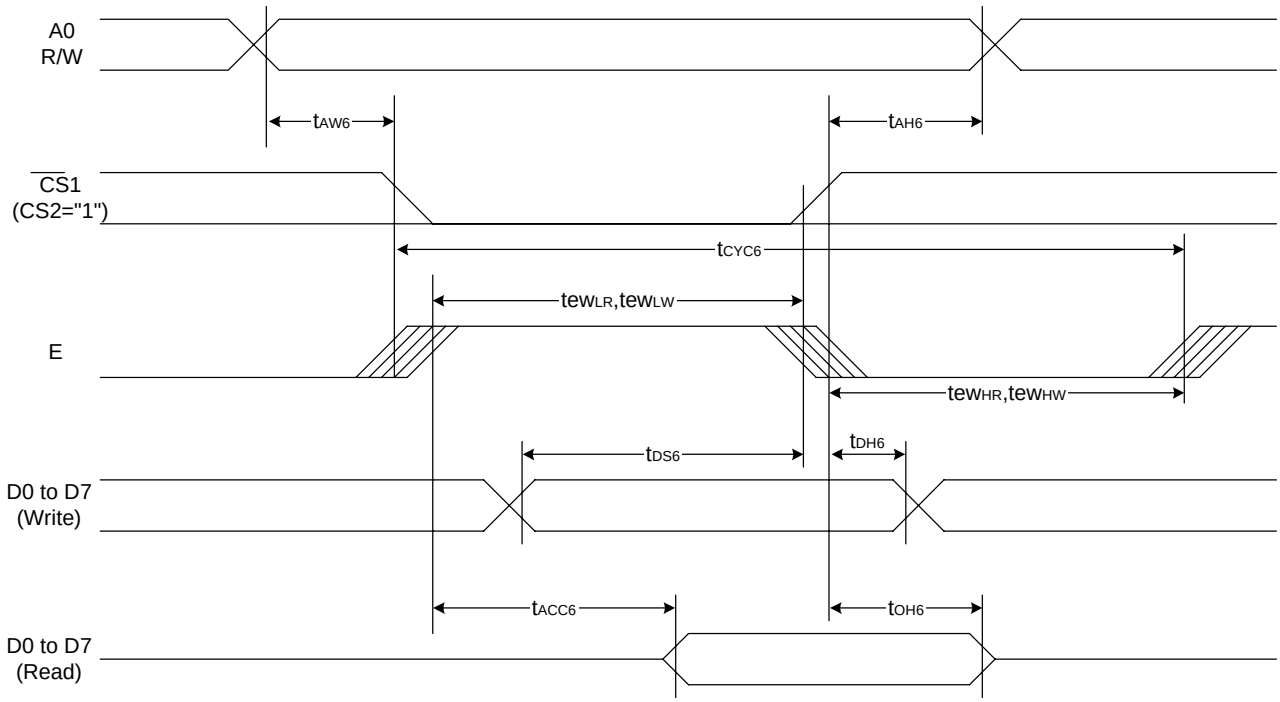


Figure 38

Table 26

(V_{DD} = 3.3V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		240	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		80	—	
Enable H pulse width (WRITE)		t_{EWHW}		80	—	
Enable L pulse width (READ)	RD	t_{EWLR}		80	—	
Enable H pulse width (READ)		t_{EWHR}		140		
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH6}	C_L = 100 pF	5	50	

Table 27

(V_{DD} = 2.7V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		400	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		220	—	
Enable H pulse width (WRITE)		t_{EWHW}		180	—	
Enable L pulse width (READ)	RD	t_{EWLR}		220	—	
Enable H pulse width (READ)		t_{EWHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	100	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) $\leqq$ ($t_{CYC6} – t_{EWLW} – t_{EWHW}$) for ($t_r + t_f$) $\leqq$ ($t_{CYC6} – t_{EWLR} – t_{EWHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being “L” (CS2 = “H”) and E.

The 4-line SPI Interface

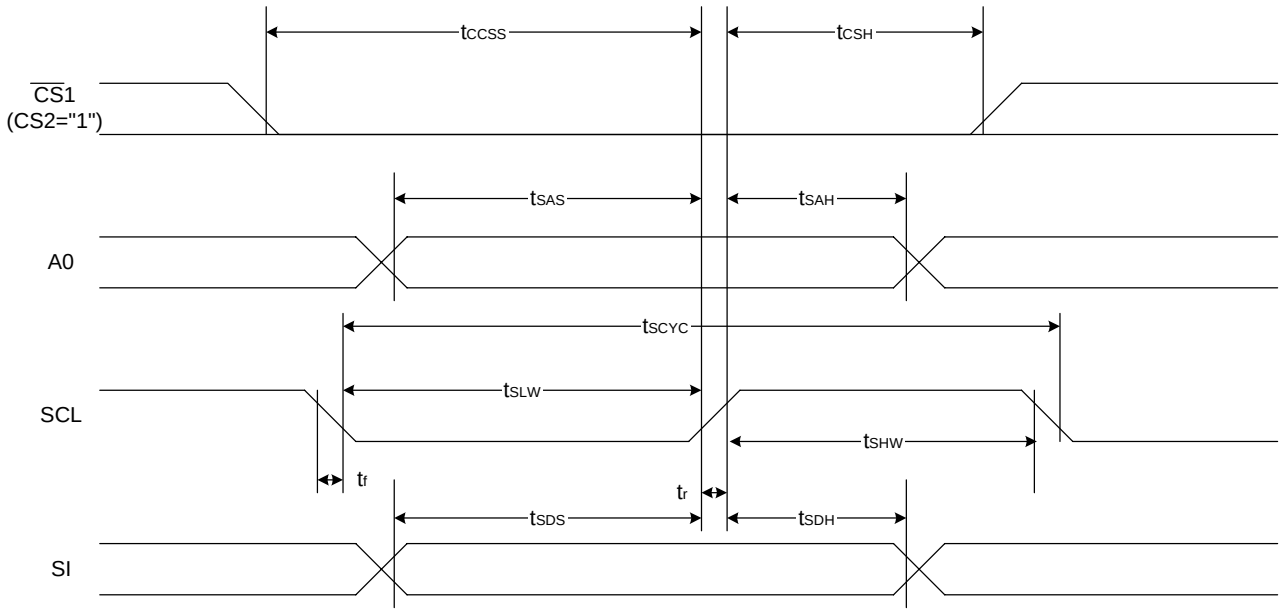


Figure 39

Table 28

(VDD = 3.3V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
4-line SPI Clock Period	SCL	Tscyc		50	—	ns
SCL “H” pulse width		Tshw		25	—	
SCL “L” pulse width		TSLW		25	—	
Address setup time	A0	TSAS		20	—	
Address hold time		Tsah		10	—	
Data setup time	SI	Tsds		20	—	
Data hold time		TSDH		10	—	
CS-SCL time	CS	Tcss		20	—	
CS-SCL time		Tcsh		40	—	

Table 29

(VDD = 2.7V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
4-line SPI Clock Period	SCL	Tscyc		100	—	ns
SCL “H” pulse width		TSHW		50	—	
SCL “L” pulse width		TSLW		50	—	
Address setup time	A0	TSAS		30	—	
Address hold time		TSAH		20	—	
Data setup time	SI	TSDS		30	—	
Data hold time		TSDH		20	—	
CS-SCL time	CS	TCSS		30	—	
CS-SCL time		TCSH		60	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
*2 All timing is specified using 20% and 80% of VDD as the standard.

Reset Timing

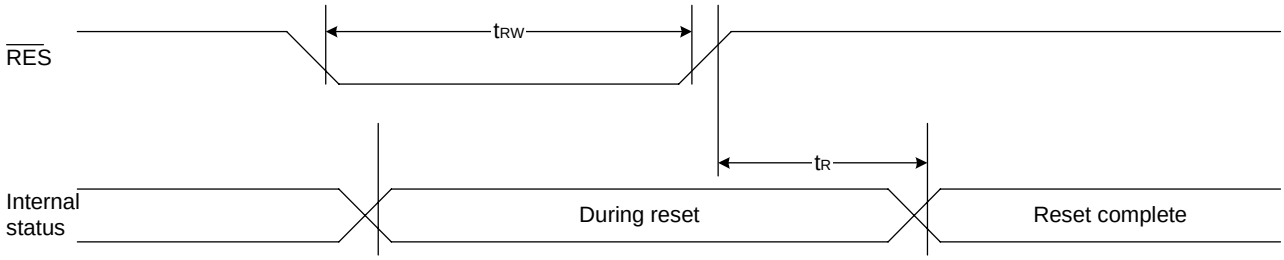


Figure 41

Table 30

(VDD = 3.3V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.0	us
Reset “L” pulse width	/RES	tRW		1.0	—	—	us

Table 31

(VDD = 2.7V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset “L” pulse width	/RES	tRW		2.0	—	—	us

*1 All timing is specified with 20% and 80% of VDD as the standard.

The MPU Interface (Reference Examples)

The ST7565R Series can be connected to either 80X86 Series MPUs or to 68000 Series MPUs. Moreover, using the 4-line SPI interface it is possible to operate the ST7565R series chips with fewer signal lines.
The display area can be enlarged by using multiple ST7565R Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

(1) 8080 Series MPUs

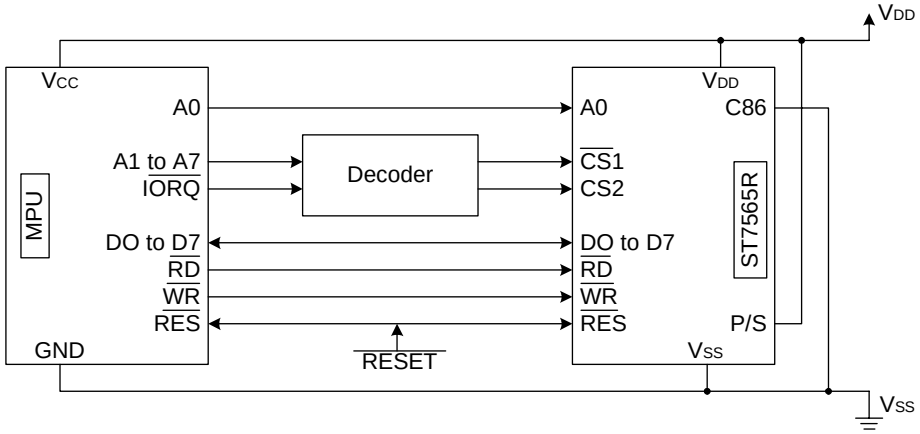


Figure 42-1

(2) 6800 Series MPUs

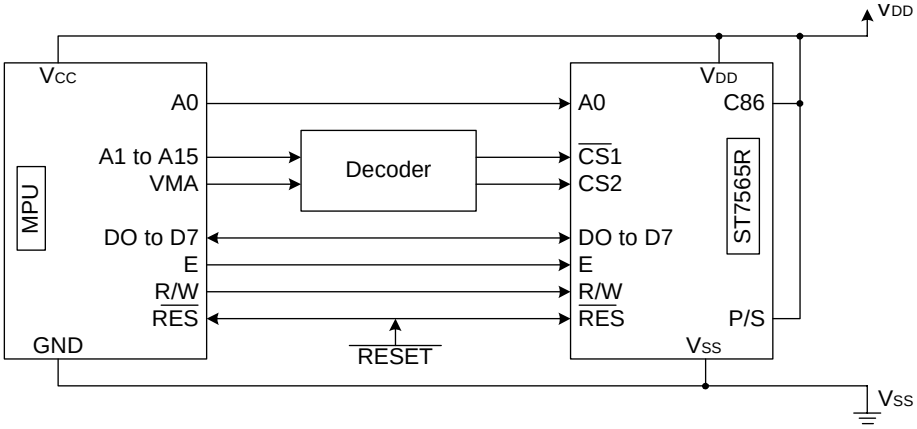


Figure 42-2

(3) Using the 4-line SPI Interface

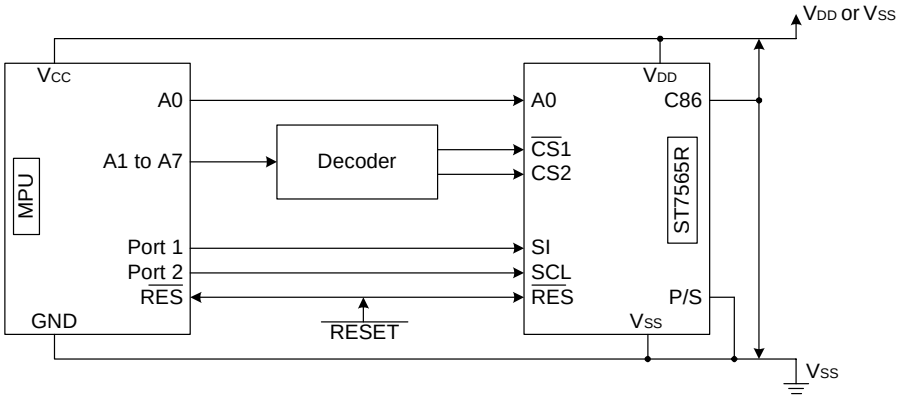


Figure 42-3

Connections Between LCD Drivers (Reference Example)

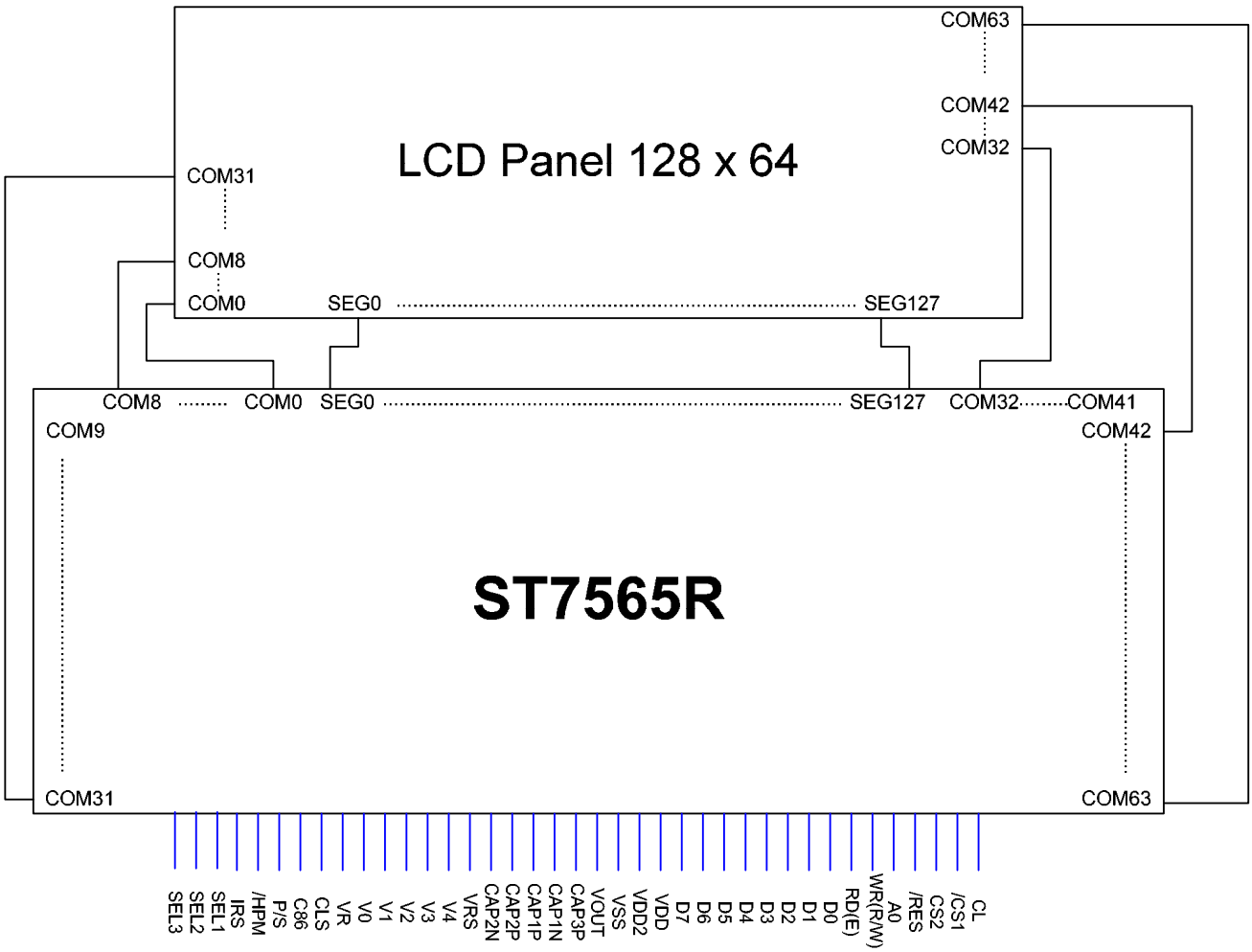
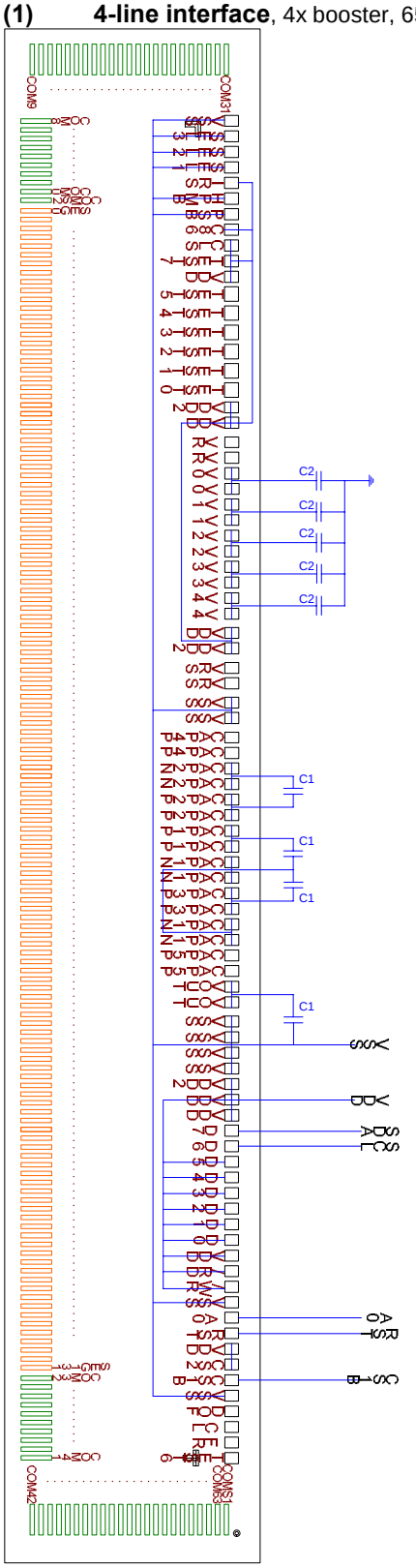


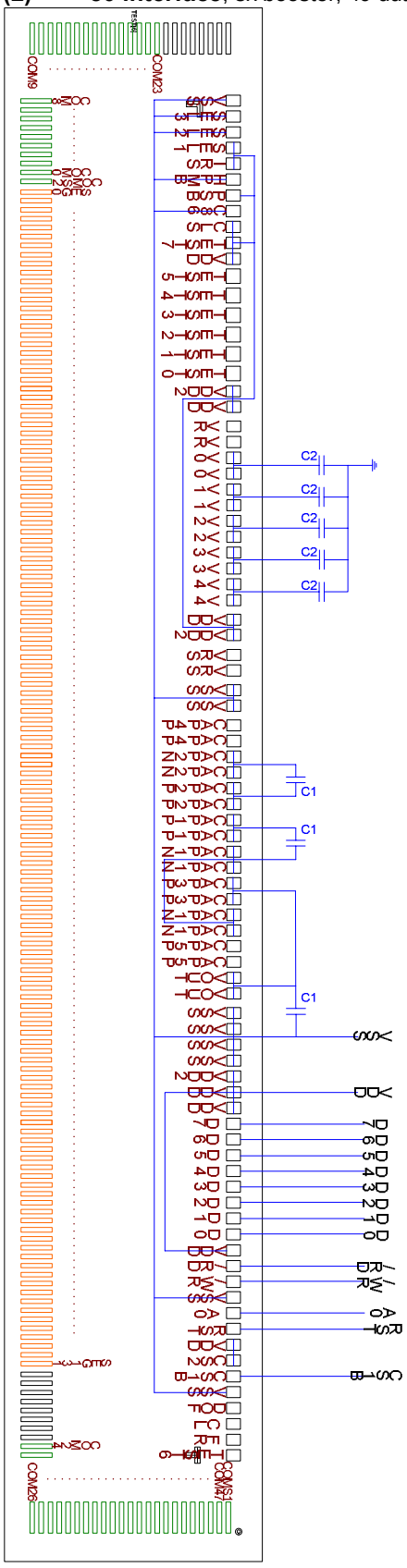
Figure 43-1

Application Notes

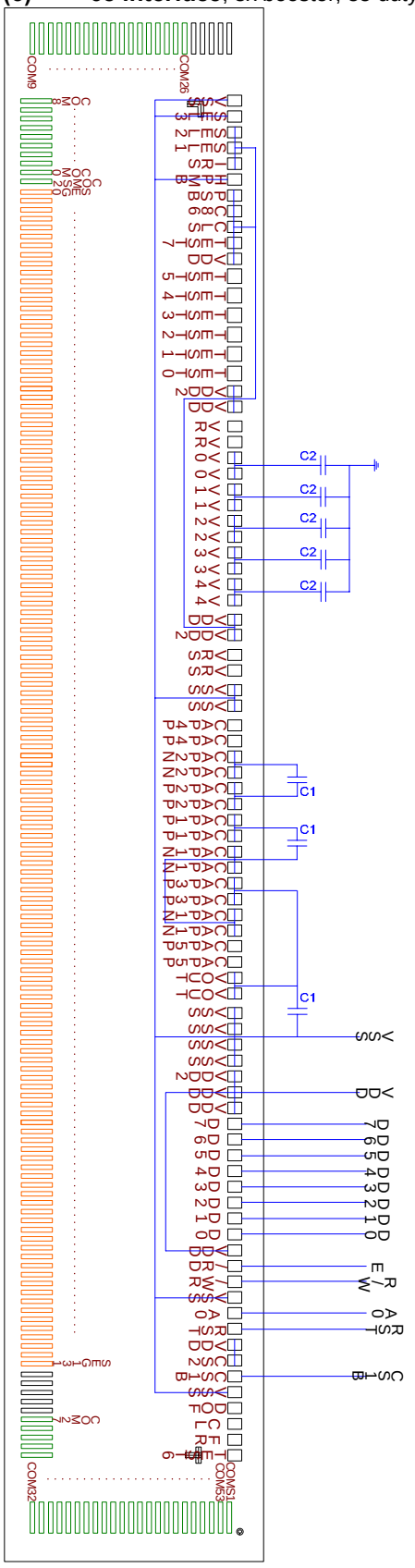
(1) 4-line interface, 4x booster, 65 duty, internal resistor, high power mode, internal oscillator



(2) 80 interface, 3x booster, 49 duty, internal resistor, high power mode, internal oscillator



(3) 68 interface, 3x booster, 55 duty, internal resistor, high power mode, internal oscillator



Recommend LCD Setting

Item	Set value	unit
C1	1 ~ 2.2	uF
C2	0.1~ 1	uF

Recommend Setting:
VDD = VDD2 = 3.0V
Booster = X3
BIAS = 1/6
Vop = 5.5~6.7V
Duty = 1/33

Recommend Setting:
VDD = VDD2 = 3.0V
Booster = X3
BIAS = 1/5
Vop = 5.0~6.1V
Duty = 1/33

Item	Set value	unit
C1	1 ~ 2.2	uF
C2	0.1~ 1	uF

Recommend Setting 1:
VDD = VDD2 = 3.0V
Booster = X3
BIAS = 1/6
Vop = 6.0~7.0V
Duty = 1/49

Recommend Setting 2:
VDD = VDD2 = 3.0V
Booster = X4
BIAS = 1/8
Vop = 7.0~8.5V
Duty = 1/49

Item	Set value	unit
C1	1 ~ 2.2	uF
C2	0.1~ 1	uF

Recommend Setting 1:
VDD = VDD2 = 3.0V
Booster = X3
BIAS = 1/6
Vop = 6.0~7.5V
Duty = 1/55

Recommend Setting 2:
VDD = VDD2 = 3.0V
Booster = X4
BIAS = 1/8
Vop = 7.0~8.5V
Duty = 1/55

Item	Set value	unit
C1	1 ~ 2.2	uF
C2	0.1~ 1	uF

Recommend Setting:
VDD = VDD2 = 3.0V
Booster = X4
BIAS = 1/7
Vop = 7.0~8.5V
Duty = 1/65

Change Notes:

2005/03/24	Ver 0.1	● Preliminary
2005/05/20	Ver 0.2	● Bump Height
2005/08/10	Ver 0.3	● Shipping Forms ● Pad Arrangement, Bump Height, Bump Pitch, Bump Height ● Pad Names- remove ":P", ":g", rename FUSE, VSSF as TEST ● Connections Between LCD Drivers ● Application Notes ● Unused Data Pin In 4-Line SPI Fixed To 'H' ● ITO Resister Limitation
2005/09/29	Ver 0.4	● Modify the Absolute Maximum Ratings. ● Modify the operating range of VDD, VDD2, VOUT and V_0. ● Modify the description of features. ● Modify the Operating Temperature. ● Modify the Ta value of DC Characteristics and Reset Timing. ● Remove redundant features on Page 2.
2005/10/20	Ver 1.0	● Remove Preliminary ● Modify the Pad Arrangement(COG) on Page 2. ● Modify the I/O PIN ITO Resister Limitation on Page 22.
2005/10/21	Ver 1.1	● Modify the Operating Temperature
2005/11/07	Ver 1.2	● Unused Data Pin In 4-Line C86 Fixed To 'H' ● Unused Data Pin In 4-Line /RD Fixed To 'H' ● Unused Data Pin In 4-Line /WR Fixed To 'H'
2005/11/25	Ver 1.3	● Modify the flow chart on Page 46, 47 and 49.
2006/02/13	Ver 1.4	● Modify the description of DC characteristics. ● Modify function description. ● Redraw figures. ● Redraw the PAD DIAGRAM. ● Highlight the HPM (High Power Mode) description. ● Put emphasis on the power OFF procedure (Page 54-55).
2006/03/10	Ver 1.5	● Fix Ver. 1.4: Booster Circuit mistake (Booster X6, Page 32).
2007/04/24	Ver 1.6	● Add V0 capacitor notes. ● Add application notes. ● Modify ITO resistance limitation. ● Modify operation voltage.
2007/05/14	Ver 1.6a	● Add a section for "Recommend LCD Setting". ● Modify the recommend setting of "Recommend LCD Setting".
2007/06/01	Ver 1.7	● Remove slave function. ● Remove static indicator function.