TOSHIBA CMOS Digital Integrated Circuit    Silicon Monolithic

# TC7MPB9326FT, TC7MPB9326FK
# TC7MPB9327FT, TC7MPB9327FK

## Low Voltage / Low Power Dual SPDT Supply Bus Switch

The TC7MPB9326 and TC7MPB9327 are CMOS dual multiplexer/demultiplexer bus switches that can provide an interface between two nodes at different voltage levels. These devices can be connected to two independent power supplies. $V_{CCA}$ supports 1.8 V, 2.5 V and 3.3 V power supplies, whereas $V_{CCB}$ supports 2.5 V, 3.3 V and 5.0 V power supplies.

Bidirectional level-shifting is possible by simply adding external pull-up resistors between the A/Bn data lines and the $V_{CCA}$ / $V_{CCB}$ supplies. There is no restriction on the relative magnitude of the A and Bn voltages; both the 1A/2A and 1B1/1B2 ,2B1/2B2 data lines can be pulled up to the arbitrary power supplies.

The Output Enable pin (OE) can be used to disable the device so that the bus lines are effectively isolated.

This device consists of dual individual two-inputs multiplexer/demultiplexer with a common select input (S) and an output enable (OE:TC7MPB9326, $\overline{OE}$:TC7MPB9327). The 1A/2A inputs are connected to 1B1/1B2 and 2B1/2B2 outputs based on the combination of select input and output enable.

For   TC7MPB9326, it has an active high Output Enable (OE) : When OE is High, the switch is on; when Low, the switch is turned off. For the TC7MPB9327, it has an active low Output Enable ($\overline{OE}$) : When $\overline{OE}$ is Low, the switch is turned on; when $\overline{OE}$ is High, the switch is off.

The TC7MPB9326 and TC7MPB9327 supports power-down protection at the  $\overline{OE}$ , OE input, with  $\overline{OE}$ , OE being 5.5 V tolerant.

The channels consist of n-type MOSFETs.

All the inputs provide protection against electrostatic discharge.

TC7MPB9326FT,TC7MPB9327FT



TSSOP14-P-0044-0.65A

TC7MPB9326FK,TC7MPB9327FK
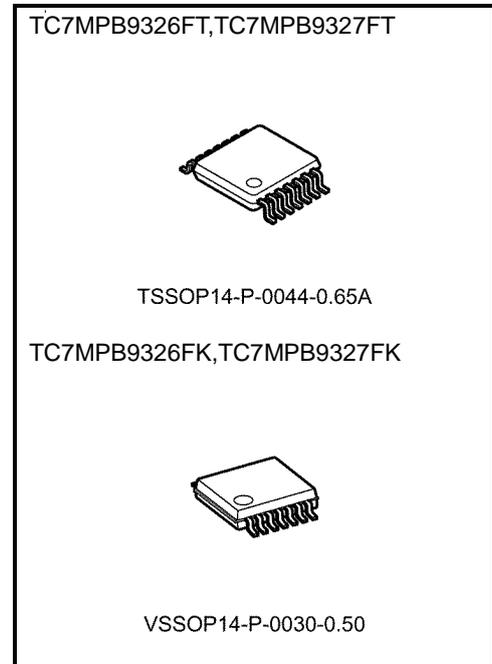


VSSOP14-P-0030-0.50

Weight
TSSOP14-P-0044-0.65A      : 0.06 g (typ.)
VSSOP14-P-0030-0.50       : 0.02 g (typ.)

## Features

- Operating voltage:1.8 V to 2.5 V, 1.8 V to 3.3 V, 1.8 V to 5.0 V, 2.5 V to 3.3 V, 2.5 V to 5.0 V or 3.3 V to 5.0 V bidirectional interface

- Operating voltage: $V_{CCA}$ = 1.65 to 5.0 V, $V_{CCB}$ = 2.3 to 5.5 V

- Low ON-resistance: $R_{ON}$ = 5.0 Ω (typ.)@ $V_{IS}$ = 0 V, $I_{IS}$ = 30 mA, $V_{CCA}$= 3.0 V , $V_{CCB}$ = 4.5 V

- ESD performance: Machine model ≥ ±200 V
                   Human body model ≥ ±2000 V

- 5.5 V tolerance and power-down protection at the Output Enable input.

- Packages: TSSOP14, VSSOP14(US14)

Start of commercial production
2009-09

## Pin Assignment (top view)

TSSOP14, US14

### TC7MPB9326FT/FK

| Pin | Signal | | Pin | Signal |
|---|---|---|---|---|
| 1 | V$_{CCA}$ | | 14 | V$_{CCB}$ |
| 2 | 1A | | 13 | 1B1 |
| 3 | N.C | | 12 | 1B2 |
| 4 | 2A | | 11 | 2B1 |
| 5 | N.C | | 10 | 2B2 |
| 6 | S | | 9 | N.C |
| 7 | GND | | 8 | OE |

### TC7MPB9327FT/FK

| Pin | Signal | | Pin | Signal |
|---|---|---|---|---|
| 1 | V$_{CCA}$ | | 14 | V$_{CCB}$ |
| 2 | 1A | | 13 | 1B1 |
| 3 | N.C | | 12 | 1B2 |
| 4 | 2A | | 11 | 2B1 |
| 5 | N.C | | 10 | 2B2 |
| 6 | S | | 9 | N.C |
| 7 | GND | | 8 | $\overline{OE}$ |
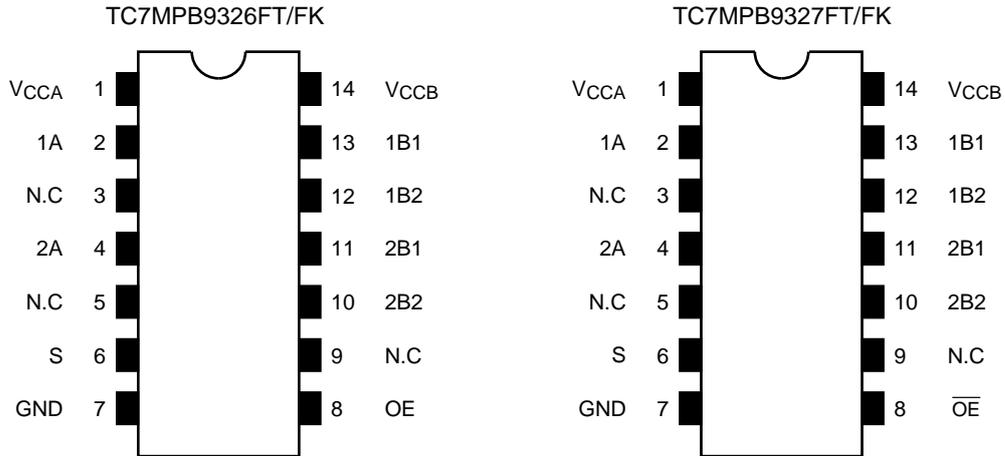
## Truth Table

| Inputs(9326) | | Function | Inputs(9327) | | Function |
|---|---|---|---|---|---|
| OE | S | | $\overline{OE}$ | S | |
| H | L | A = B1 | L | L | A = B1 |
| H | H | A = B2 | L | H | A = B2 |
| L | X | Disconnect | H | X | Disconnect |

X : Don't care

## Circuit Schematic



TC7MPB9326



TC7MPB9327
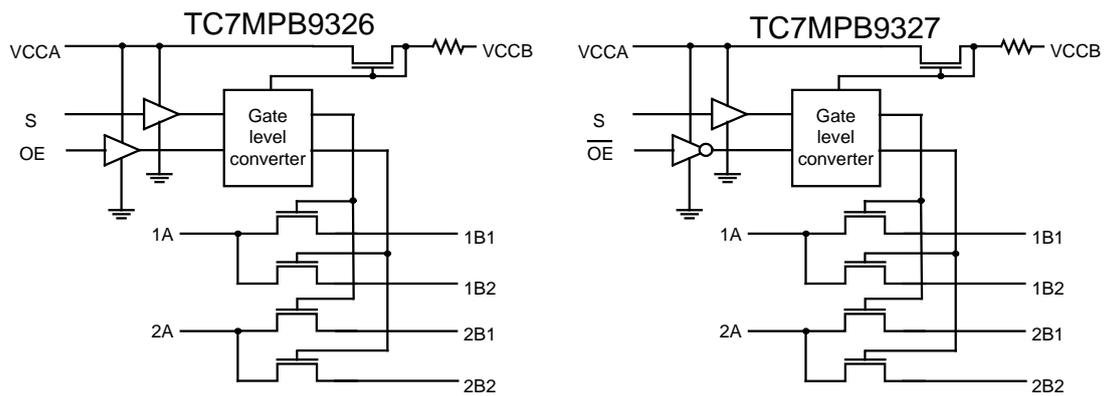
## Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CCA}$ | -0.5 to 7.0 | V |
| | $V_{CCB}$ | -0.5 to 7.0 | |
| Control input voltage | $V_{IN}$ | -0.5 to 7.0 | V |
| Switch input/output voltage | $V_S$ | -0.5 to 7.0 | V |
| Clamp diode current | $I_{IK}$ | -50 | mA |
| Switch input/output current | $I_S$ | 64 | mA |
| DC $V_{CC}$/ground current per supply pin | $I_{CCA}$ | ±25 | mA |
| | $I_{CCB}$ | ±25 | |
| Power dissipation | $P_D$ | 180 | mW |
| Storage temperature | $T_{stg}$ | -65 to 150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage (Note 1) | $V_{CCA}$ | 1.65 to 5.0 | V |
| | $V_{CCB}$ | 2.3 to 5.5 | |
| Control input voltage | $V_{IN}$ | 0 to 5.5 | V |
| Switch input/output voltage | $V_S$ | 0 to 5.5 | V |
| Operating temperature | $T_{opr}$ | -40 to 85 | °C |
| Control input rise and fall times | dt/dv | 0 to 10 | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either $V_{CCA}$ or GND.

Note 1: The $V_{CCA}$ voltage must be lower than the $V_{CCB}$ voltage.

## Application Circuit
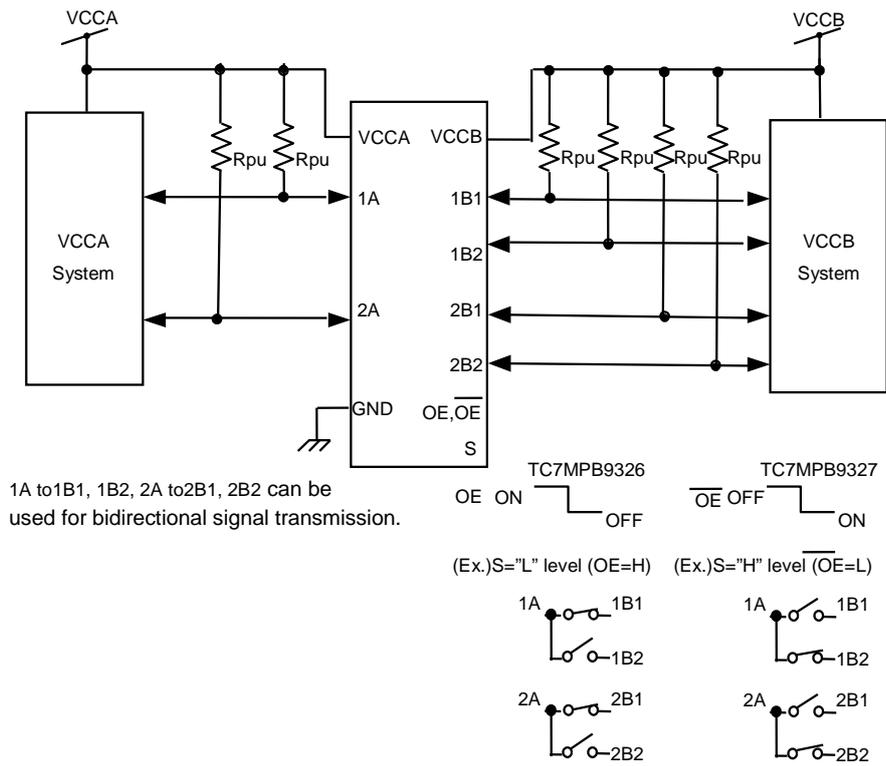


**Figure 1    Application Circuit Diagram**

The $V_{CCA}$ voltage must be lower than the $V_{CCB}$ voltage.

Level-shifting functionality is enabled by adding pull-up resistors from A to $V_{CCA}$ or $V_{CCB}$ and from Bn to $V_{CCB}$ or $V_{CCA}$, respectively.

## Electrical Characteristics

### DC Characteristics (Ta = -40 to 85°C)

| Characteristics | | Symbol | Test Condition | $V_{CCA}$ (V) | $V_{CCB}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| input voltage (OE/$\overline{OE}$, S) | High-level | $V_{IH}$ | — | $1.65 \leq V_{CCA} < 2.3$ | $V_{CCA}$ to 5.5 | $0.8\times V_{CCA}$ | — | V |
| | | | | $2.3 \leq V_{CCA} < 5.0$ | $V_{CCA}$ to 5.5 | $0.7\times V_{CCA}$ | — | |
| | Low-level | $V_{IL}$ | — | $1.65 \leq V_{CCA} < 2.3$ | $V_{CCA}$ to 5.5 | — | $0.2\times V_{CCA}$ | |
| | | | | $2.3 \leq V_{CCA} < 5.0$ | $V_{CCA}$ to 5.5 | — | $0.3\times V_{CCA}$ | |
| ON-resistance (Note 1) | | $R_{ON}$ | $V_{IS}$ = 0 V, $I_{IS}$ = 30 mA (Figure 2) | 1.65 | 2.3 | — | 16.0 | Ω |
| | | | | 2.3 | 3.0 | — | 11.0 | |
| | | | | 3.0 | 4.5 | — | 8.0 | |
| Power off leakage current | | $I_{OFF}$ | 1A, 2A, 1Bn, 2Bn = 0 to 5.5 V (per circuit) | 0 | 0 | — | ±1.0 | μA |
| Switch-off leakage current | | $I_{SZ}$ | 1A, 2A, 1Bn, 2Bn = 0 to 5.5 V $\overline{OE}$ = $V_{CCA}$, OE = GND | 1.65 to 5.0 | $V_{CCA}$ to 5.5 | — | ±1.0 | μA |
| Control input current | | $I_{IN}$ | OE, $\overline{OE}$, S = 0 to 5.5 V | 1.65 to 5.0 | $V_{CCA}$ to 5.5 | — | ±1.0 | μA |
| leakage current from $V_{CCB}$ to $V_{CCA}$ | | $I_{CCBA}$ | OE, $\overline{OE}$ = GND or $V_{CCA}$ $V_{CCB} \rightarrow V_{CCA}$ | 3.3 | 5.0 | — | 20.0 | μA |
| Quiescent supply current | | $I_{CCA1}$ | OE, $\overline{OE}$ = $V_{CCA}$ or GND, $I_S$ = 0 A | 1.65 to 5.0 | $V_{CCA}$ | — | 4.0 | μA |
| | | $I_{CCB1}$ | OE, $\overline{OE}$ = $V_{CCA}$ or GND, $I_S$ = 0 A | 1.65 to 5.0 | $V_{CCA}$ | — | 4.0 | |
| | | $I_{CCA2}$ | $V_{CCA} \leq$ OE, $\overline{OE} \leq$ 5.5 V, $I_S$ = 0 A | 1.65 to 5.0 | $V_{CCA}$ | — | ±4.0 | |
| | | $I_{CCB2}$ | $V_{CCA} \leq$ OE, $\overline{OE} \leq$ 5.5 V, $I_S$ = 0 A | 1.65 to 5.0 | $V_{CCA}$ | — | ±4.0 | |

Note 1:  ON-resistance is measured by measuring the voltage drop across the switch at the indicated current.

### Level Shift Characteristics (Ta = -40 to 85°C)

| Characteristics | Symbol | Test Condition | $V_{CCA}$ (V) | $V_{CCB}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input/Output Characteristics (Up Translation) (Note 1) | $V_{OHU}$ | 1A, 2A = $V_{IN}$ SW = ON (Figure 7) | 1.65 | 3.0 to 5.5 | 1.4 | — | V |
| | | | 2.3 | 4.5 to 5.5 | 2.05 | — | |
| | | | 3.0 | 4.5 to 5.5 | 2.7 | — | |
| Input/Output Characteristics (Down Translation) (Note 2) | $V_{OHD}$ | 1A, 2A = $V_{IN}$ SW = ON (Figure 9) | 1.65 | 3.3 to 5.5 | 1.3 | 1.65 | |
| | | | 2.3 | 4.5 to 5.5 | 1.95 | 2.3 | |
| | | | 3.0 | 4.5 to 5.5 | 2.6 | 3.0 | |

Note 1:  The Input/Output Characteristics for up translation indicate the input voltages required to provide $V_{CCA}$ + 0.5 V on the outputs when measured using the test circuitry shown in Figure 7.

Note 2:  The Input/Output Characteristics for down translation indicate the voltages that cause the output voltages to saturate when measured using the test circuitry shown in Figure 9.

## AC Characteristics (Ta = -40 to 85°C, Input: $t_r = t_f = 2.0$ ns, $f = 10$ kHz)

### V$_{CCA}$= 3.3 ± 0.3 V, V$_{CCB}$= 5.0 ± 0.5 V

| Characteristics | Symbol | Test Condition | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time (Bus to Bus) | $t_{pLH}$ | Figure 3, Figure 5 | (Note 1) | — | 0.3 | ns |
| Propagation delay time (Bus to Bus) | $t_{pHL}$ | Figure 3, Figure 5 | (Note 1) | — | 1.2 | |
| Output enable time | $t_{pZL}$ | Figure 4, Figure 6 | | — | 9.0 | |
| Output disable time | $t_{pLZ}$ | Figure 4, Figure 6 | | — | 11.0 | |

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

### V$_{CCA}$= 2.5 ± 0.2 V, V$_{CCB}$= 5.0 ± 0.5 V

| Characteristics | Symbol | Test Condition | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time (Bus to Bus) | $t_{pLH}$ | Figure 3, Figure 5 | (Note 1) | — | 0.35 | ns |
| Propagation delay time (Bus to Bus) | $t_{pHL}$ | Figure 3, Figure 5 | (Note 1) | — | 1.8 | |
| Output enable time | $t_{pZL}$ | Figure 4, Figure 6 | | — | 13.0 | |
| Output disable time | $t_{pLZ}$ | Figure 4, Figure 6 | | — | 15.0 | |

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

### V$_{CCA}$ = 2.5 ± 0.2 V, V$_{CCB}$= 3.3 ± 0.3 V

| Characteristics | Symbol | Test Condition | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time (Bus to Bus) | $t_{pLH}$ | Figure 3, Figure 5 | (Note 1) | — | 0.45 | ns |
| Propagation delay time (Bus to Bus) | $t_{pHL}$ | Figure 3, Figure 5 | (Note 1) | — | 2.2 | |
| Output enable time | $t_{pZL}$ | Figure 4, Figure 6 | | — | 17.0 | |
| Output disable time | $t_{pLZ}$ | Figure 4, Figure 6 | | — | 19.0 | |

Note 1: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 30 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

## Capacitive Characteristics (Ta = 25°C)

| Characteristics | | Symbol | Test Condition | V$_{CCA}$ (V) | V$_{CCB}$ (V) | Typ. | Unit |
|---|---|---|---|---|---|---|---|
| Control input capacitance | (OE/$\overline{OE}$ , S) | $C_{IN}$ | | 3.3 | 3.3 | 3 | pF |
| Switch input/output capacitance | (1A, 2A) | $C_{I/O}$ | SW = ON (A,B) | 3.3 | 3.3 | 14 | |
| | (1A, 2A) | | SW = OFF (A) | 3.3 | 3.3 | 7 | |
| | (1B1, 1B2, 2B1, 2B2) | | SW = OFF (B) | 3.3 | 3.3 | 7 | |

**DC Test Circuit**
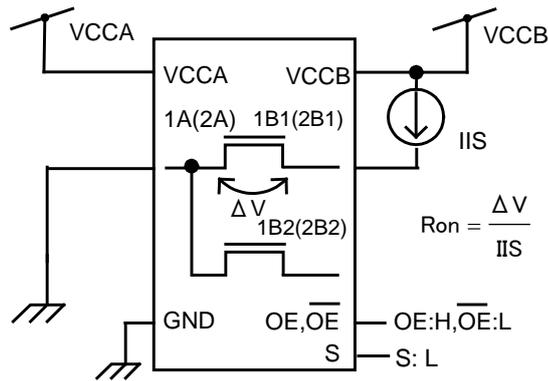


**Figure 2   ON-resistance Test Circuits**

**AC Test Circuits**

· **tpLH, HL**
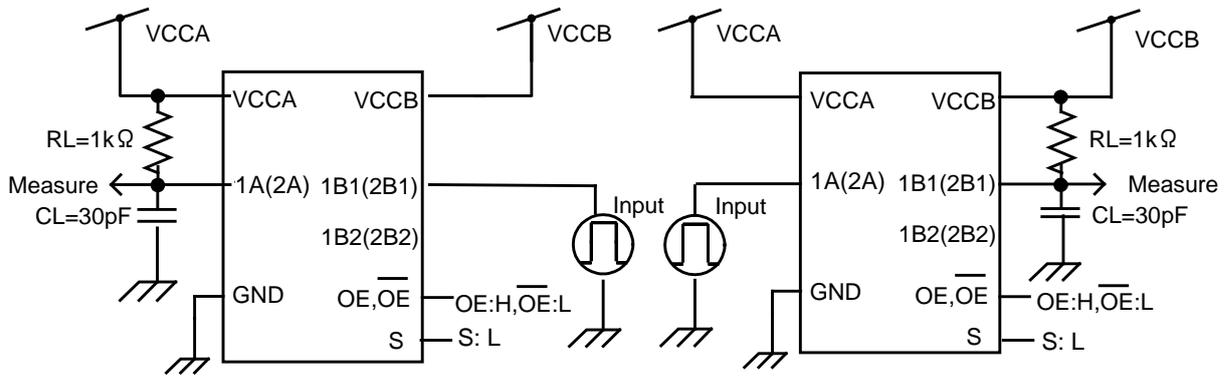


**Figure 3   t$_p$LH, t$_p$HL Test Circuits**

· **tpLZ, ZL**
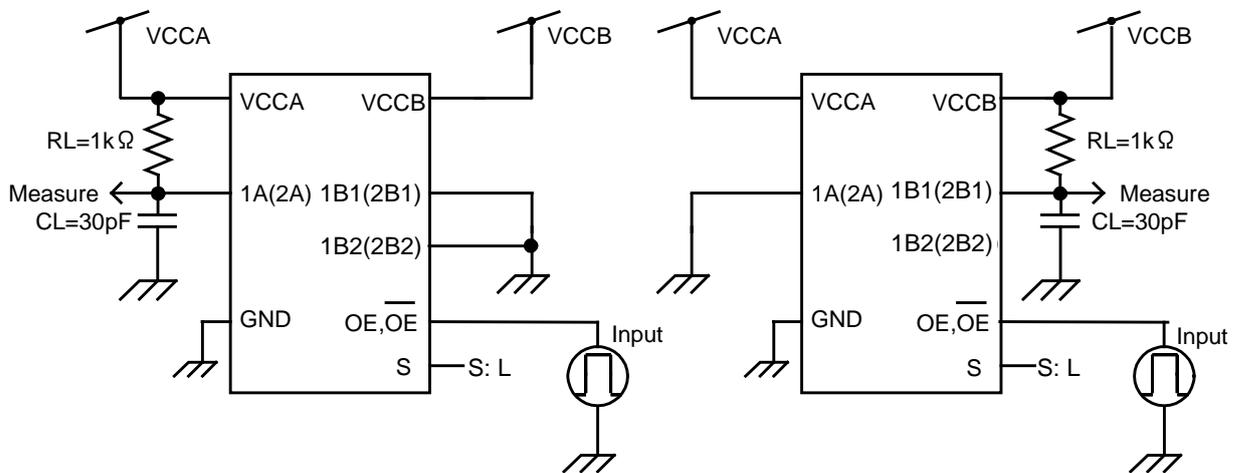


**Figure 4   t$_p$LZ, t$_p$ZL Test Circuits**

## AC Waveform

$t_r$ 2.0 ns  $t_f$ 2.0 ns

Input
(1A, 2A)

VCCA
90%
50%
10%
GND

Output
(1Bn, 2Bn)

$V_{OH}$
1/2 VCCA
$V_{OL}$

$t_{pLH}$  $t_{pHL}$

**Figure 5   $t_{pLH}$, $t_{pHL}$**

$t_r$ 2.0 ns  $t_f$ 2.0 ns

Output Enable
Control OE, $\overline{OE}$

VCCA
90%
50%
10%
GND

$t_{pLZ}$  $t_{pZL}$

Output (1A,2A or
1Bn,2Bn)
Low to off to Low

VOH
10%
50%

Outputs
enabled
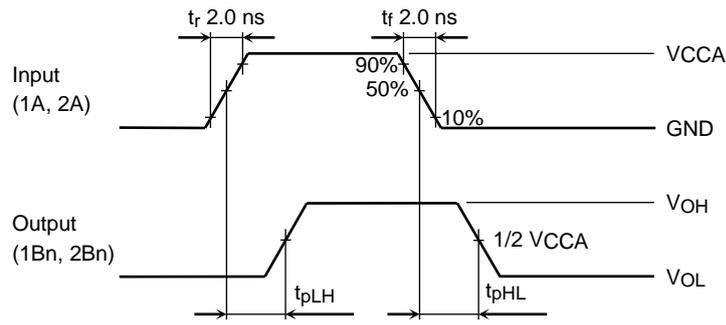
Outputs
disabled
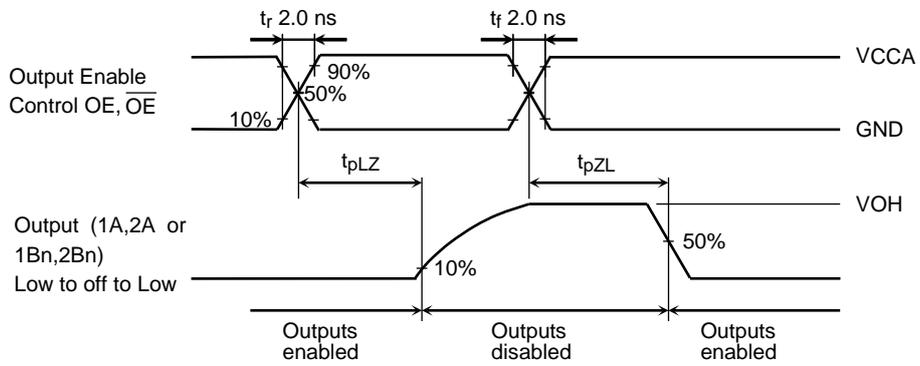
Outputs
enabled

**Figure 6   $t_{pLZ}$, $t_{pZL}$**

**Level Shift Function (Used Pull-up Resistance)**
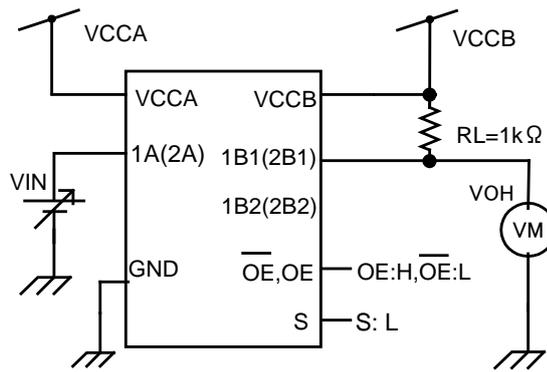


**Figure 7    Test Circuit**
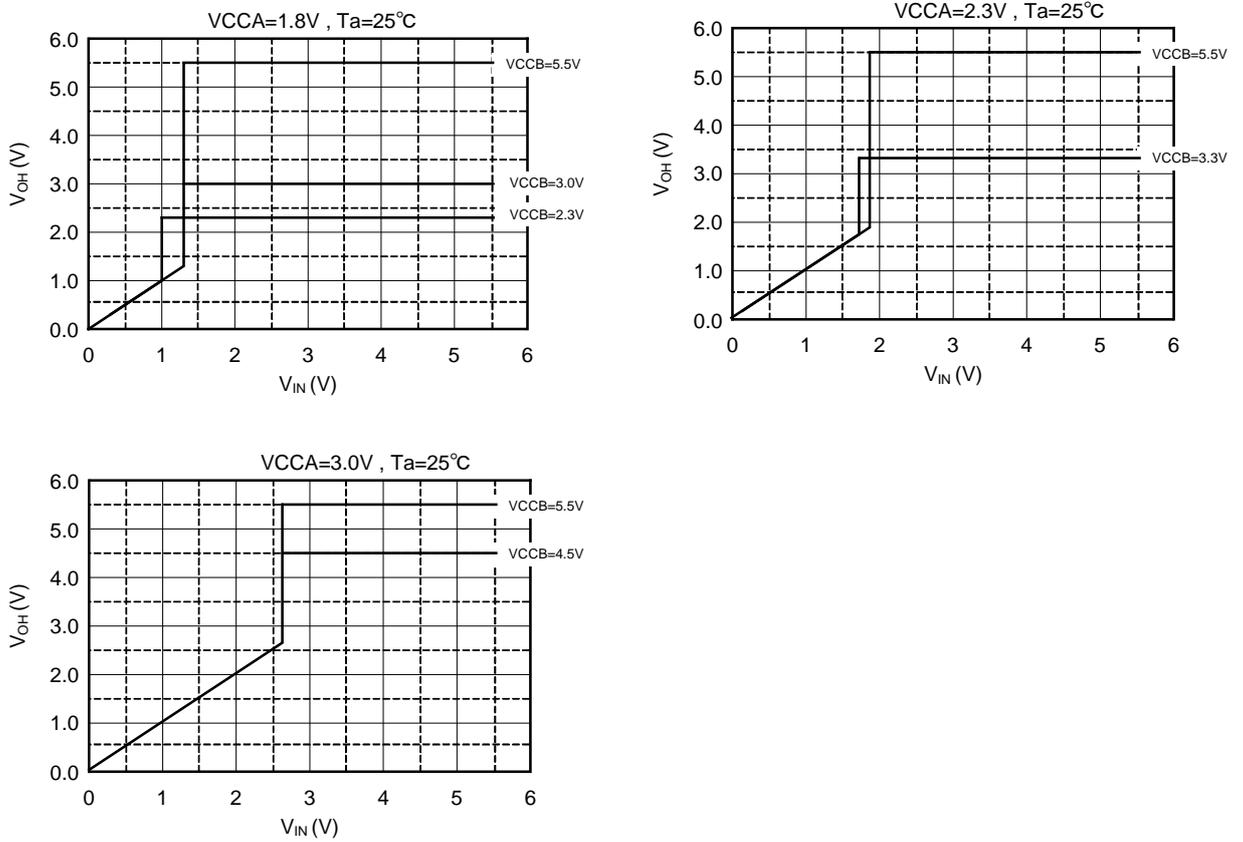


**Figure 8    Input/Output Characteristics (Typ.)**

**Level Shift Function (Unused Pull-up Resistance)**
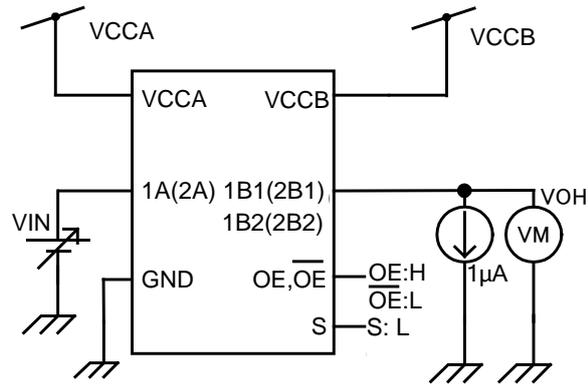


**Figure 9    Test Circuit**
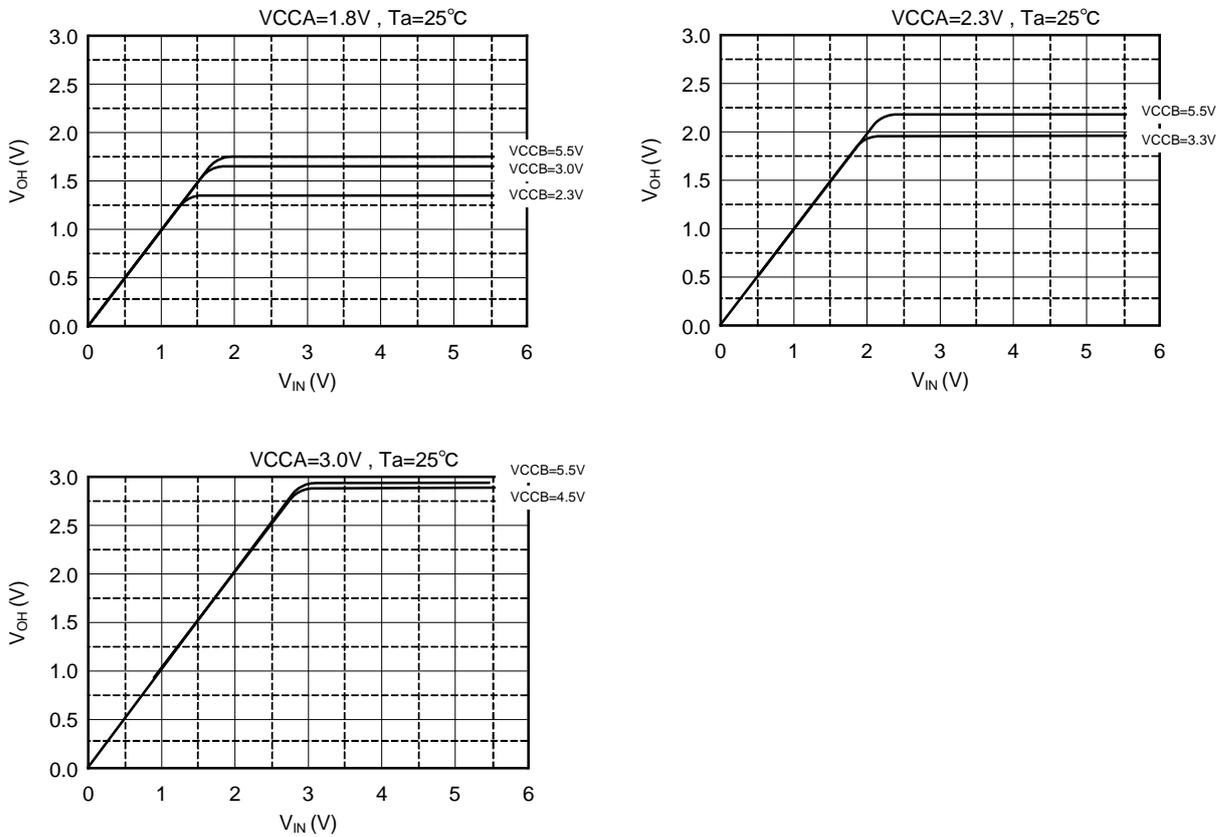


**Figure 10    Input/Output Characteristics (Typ.)**

## Package Dimensions

TSSOP14-P-0044-0.65A                                                    Unit: mm

14        8

4.4±0.1

6.4±0.2

1        7

0.55TYP        0.65        0.22 +0.09 −0.06        ⊕ 0.13 Ⓜ

5.4 MAX

5.0±0.1

1.2 MAX

Ⓢ        ⟋ 0.1 Ⓢ

0.1±0.05        1.0±0.05

0.15 +0.03 −0.01        0~10°        (0.5)        0.25

0.45~0.75
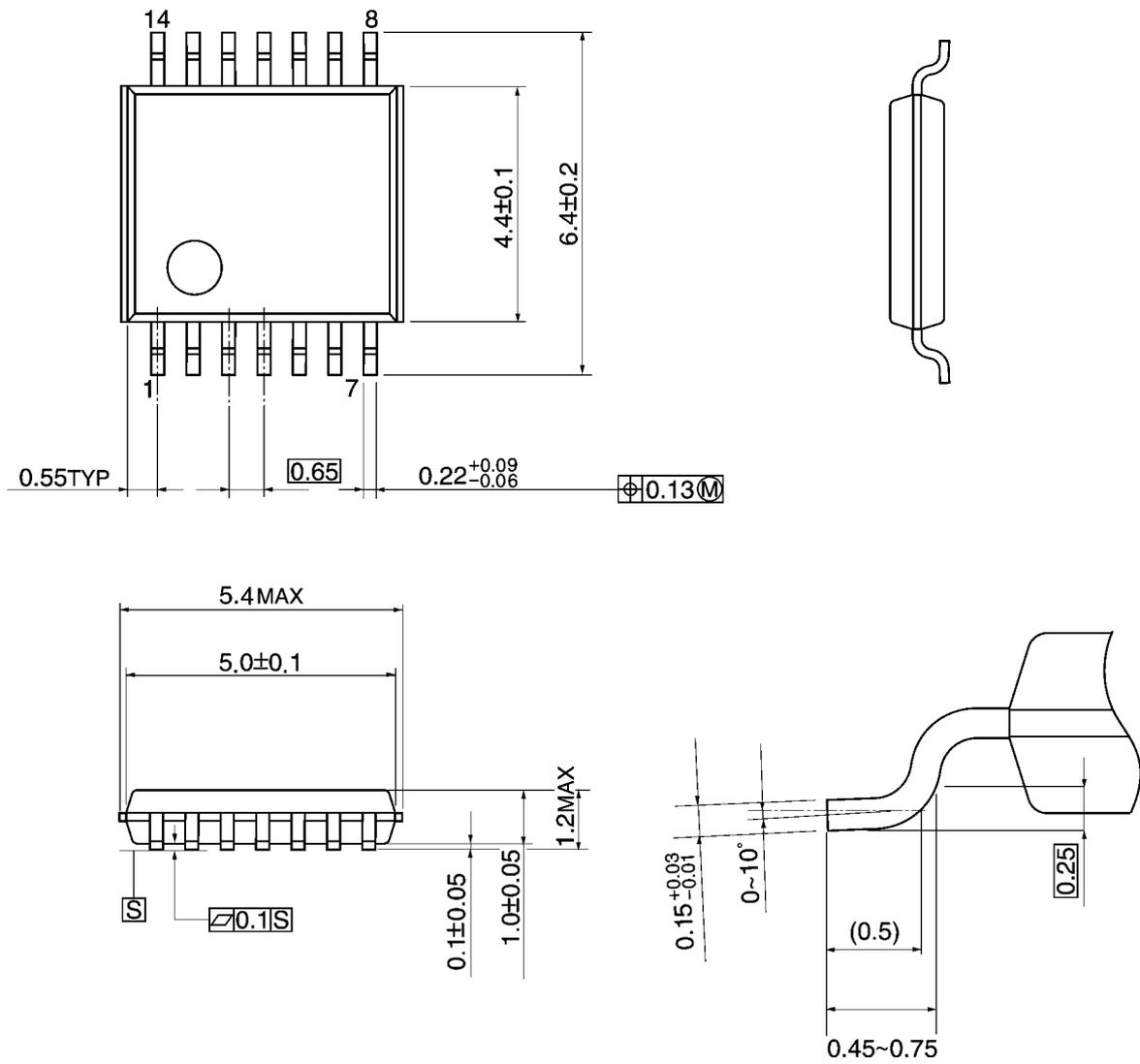
Weight: 0.06 g (typ.)

## Package Dimensions

VSSOP14-P-0030-0.50                                                    Unit: mm



Weight: 0.02 g (typ.)

2017-02-23