Single Output LNB Supply Voltage Regulator for Satellite Set-Top Box Applications

ISL9491, ISL9491A

These devices are designed for supplying power and control signals from advanced satellite set-top box (STB) modules to the low noise blocks (LNBs) of single antenna ports. Each device consists of a current-mode boost converter and a low-noise linear regulator along with the circuitry required for tone injection and pin controllable interface. The device makes the total LNB supply design simple, efficient and compact with low external component count.

The current-mode boost converters provide the linear regulator with input voltage that is set to the voltage at the VOUT pin plus a minimal drop to insure minimum power dissipation across the internal LDO. This maintains constant voltage drop across the linear pass element while permitting adequate voltage range for tone injection.

The final regulated output voltage is available at the cathode of the back diode to support the operation of an antenna port for a single tuner. The outputs can be set to various voltage level for the desired polarization reception by means of the logic presented to the VSET0 and VSET1 pins. An EN pin is to be driven high to enable the outputs for the PWM and linear combination; setting EN low disables the output, forcing a shutdown mode.

The external modulation input (EXTM) can accept a tone modulated DiSEqC command and transfer it symmetrically to the output to meet DiSEqC 1.x protocol. An external DiSEqC tank circuit can also be implemented to support DiSEqC 2.x.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL9491ERZ*	94 91ERZ	-20 to +85	16 Ld QFN	L16.4x4
ISL9491AERZ* **(No longer available or supported)**	94 91AERZ	-20 to +85	16 Ld QFN	L16.4x4

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

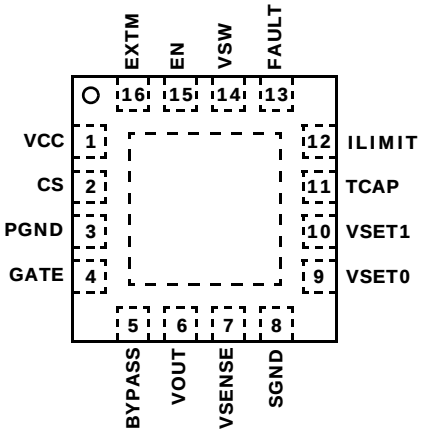
- Single Chip Power Solution
  - Operation for 1-Tuner/1-Dish Applications
- Switch-Mode Power Converter for Lowest Dissipation
  - Boost PWMs with >92% Efficiency
  - Pin Controllable Enable and Output
- 2.5V/3.3V/5V Logic Compatible
- FAULT Signal
- DIRECTV SWM Compliant
- VSET Pin to Toggle between Vertical and Horizontal Polarizations
- External Tone Input
- Internal Overcurrent and Over-Temperature Protection
- Pb-Free (ROHs Compliant)

Applications

- LNB Power Supply and Control for Satellite Set-Top Box

Pin Configuration

ISL9491, ISL9491A
(16 LD QFN)
TOP VIEW

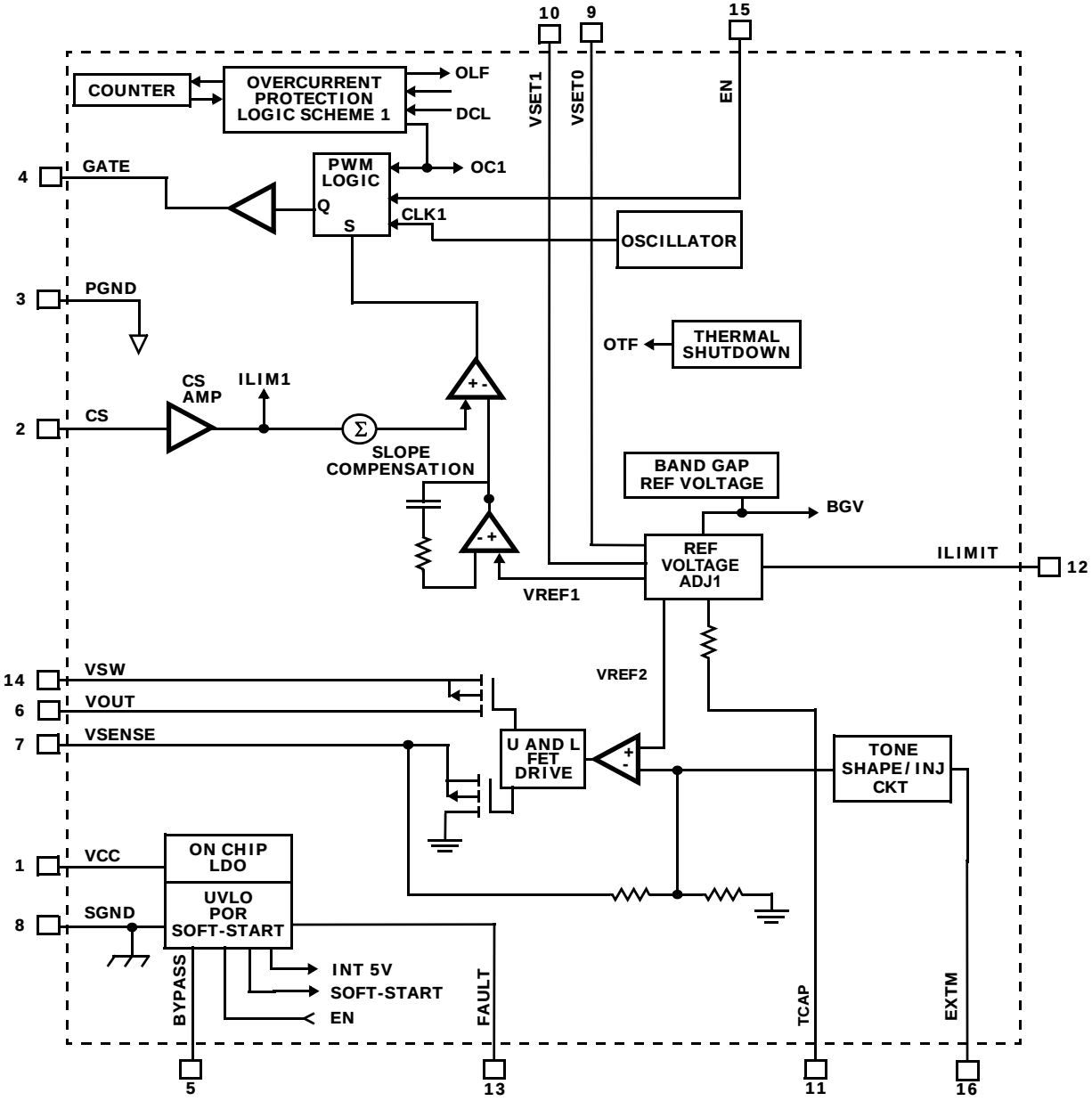


ISL9491, ISL9491A

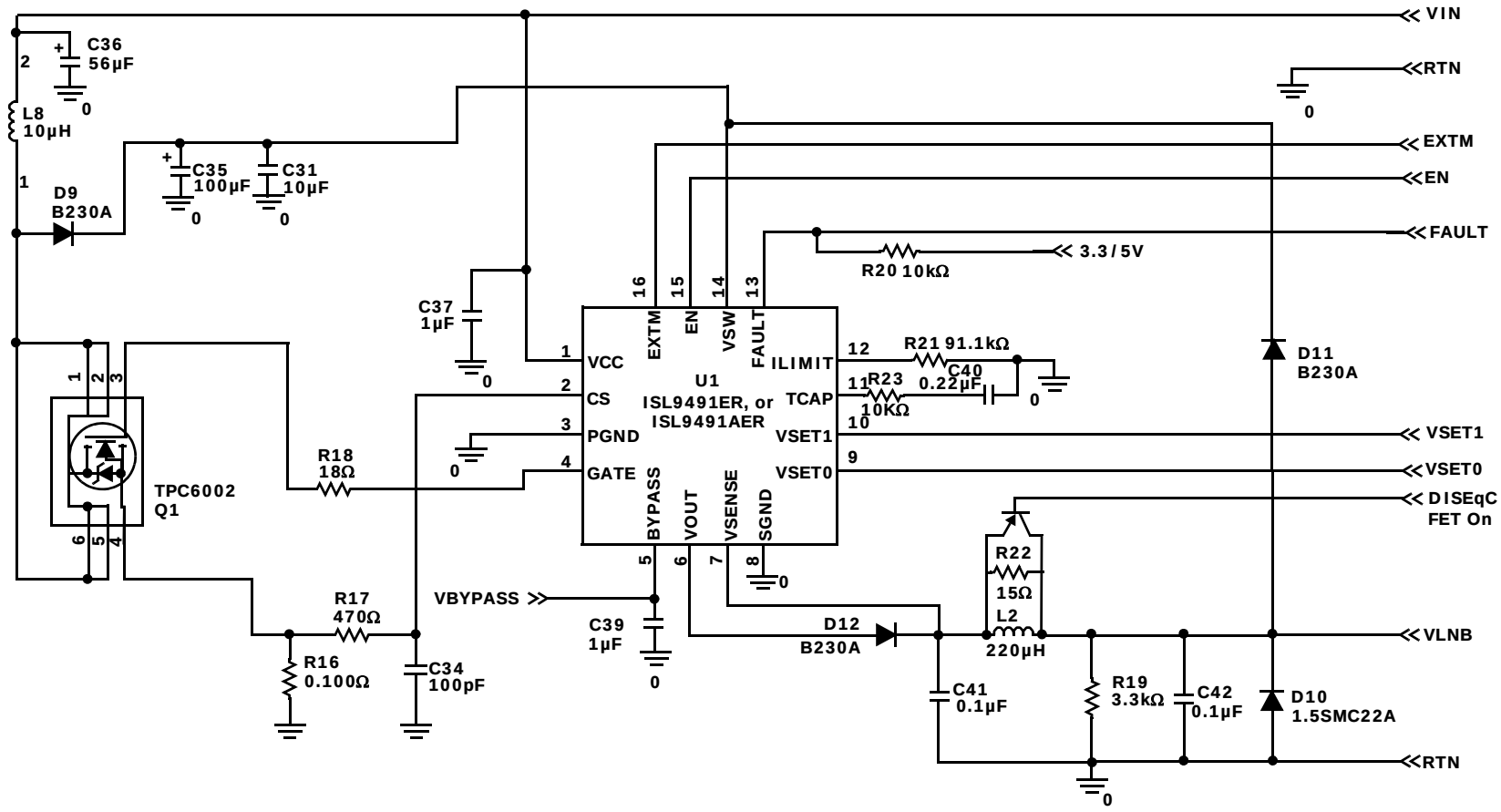
Functional Pin Description

SYMBOL	FUNCTION
VSW	Input of the linear post-regulator.
PGND	Dedicated ground for the output gate driver of respective PWM.
CS	Current sense input; connect the sense resistor R_{SC} at this pin for desired peak overcurrent value for the boost FET.
SGND	Small signal ground for the IC.
TCAP	Capacitor for setting rise and fall time of the output voltage. Typical value is 0.1µF.
BYPASS	Connect a bypass capacitor of 1µF for the internal 5V.
VCC	Main power supply to the chip.
GATE	This pin connects to the Gate of the Boost FET.
VOUT	Output voltage for the LNB meant to be connected to the anode of a back diode in series with the LNB output.
VSENSE	This pin provides for a sensing and pull-down function for the VLNB and is meant to be connected to the cathode of the back diode.
EXTM	This is an input for externally modulated DiSEqC tone signal, which is transferred symmetrically onto VLNB.
VSET0, VSET1	Output voltage selection pins.
EN	When this pin is low, the output is disabled in a low power standby state. Setting EN = 1 enables the output voltage.
FAULT	This an open drain output to be pulled up to the logic high through a resistor. A low indicates that the output voltage is out of regulation.
ILIMIT	The ILIMIT is used to set the value of the output current limit from the linear. A resistor from ILIMIT to GND programs this limit.

Block Diagram



Typical Application Schematic QFN



NOTES:

1. The output voltage level for the desired polarization reception can be selected by means of the logic presented to VSET0 and VSET1 pins.

Absolute Maximum Ratings

VCC (Input Voltage) . . . . . 8.0V to 18.0V
VOUT, VSW . . . . . -0.3V to 24V
BYPASS . . . . . -0.3V to 5.5V
EN, VSET0/1, EXTM (Logic Control Pins) . . . . . -0.3V to 5.5V
All Pins Referenced to Ground

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 2, 3)	47	9.5

Maximum Junction Temperature (Note 4) . . . . . +150°C
Maximum Storage Temperature Range . . . -40°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature . . . . . -20°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
4. The device junction temperature should be kept below +150°C. Thermal shut-down circuitry turns off the device if junction temperature exceeds +130°C typical.

Electrical Specifications

V_{CC} = 12V, T_A = -20°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range		ISL9491	8	12	14	V
		ISL9491A	8	10	11	V
Supply Current (Ivcc current)	I_{IN}	EN = 1, Boost disconnected, and ext. 14.5V supply on VSW when V_{OUT} = 13.3V, No Load	-	4	8	mA
UNDERVOLTAGE LOCKOUT						
Stop Threshold		Input voltage falling from above 8V	-	4.4	-	V
Start Threshold		Input voltage rising from 0V	-	4.9	-	V
Output Voltage, ISL9491	V_O	EN = 1, VSET1 = 0, VSET0 = 0	12.8	13.3	13.6	V
		EN = 1, VSET1 = 0, VSET0 = 1	17.7	18.3	18.7	V
		EN = 1, VSET1 = 1, VSET0 = 0	13.8	14.3	14.6	V
		EN = 1, VSET1 = 1, VSET0 = 1	19.4	20.0	20.4	V
Output Voltage, ISL9491A	V_O	EN = 1, VSET1 = 0, VSET0 = 0	10.5	11.0	11.3	V
		EN = 1, VSET1 = 0, VSET0 = 1	14.5	15.0	15.3	V
		EN = 1, VSET1 = 1, VSET0 = 0	11.5	12.0	12.3	V
		EN = 1, VSET1 = 1, VSET0 = 1	15.5	16.0	16.3	V
Line Regulation	DV_{O1}, DV_{O2}	V_{IN} = 8V to 14V; V_O = 13.30V	-	4	40	mV
		V_{IN} = 8V to 14V; V_O = 18.30V	-	4	60	mV
Load Regulation	DV_{O1}, DV_{O2}	I_O = 0mA to 350mA, V_{OUT} = 13.3V	-	125	180	mV
		I_O = 0mA to 500mA, V_{OUT} = 13.3V (Note 4)	-	190	260	mV
Output Overcurrent Threshold	I_{OCT}	R at I_{LIMIT} = 148k (Note 8)	270	350	435	mA
Internal Regulator Overcurrent Clamp	I_{OCLMP}	Output Shorted to GND, R_{ILIM} = 0			860	mA

Electrical Specifications V_{CC} = 12V, T_A = -20°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

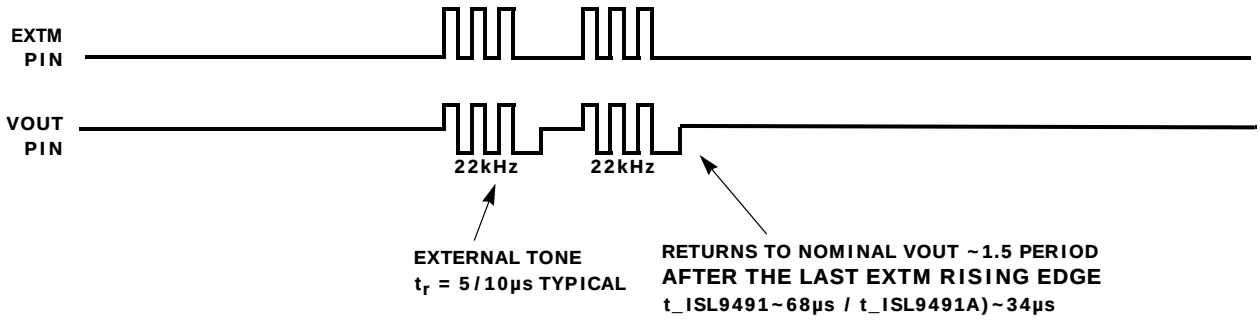
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Dynamic Overload Protection Off-Time	t_{OFF}	Output Shorted to GND (Note 6)	-	900	-	ms
Dynamic Overload Protection On-Time	t_{ON}		-	50	-	ms
TCAP Charging Current	$TCAP_C$	TCAP Pin = 0V	-	22	-	µA
TCAP Discharging Current	$TCAP_D$	TCAP Pin = 2V	-	21	-	µA
LINEAR REGULATOR						
Drop-out Voltage		I_{OUT} = 500mA, with a Schottky b/w Vsw and V_{OUT} (Note 4)	-	1.2	1.4	V
Output Backward Leakage Current	I_{BKLK}	EN = 0; V_{OBK} = 24V (Note 9)	-	2.0	3.0	mA
Output Undervoltage (After Initial Power-up)		$\overline{FAULT}$ asserted for typical V_{OUT} = 13.3V	-12	-	-1	%
Output Overvoltage (After Initial Power-up)		$\overline{FAULT}$ asserted for typical V_{OUT} = 13.3V	+1	-	+12	%
EN, VSET, EXTM INPUT PINS (Note 5)						
Asserted LOW			-	-	0.8	V
Asserted HIGH			2.5	-	-	V
Input Current			-	25	-	µA
Tone Input Frequency	ISL9491	EXTM input		22		kHz
	ISL9491A	EXTM input		44		kHz
V_{OUT} Tone Amplitude	ISL9491	EXTM input = 22kHz square wave Vmax = 2.5V, Vmin = 0V, Duty = 50%,	400	650	900	mV
	ISL9491A	EXTM input = 44kHz square wave Vmax = 2.5V, Vmin = 0V, Duty = 50%	400	650	900	mV
V_{OUT} Tone Rise (Note 10)	ISL9491	EXTM input = 22kHz square wave VHmax = 2.5V, VLmin = 0V, R_L = 1k	5	10	15	µs
	ISL9491A	EXTM input = 44kHz square wave VHmax = 2.5V, VLmin = 0V, R_L = 1k	4	6	8	µs
V_{OUT} Tone Fall (Note 10)	ISL9491	EXTM input = 22kHz square wave VHmax = 2.5V, VLmin = 0V, Duty = 50%, R_L = 1k	5	10	15	µs
	ISL9491A	EXTM input = 44kHz square wave VHmax = 2.5V, VLmin = 0V, Duty = 50%, R_L = 1k	4	6	8	µs
CURRENT SENSE (CS PIN)						
Overcurrent Threshold	V_{CS}		380	445	510	mV
BYPASS						
Voltage at BYPASS pin	V_{BYPASS}	(Note 7)	-	5	-	V
PWM						
Maximum Duty Cycle			90	93	-	%
Minimum Pulse Width			-	20	-	ns

Electrical Specifications V_{CC} = 12V, T_A = -20°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
Oscillator Frequency	f_{sw}	Boost switching frequency	380	440	480	kHz
Thermal Shutdown						
Temperature Shutdown Threshold		(Note 4)	-	130	-	°C
Temperature Shutdown Hysteresis		(Note 4)	-	20	-	°C

5. VSET, EXTM, EN pins have 200kΩ internal pull-down resistors.
6. In the Dynamic current limit mode, the output is ON for 50ms and OFF for 900ms but it remains continuously ON when RILIM=0.
7. This pin is to connect a bypass capacitor in order to decouple the internal LDO and is not designed to source external circuits.
8. The value of the R_{LIMIT} resistor will determine the overcurrent threshold at which the 50ms timer is activated.
9. This defines the back voltage applicable to the VSENSE pin. The VOUT pin will not support back bias and hence will need the use of a back diode for protection.

Tone Waveform



NOTES:

10. The tone rise and fall times are not shown due to resolution of graphics. It is 5/10µs typical.
11. The EXTM pins have input thresholds of Vil(max) = 0.8V and Vih(min) = 2.5V

FIGURE 1. TONE WAVEFORM

Typical Performance Curves

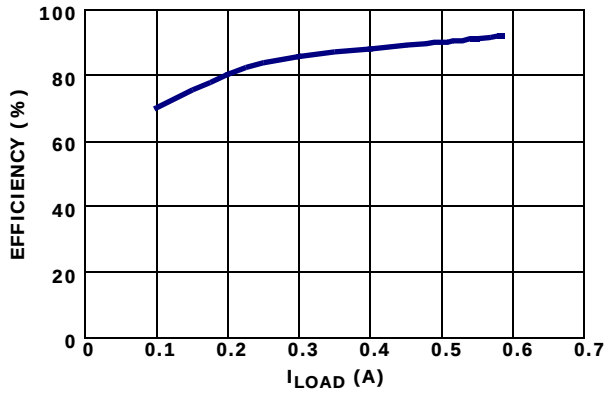


FIGURE 2. BOOST EFFICIENCY FOR 12V_{IN} TO 14.3V_{OUT}

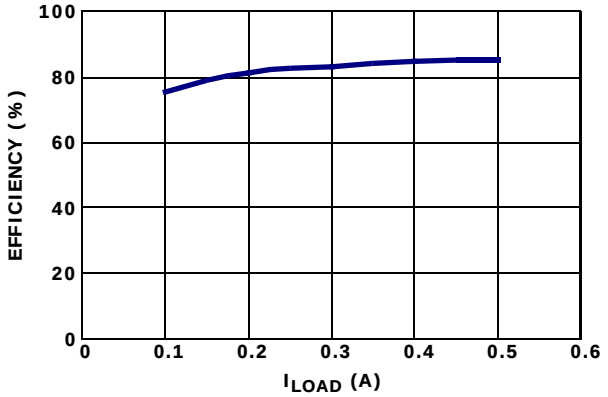


FIGURE 3. SYSTEM EFFICIENCY (BOOST + LDO) FOR 12V_{IN} TO 13.3V_{OUT}

Typical Performance Curves (Continued)

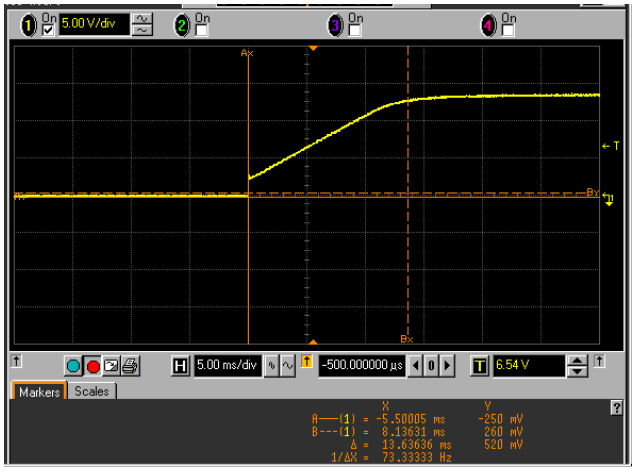


FIGURE 4. VLNB RISE TIME WITH TCAP = 0.22µF is 13ms

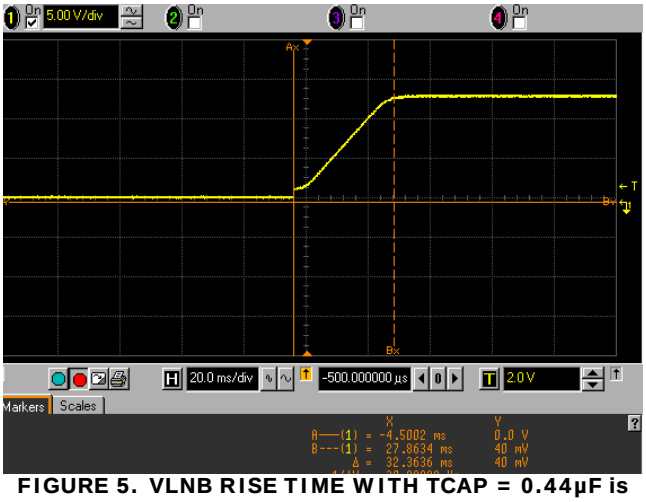


FIGURE 5. VLNB RISE TIME WITH TCAP = 0.44µF is 32ms

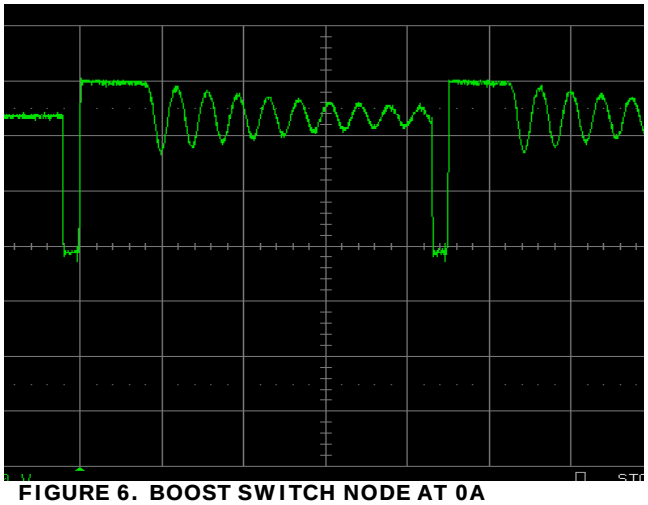


FIGURE 6. BOOST SWITCH NODE AT 0A (DISCONTINUOUS)

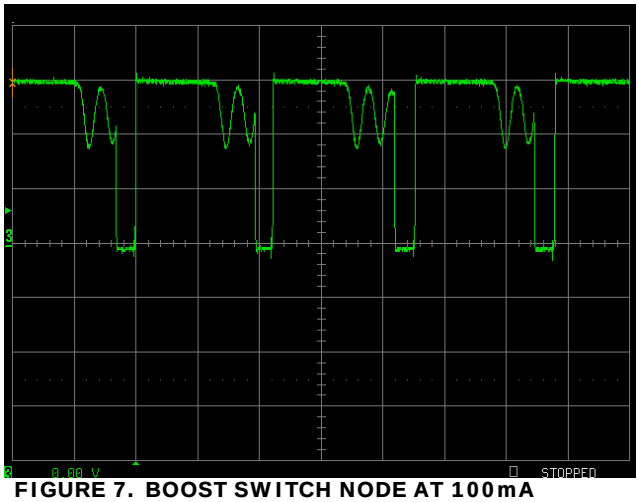


FIGURE 7. BOOST SWITCH NODE AT 100mA (PARTIAL CONTINUOUS)

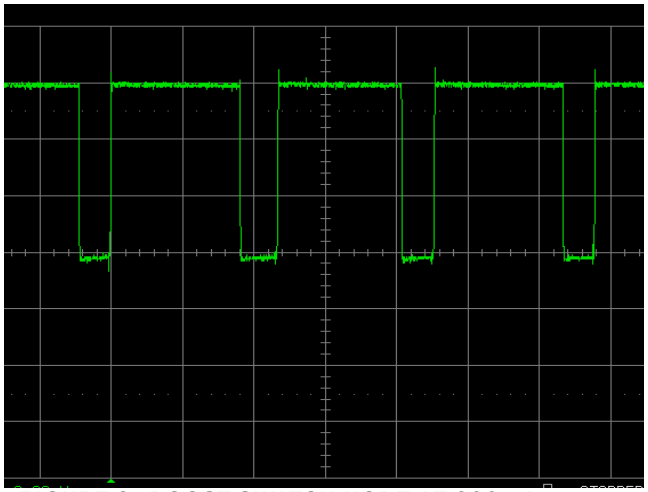


FIGURE 8. BOOST SWITCH NODE AT 300mA (CONTINUOUS MODE)

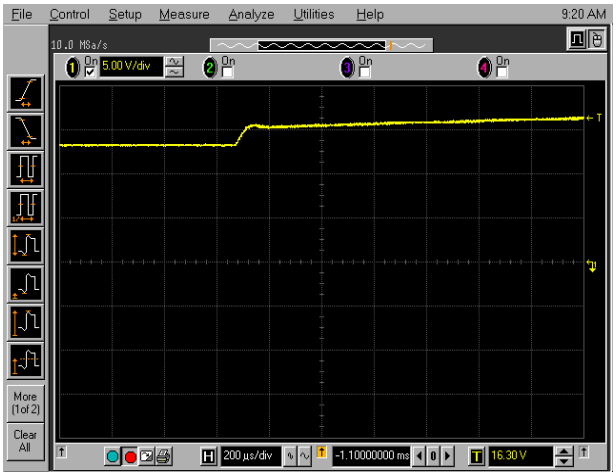


FIGURE 9. VLBNB TRANSITIONS FROM 13.3V TO 18.3V

Typical Performance Curves (Continued)

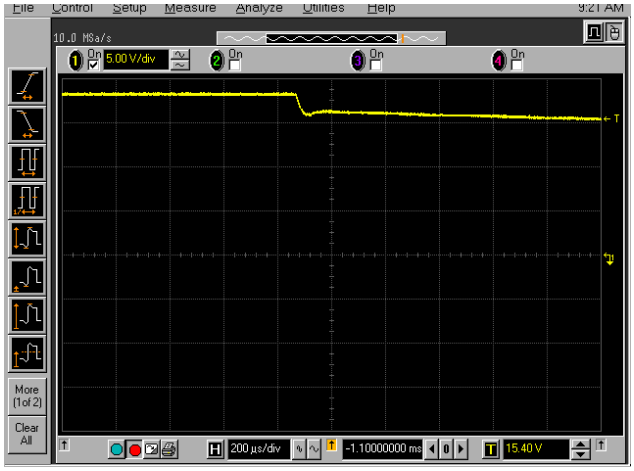


FIGURE 10. VLNB TRANSITIONS FROM 18.3V TO 13.3V

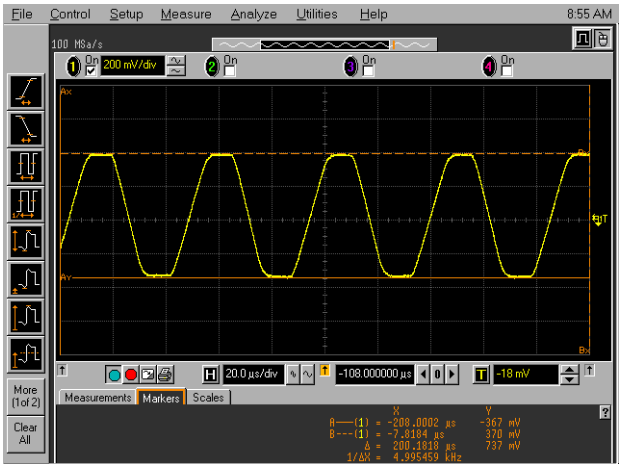


FIGURE 11. 22kHz TONE ON 13.3V_{OUT} WITH 50mA LOAD

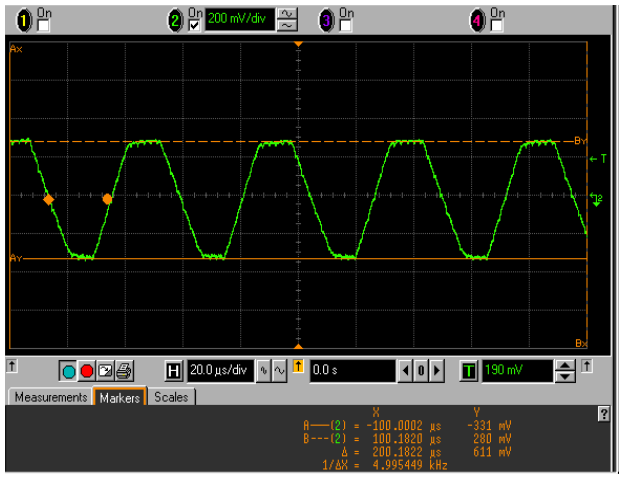


FIGURE 12. 22kHz TONE ON 13.3V_{OUT} WITH 500mA LOAD

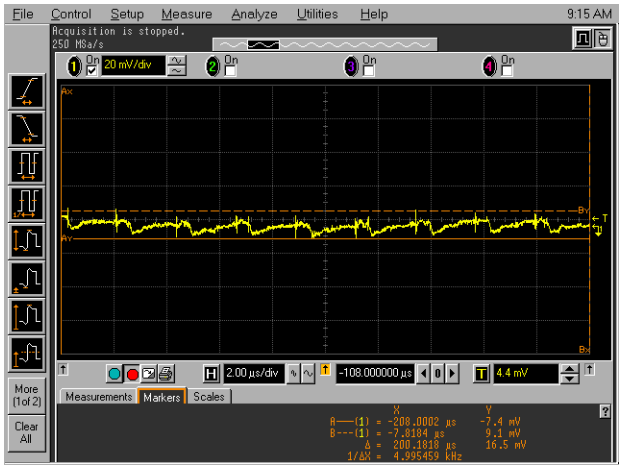


FIGURE 13. AC NOISE ON 13.3V_{OUT} AT 500mA OF LOAD

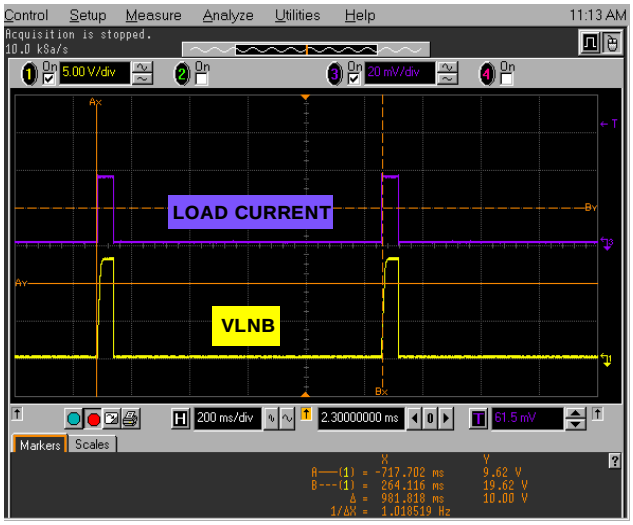


FIGURE 14. VLNB CONNECTED TO 350mA LOAD WITH R_{ILIM} = 148k

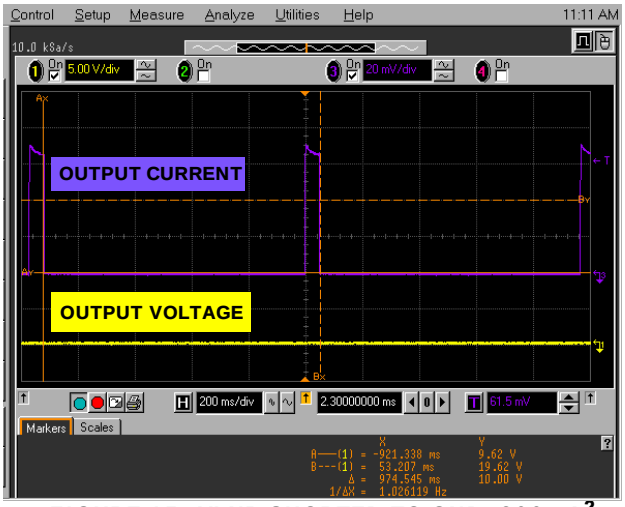


FIGURE 15. VLNB SHORTED TO GND, 200mA[2]

Typical Performance Curves (Continued)

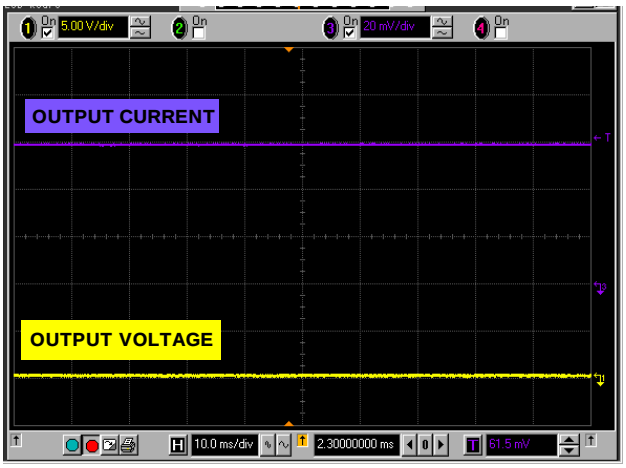


FIGURE 16. OUTPUT CURRENT AND VOLTAGE WITH OUTPUT SHORTED TO GND, R_{ILIM} = 0

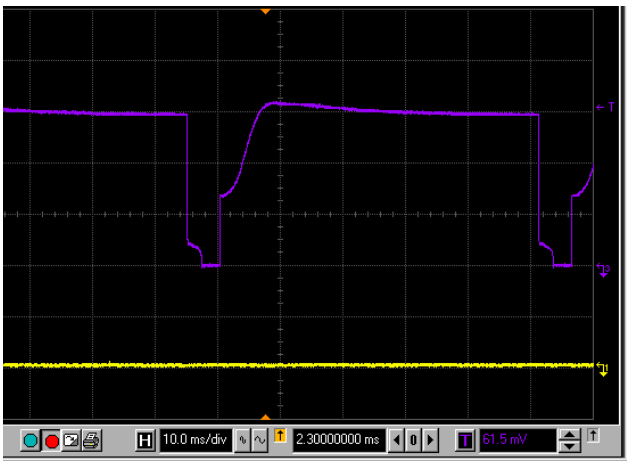


FIGURE 17. THE ISL9491 ENTERING THERMAL SHUTDOWN WITH R_{ILIM} = 0

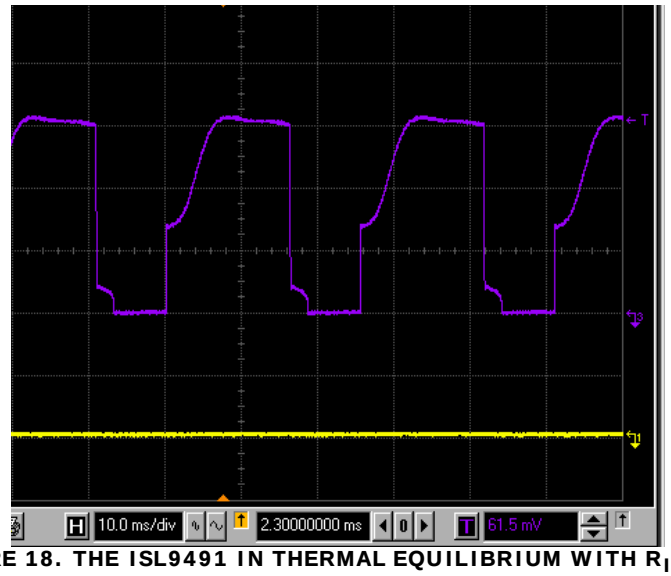


FIGURE 18. THE ISL9491 IN THERMAL EQUILIBRIUM WITH R_{ILIM} = 0

Functional Description

The ISL9491 or ISL9491A single output voltage regulator makes an ideal choice for advanced satellite set-top box and personal video recorder applications. The device utilizes built-in DC/DC step-up converters, which operate from a single supply source ranging from 8V to 14V and generate the voltage needed to enable the linear post-regulator to work with minimum dissipated power. An undervoltage lockout circuit disables the device when VCC drops below a fixed threshold (4.5V typical).

DiSEqC Encoding

The EXTM accepts an externally modulated tone command and in turn modulates the V_{LNB} symmetrically to meet the DiSEqC 1.0 and DiSEqC 2.0 transmit protocol. Burst coding of the tone can be accomplished due to the fast response of the EXTM pin.

Linear Regulator

The output linear regulator is designed to source 500mA continuous current and 750mA peak. The sink feature is limited and thus requires a bleeder resistor of 3.3kΩ to be connected at the VLNB to enable proper tone modulation capability into capacitive loads as high as 0.22µF. In order to minimize the power dissipation, the output voltage of the internal step-up converter is adjusted to allow the linear regulator to work at a minimum dropout of 1.2V typical (Load current = 500mA) between the VSW and VOUT pin. The VOUT pin drives the anode of the back diode and the VSENSE pin drives the cathode of the back diode. The VSENSE pin is capable of withstanding a back voltage of 24V.

When the device is put in the shutdown mode (EN = LOW), the PWM power block is disabled. When the regulator blocks are active (EN = HIGH), the output can be controlled by the VSET0 and VSET1 pins to be 13.3V, 14.3V, 18.3V or 20V (typical ISL9491) or 11V, 12V, 15V, or 16V (typical ISL9491A) for remote controlling of non-DiSEqC LNBs.

A separate open-drain FAULT pin serves as an interrupt and is driven low by undervoltage, overvoltage and linear overcurrent and over-temperature faults.

Output Voltage Rise and Fall TimeTiming

The output voltage rise and fall times or soft-start time can be set by an the external capacitor on the TCAP pin. The output rise and fall times are given by Equation 1:

$$C = \frac{220 t_{rise}}{\Delta V} \quad \text{(EQ. 1)}$$

Where C is the TCAP value in nF, t_{rise} the required transition time in ms and ΔV is the differential transition voltage from low output voltage range to the high output range in Volts.

Too large a value of TCAP prevents the output from rising to the nominal value, within a reasonable time. Too small a value of the TCAP can cause high peak currents in the boost circuit. Figures 4 and 5 show the output voltage rise time for TCAP value of 0.22µF and 0.44µF as 13.6ms and 32ms which according to Equation 1 should be 13.3ms and 26.6ms. The difference between measured and calculated values is due to capacitor tolerance of ± 20%. Since the output voltage uses TCAP voltage as a reference, it is recommended to use a 10kΩ resistor in series to filter out some of the switching noise from injecting on this pin.

Dynamic and Static Current Limiting

When the LDO current exceeds the preset overcurrent threshold set by means of a resistor from the ILIMIT pin to GND for a period of 50ms, the device enters a t_{ON} = 50ms/t_{OFF} = 900ms routine. This type of current limiting is also called “Dynamic Current Limiting”, which is used extensively on other Intersil LNB controllers. A linear overcurrent will drive the FAULT pin low during the t_{OFF} = 900ms period. This operation continues until the fault is removed. Upon removal of the fault, the device returns to normal operation after a successful soft-start cycle. Figure 14 shows the output current and voltage waveforms with an I_{LIMIT} resistor of 148kΩ and a load current of 350mA. It can be seen that under this loading condition, the chip stays powered up and sources load current for 50ms and turns-off for approximately 900ms. The output voltage ramps up to programmed output voltage during the on time.This cycle repeats itself until load current is reduced below the current limit value of 350mA. Equation 2 shows the relationship between ILIMIT resistor and load current:

$$ILIMIT = 52,000 \times \frac{\alpha}{R_{ILIMIT}} \quad \text{(EQ. 2)}$$

I_{LIMIT} is the programmed load current in mA before the chip goes into current limit where R_{ILIMIT} is in kΩ. Alpha (α) is a gain term which is shown in Figure 19 and has a value of one at 350mA. It is a good design practice to use a 1% tolerance resistor and allow for at least 20% higher margin on the maximum load current when calculating the R_{ILIMIT} resistor value.

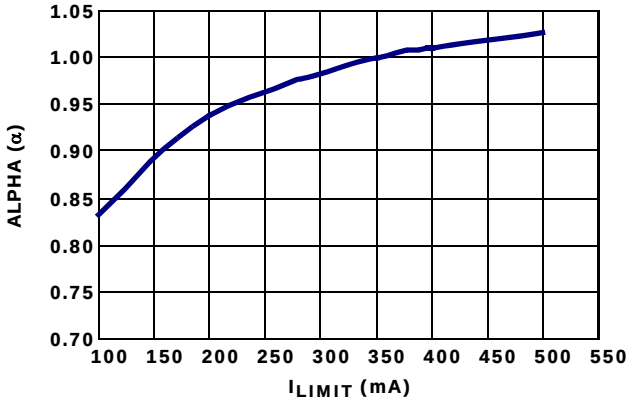


FIGURE 19. ALPHA CONSTANT

Figure 15 shows the output current and voltage for R_{ILIMIT} =148kΩ when the output voltage is shorted to GND. Under this condition, the chip still exhibits the 50ms on and 900ms off pulse to minimize power dissipation, however, current gets internally clamped to approximately 750mA. The output voltage stays at 0V

due to hard short on the output. The current limiting described so far is called “Dynamic Current” limiting which limits current to approximately 750mA for 50ms and turns off the output for 900ms. R_{ILIM} is used to program the current level at which the ISL9491 enters into this protection mode. On the other hand, the ISL9491 can also be programmed in “Static Current Limit” mode which defeats the 50ms/900ms(on/off) pulse by delivering constant 750mA load current to the system by using a 0Ω R_{ILIMIT} resistor. In this mode the chip will deliver this current to the load for as long as the die junction temperature is less than 130ºC. Figure 16 shows the static current limit by shorting the output to GND. It also shows that initially the chip delivers 750mA but the junction starts heating up since approximately 10W (13.3V*0.75A) is being dissipated internally. The thermal shutdown circuitry takes over and shuts the output LDO stage-off after approximately 50ms and the load current drops to zero as seen in Figure 17. The chip restarts as soon as the junction temperature drops below the thermal shutdown level but quickly shuts off in 15ms as seen in Figure 18.

The CS pin provides peak current protection for the Boost FET on a pulse-by-pulse basis. Once the voltage on the FET source sense resistor crosses 0.45V typical, the Boost FET drive is set to low. The sense resistor can be sized to limit the peak current through the FET. It is highly recommended to have a boost current limit of 200% when sizing the sense resistor to accommodate high current transients in the boost circuit.

Thermal Protection

This IC is protected against overheating. When the junction temperature exceeds +130°C (typical), the step-up converter and the linear regulator are shut-off. When the junction is cooled down to +110°C (typical), normal operation is resumed.

External Output Voltage Selection

The pin VSET0 and VSET1 are provided for switching between typical output voltages, as indicated in Table 1.

TABLE 1.

EN	VSET1	VSET0	VLNB ISL9491	VLNB ISL9491A
0	X	X	Disabled	Disabled
1	0	0	13.3V	11.0V
1	0	1	18.3V	15.0V
1	1	0	14.3V	12.0V
1	1	1	20.0V	16.0V

Output Over/Undervoltage Fault and EXTM

The recommended start-up sequence is Vcc going high followed by ENABLE while EXTM is pulled low. This will start the output voltage to ramp up with a dv/dt which is based on the TCAP value. Once ENABLE is pulled high, allow a 50ms delay before applying 22kHz/44kHz, 50% square pulse on EXTM pin to generate the DISEQ tone on the output. At this point, FAULT should also be high, indicating that output voltage is in regulation. FAULT is designed to stay high when the output voltage is commanded to transition between the values listed in Table 1, and also when passing the DiSEQ tone on the output. FAULT will immediately pull low if there is a short on the output or if the voltage falls outside the ± 10% window indicating that the voltage is out of regulation. FAULT signal is armed after the first initial power-up when output voltage is in steady-state. If tone is applied to the EXTM pin before the chip is ENABLED, it causes the FAULT to remain low even after the output voltage reaches steady state. This issue can be resolved by pulling the EXTM low for 2 cycles which is 90ms of ISL9491 and 45ms for ISL9491A.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 12, 2015	FN6531.1	Updated Ordering Information table on page 1. Added Revision History and About Intersil sections.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

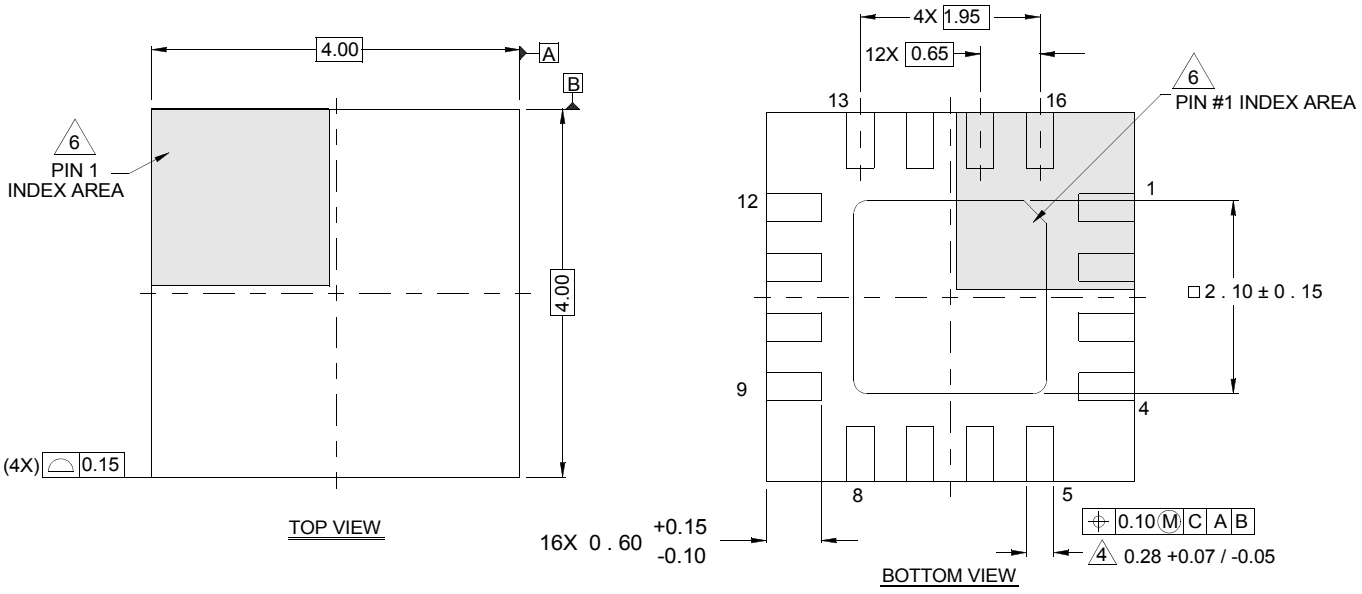
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

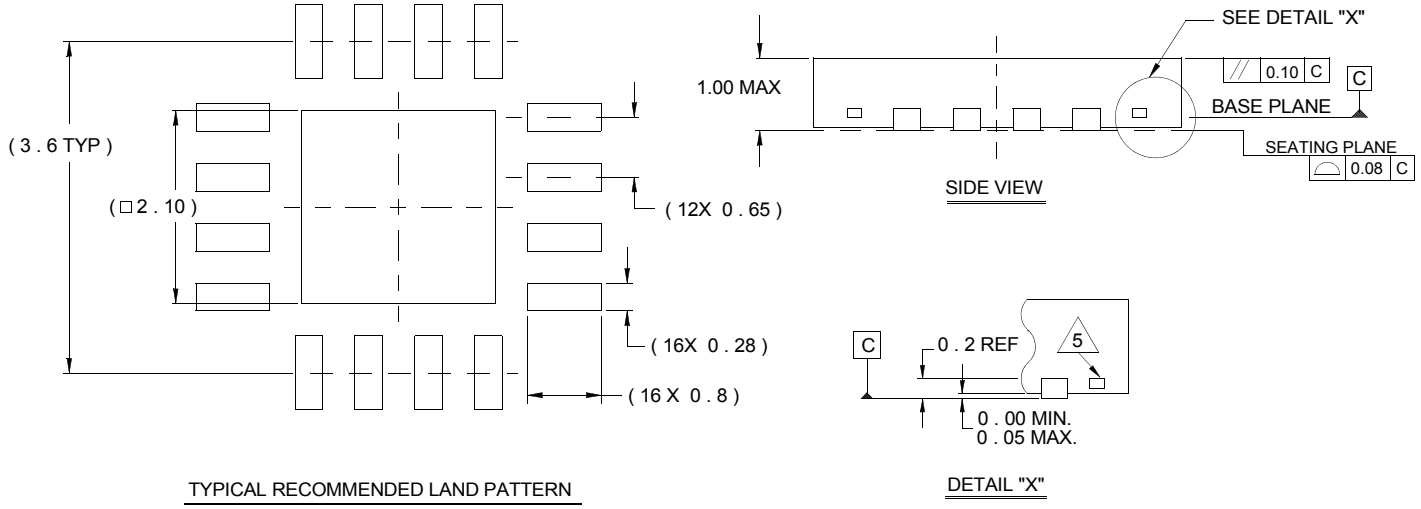
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 6, 02/08





NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.