

DM74LS373 • DM74LS374

3-STATE Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the DM74LS373 are transparent D-type latches meaning that while the enable (G) is HIGH the Q outputs will follow the data (D) inputs. When the enable is taken LOW the output will be latched at the level of the data that was set up.

The eight flip-flops of the DM74LS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (HIGH or LOW logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are OFF.

Features

- Choice of 8 latches or 8 D-type flip-flops in a single package
- 3-STATE bus-driving outputs
- Full parallel-access for loading
- Buffered control inputs
- P-N-P inputs reduce D-C loading on data lines

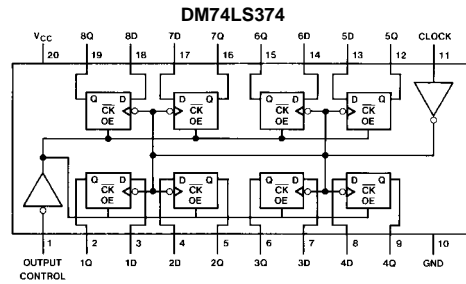
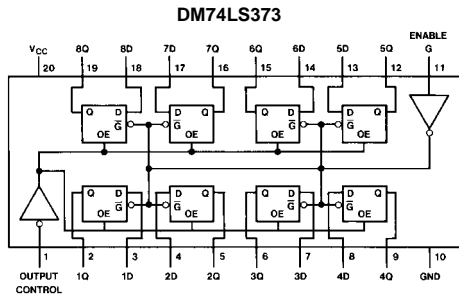
Ordering Code:

Order Number	Package Number	Package Description
DM74LS373WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
DM74LS373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS373N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
DM74LS374WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
DM74LS374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS374N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

DM74LS373 • DM74LS374 3-STATE Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

Connection Diagrams



Function Tables

DM74LS373

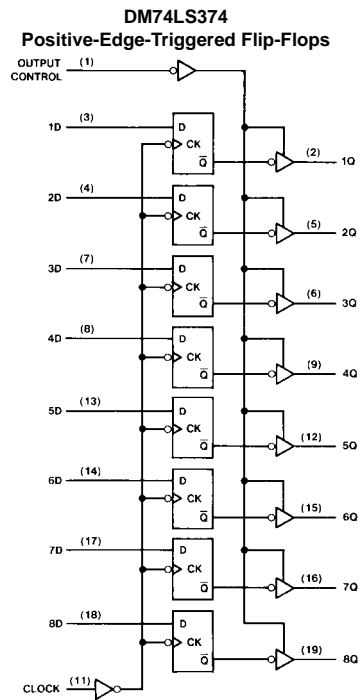
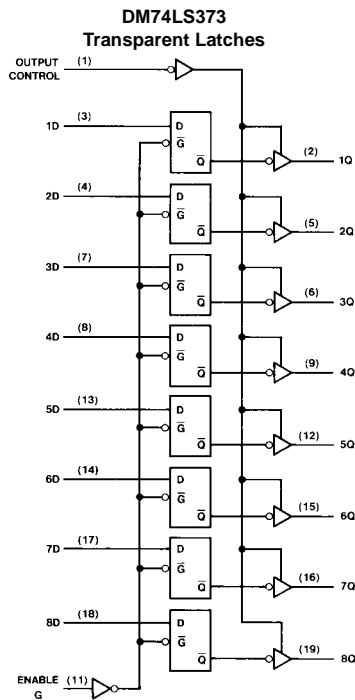
Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

DM74LS374

Output Control	Clock	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

H = HIGH Level (Steady State) L = LOW Level (Steady State)
 X = Don't Care Z = High Impedance State
 ↑ = Transition from LOW-to-HIGH level Q₀ = The level of the output before steady-state input conditions were established.

Logic Diagrams



Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	-65°C to +150°C
Operating Free Air Temperature Range	0°C to +70°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DM74LS373 Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			-2.6	mA
I_{OL}	LOW Level Output Current			24	mA
t_W	Pulse Width (Note 3)	Enable HIGH	15		ns
		Enable LOW	15		
t_{SU}	Data Setup Time (Note 2) (Note 3)	5↓			ns
t_H	Data Hold Time (Note 2) (Note 3)	20↓			ns
T_A	Free Air Operating Temperature	0		70	°C

Note 2: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 3: $T_A = 25^\circ\text{C}$ and $V_{CC} = 5\text{V}$.

DM74LS373 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}$, $I_I = -18\text{ mA}$			-1.5	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$	2.4	3.1		V
		$V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$				
V_{OL}	LOW Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OL} = \text{Max}$		0.35	0.5	V
		$V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$ $I_{OL} = 12\text{ mA}$, $V_{CC} = \text{Min}$				
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$, $V_I = 7\text{V}$			0.1	mA
I_{IH}	HIGH Level Input Current	$V_{CC} = \text{Max}$, $V_I = 2.7\text{V}$			20	μA
I_{IL}	LOW Level Input Current	$V_{CC} = \text{Max}$, $V_I = 0.4\text{V}$			-0.4	mA
I_{OZH}	Off-State Output Current with HIGH Level Output Voltage Applied	$V_{CC} = \text{Max}$, $V_O = 2.7\text{V}$ $V_{IH} = \text{Min}$, $V_{IL} = \text{Max}$			20	μA
I_{OZL}	Off-State Output Current with LOW Level Output Voltage Applied	$V_{CC} = \text{Max}$, $V_O = 0.4\text{V}$ $V_{IH} = \text{Min}$, $V_{IL} = \text{Max}$			-20	μA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 5)	-50		-225	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}$, $OC = 4.5\text{V}$, D_n , Enable = GND		24	40	mA

Note 4: All typicals are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

DM74LS373 Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ C$

Symbol	Parameter	From (Input) To (Output)	$R_L = 667\Omega$				Units
			$C_L = 45\text{ pF}$		$C_L = 150\text{ pF}$		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Data to Q		18		26	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Data to Q		18		27	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Q		30		38	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Q		30		36	ns
t_{PZH}	Output Enable Time to HIGH Level Output	Output Control to Any Q		28		36	ns
t_{PZL}	Output Enable Time to LOW Level Output	Output Control to Any Q		36		50	ns
t_{PHZ}	Output Disable Time from HIGH Level Output (Note 6)	Output Control to Any Q		20			ns
t_{PLZ}	Output Disable Time from LOW Level Output (Note 6)	Output Control to Any Q		25			ns

Note 6: $C_L = 5\text{ pF}$.

DM74LS374 Recommended Operating Conditions

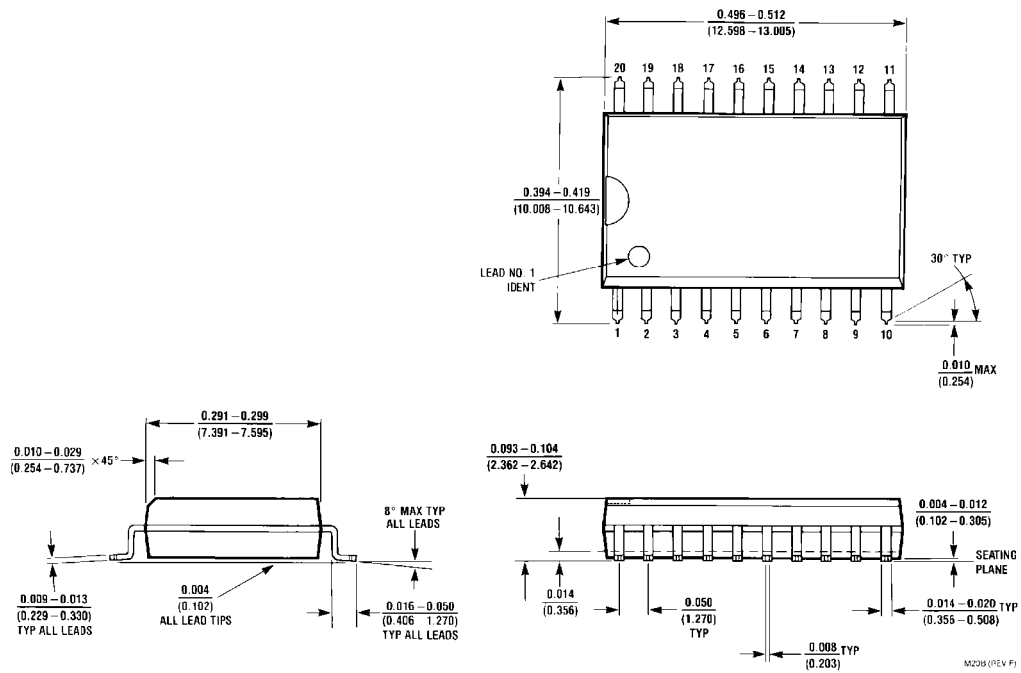
Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			-2.6	mA
I_{OL}	LOW Level Output Current			24	mA
t_W	Pulse Width (Note 8)	Clock HIGH	15		ns
		Clock LOW	15		
t_{SU}	Data Setup Time (Note 7) (Note 8)	$20\uparrow$			ns
t_H	Data Hold Time (Note 7) (Note 8)	$1\uparrow$			ns
T_A	Free Air Operating Temperature	0		70	$^\circ C$

Note 7: The symbol (\uparrow) indicates the rising edge of the clock pulse is used for reference.

Note 8: $T_A = 25^\circ C$ and $V_{CC} = 5V$.

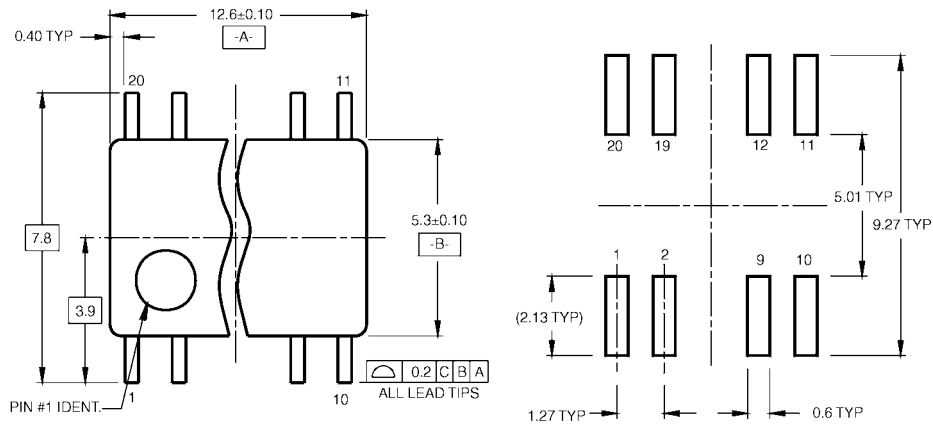
DM74LS374 Electrical Characteristics						
over recommended operating free air temperature range (unless otherwise noted)						
Symbol	Parameter	Conditions	Min	Typ (Note 9)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$	2.4	3.1		V
V_{OL}	LOW Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = \text{Max}$ $V_{IL} = \text{Max}, V_{IH} = \text{Min}$ $I_{OL} = 12 \text{ mA}, V_{CC} = \text{Min}$		0.35 0.25	0.5 0.4	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}, V_I = 7\text{V}$			0.1	mA
I_{IH}	HIGH Level Input Current	$V_{CC} = \text{Max}, V_I = 2.7\text{V}$			20	μA
I_{IL}	LOW Level Input Current	$V_{CC} = \text{Max}, V_I = 0.4\text{V}$			-0.4	mA
I_{OZH}	Off-State Output Current with HIGH Level Output Voltage Applied	$V_{CC} = \text{Max}, V_O = 2.7\text{V}$ $V_{IH} = \text{Min}, V_{IL} = \text{Max}$			20	μA
I_{OZL}	Off-State Output Current with LOW Level Output Voltage Applied	$V_{CC} = \text{Max}, V_O = 0.4\text{V}$ $V_{IH} = \text{Min}, V_{IL} = \text{Max}$			-20	μA
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 10)	-50		-225	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}, D_n = \text{GND}, \text{OC} = 4.5\text{V}$		27	45	mA
Note 9: All typicals are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.						
Note 10: Not more than one output should be shorted at a time, and the duration should not exceed one second.						
DM74LS374 Switching Characteristics						
at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$						
Symbol	Parameter	$R_L = 667\Omega$				Units
		$C_L = 45 \text{ pF}$		$C_L = 150 \text{ pF}$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	35		20		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		28		32	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		28		38	ns
t_{PZH}	Output Enable Time to HIGH Level Output		28		44	ns
t_{PZL}	Output Enable Time to LOW Level Output		28		44	ns
t_{PHZ}	Output Disable Time from HIGH Level Output (Note 11)		20			ns
t_{PLZ}	Output Disable Time from LOW Level Output (Note 11)		25			ns
Note 11: $C_L = 5 \text{ pF}$.						

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



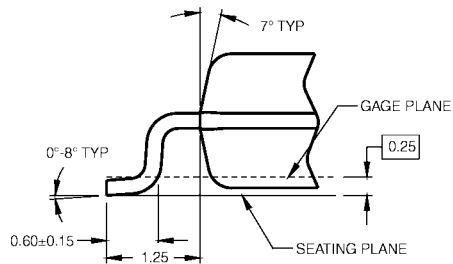
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

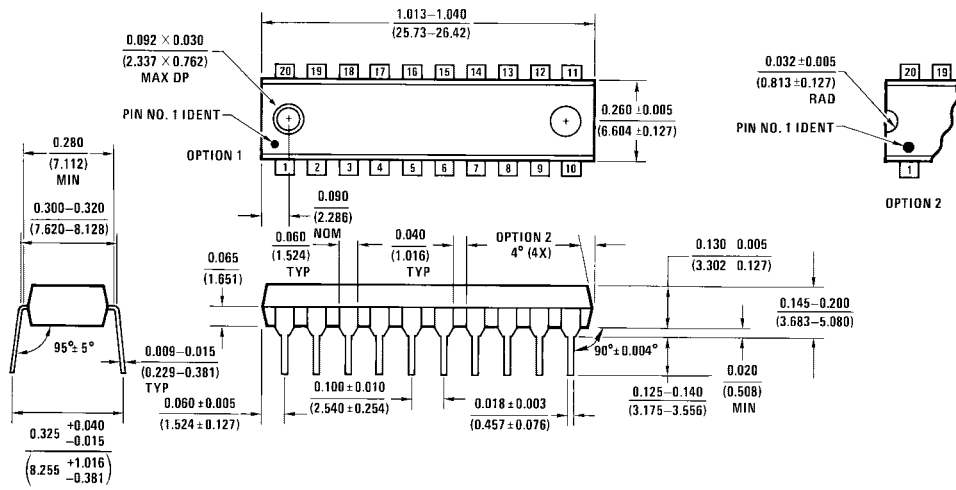
M20DRevB1



DETAIL A

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com