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# 32-Bit

Microcontroller

# TC1728

32-Bit Single-Chip Microcontroller

## Data Sheet

V1.2 2014-06

Microcontrollers

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# TC1728

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# 1 Summary of Features

The **SAK-TC1728N-192F133HL** / **SAK-TC1728N-192F133HR** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 133 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 8 Kbyte Parameter Memory (PRAM)
  - 24 Kbyte Code Memory (CMEM)
  - 133 MHz operation at full temperature range
- Multiple on-chip memories
  - 1.5 Mbyte Program Flash Memory (PFLASH) with ECC
  - 64 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 120 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 8Kbyte (ICACHE, configurable)
  - 24 Kbyte Code Scratchpad Memory (SPRAM)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with $2 \times 255$ hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Four High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 3 CAN nodes and 64 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer

  - One General Purpose Timer Array Module (GPTA) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two Capture/Compare Unit 6 (CAPCOM6) kernels
  - Two General Purpose Timer (GPT12) modules
- 36 analog input lines for ADC
  - 2 independent kernels (ADC0 and ADC1)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
  - Broken wire detection
- 2 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of $f_{FADC}$ clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 127 digital general purpose I/O lines (GPIO), 3 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1728ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

The **SAK-TC1728F-192F133HL / SAK-TC1728F-192F133HR** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 133 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 8 Kbyte Parameter Memory (PRAM)
  - 24 Kbyte Code Memory (CMEM)
  - 133 MHz operation at full temperature range
- Multiple on-chip memories
  - 1.5 Mbyte Program Flash Memory (PFLASH) with ECC
  - 64 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 120 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 8Kbyte (ICACHE, configurable)
  - 24 Kbyte Code Scratchpad Memory (SPRAM)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)

  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with 2 × 255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Four High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 3 CAN nodes and 64 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer
  - One FlexRay™ module with 2 channels (E-Ray).
  - One General Purpose Timer Array Module (GPTA) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two Capture/Compare Unit 6 (CAPCOM6) kernels
  - Two General Purpose Timer (GPT12) modules
- 36 analog input lines for ADC
  - 2 independent kernels (ADC0 and ADC1)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
  - Broken wire detection
- 2 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of $f_{FADC}$ clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 127 digital general purpose I/O lines (GPIO), 3 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1728ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

### Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1728 please refer to the **"Product Catalog Microcontrollers"**, which summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 1** enumerates these derivatives and summarizes the differences.

**Table 1 TC1728 Derivative Synopsis**

| Derivative | Ambient Temperature Range | ERAY | Wire Bond Material |
|---|---|---|---|
| SAK-TC1728N-192F133HL | $T_A$ = -40°C to +125°C | No | Gold |
| SAK-TC1728N-192F133HR[1)] | $T_A$ = -40°C to +125°C | No | Copper |
| SAK-TC1728F-192F133HR[2)] | $T_A$ = -40°C to +125°C | Yes | Copper |
| SAK-TC1728F-192F133HL | $T_A$ = -40°C to +125°C | Yes | Gold |

1) This derivative has the same features as the SAK-TC1728N-192F133HL, except the wire-bonding material.

2) This derivative has the same features as the SAK-TC1728F-192F133HL, except the wire-bonding material.

# 2 System Overview of the TC1728

The TC1728 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1728 include:

- Efficient memory organization: instruction and data scratch memories, caches
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

The TC1728 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor and a DMA controller and several on-chip peripherals. The TC1728 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1728 offers several versatile on-chip peripheral units such as serial controllers, timer units, CAPCOM6 and Analog-to-Digital converters. Within the TC1728, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Local Memory Bus (LMB). Several I/O lines on the TC1728 ports are reserved for these peripheral units to communicate with the external world.

## 2.1 Block Diagrams

Figure 1 shows the block diagram of the SAK-TC1728N-192F133HL./ SAK-TC1728N-192F133HR.

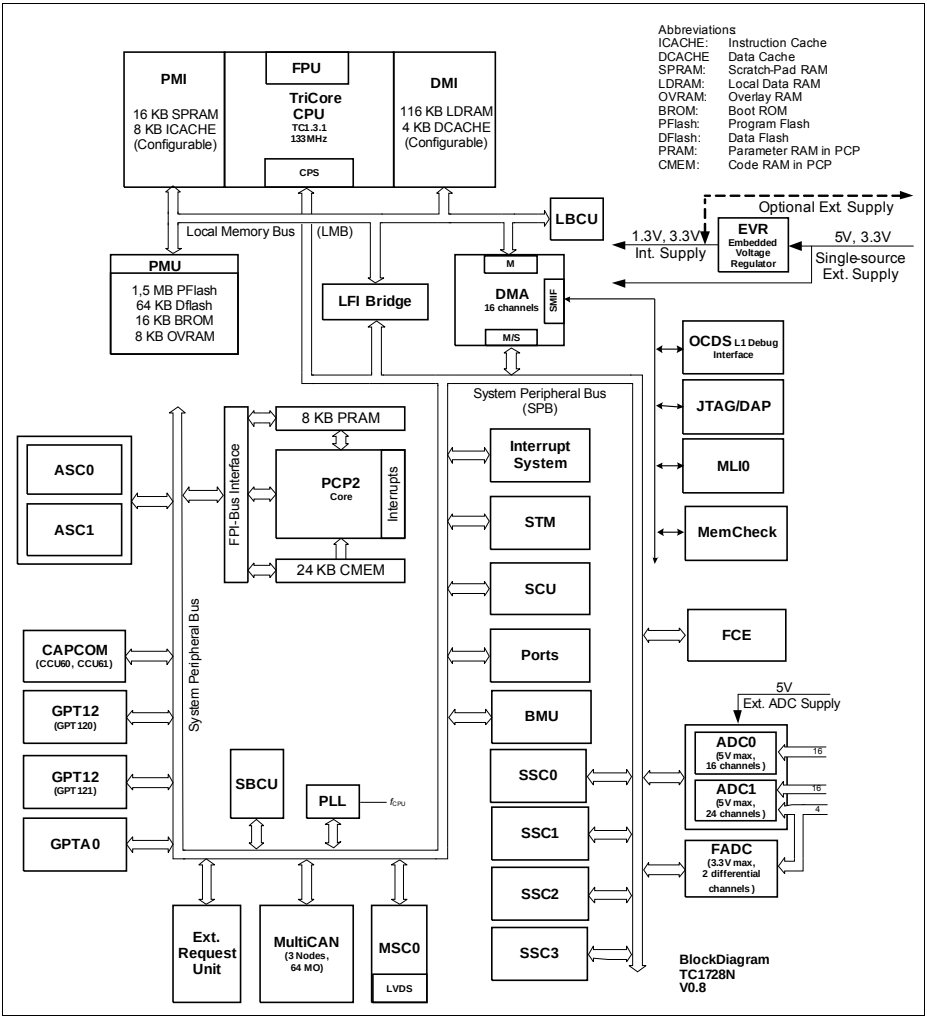



**Figure 1 SAK-TC1728N-192F133HL / SAK-TC1728N-192F133HR Block Diagram**

**Figure 2** shows the block diagram of the SAK-TC1728F-192F133HL / SAK-TC1728F-192F133HR.

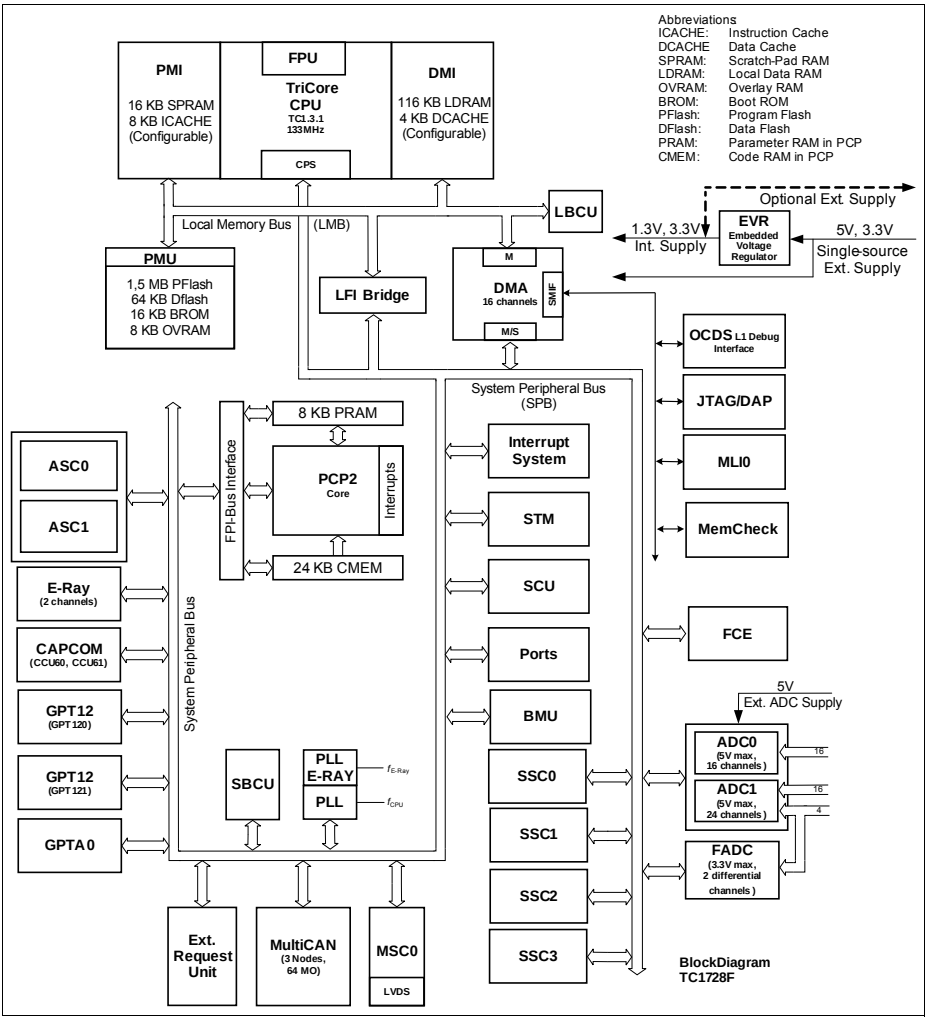



**Figure 2 SAK-TC1728F-192F133HR Block Diagram**

# 3 Pinning

**Figure 3-1** shows the TC1728 Logic Symbol.

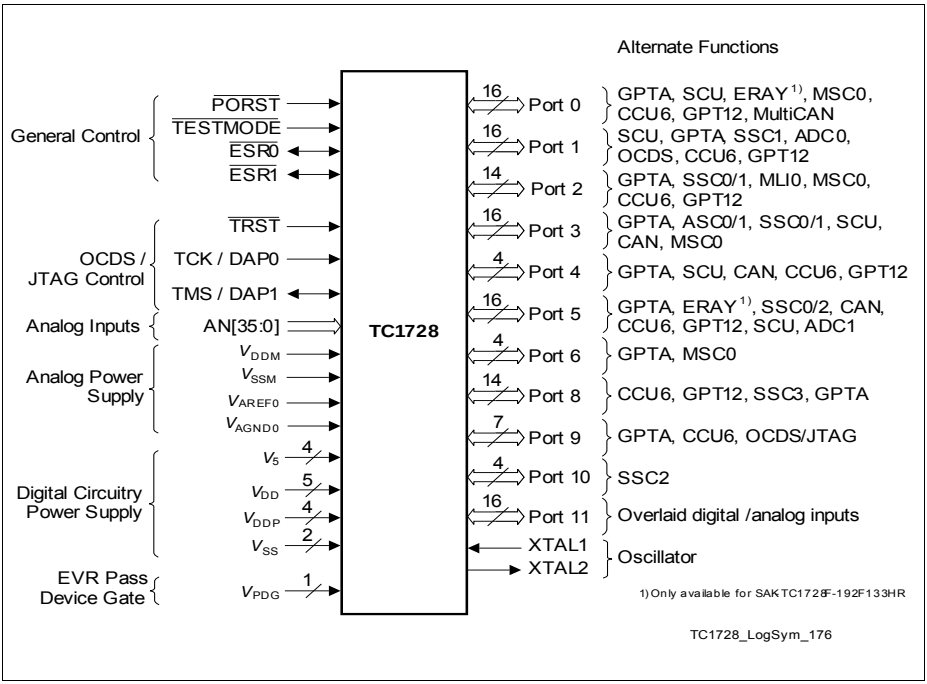



**Figure 3-1 TC1728 Logic Symbol**

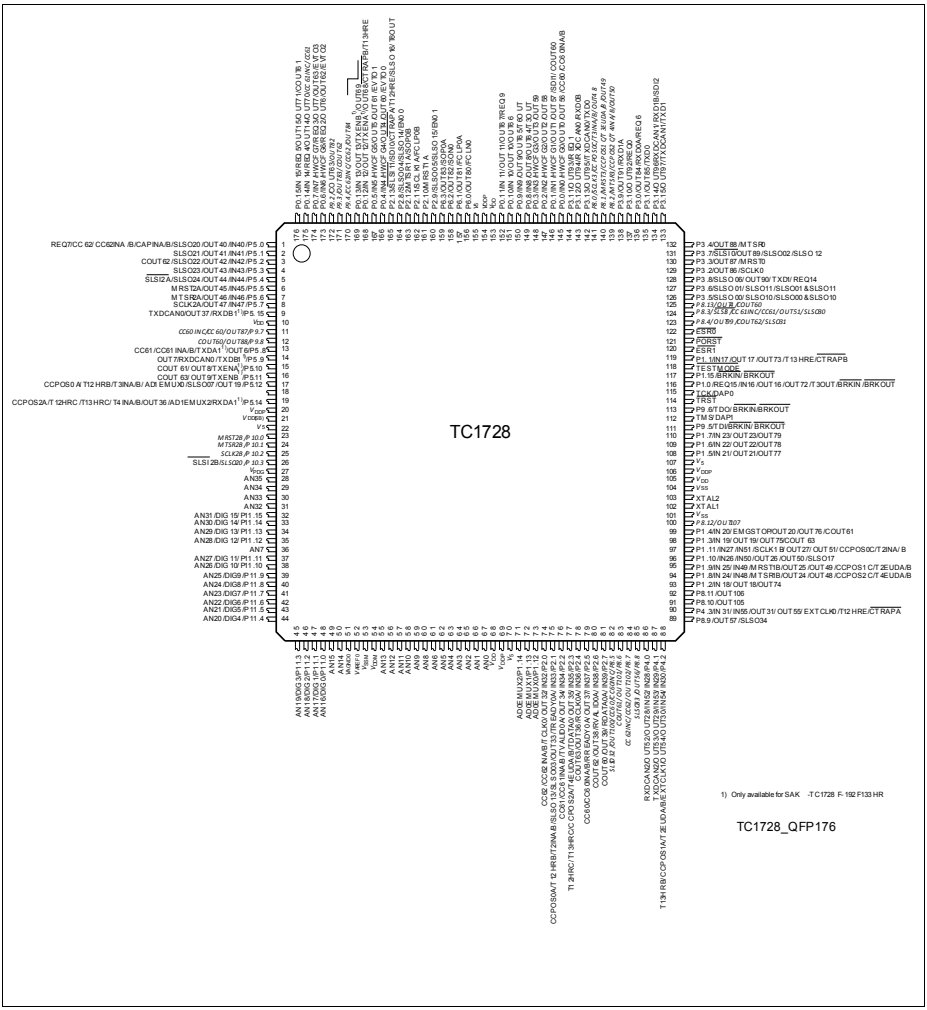



**Figure 3-2 SAK-TC1728N-192F133HL / SAK-TC1728N-192F133HR / SAK-TC1728F-192F133HR Pinning**

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| **Port 0** | | | | |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 145 | P0.0 | I/O0 | A1/ PU | **Port 0 General Purpose I/O Line 0** |
| | IN0 | I | | **GPTA0 Input 0** |
| | CCU60 | I | | **CC60INA** |
| | CCU61 | I | | **CC60INB** |
| | HWCFG0 | I | | **Hardware Configuration Input 0** |
| | OUT0 | O1 | | **GPTA0 Output 0** |
| | OUT56 | O2 | | **GPTA0 Output 56** |
| | CCU60 | O3 | | **CC60** |
| 146 | P0.1 | I/O0 | A1/ PU | **Port 0 General Purpose I/O Line 1** |
| | IN1 | I | | **GPTA0 Input 1** |
| | SDI1 | I | | **MSC0 Serial Data Input 1** |
| | HWCFG1 | I | | **Hardware Configuration Input 1** |
| | OUT1 | O1 | | **GPTA0 Output 1** |
| | OUT57 | O2 | | **GPTA0 Output 57** |
| | CCU60 | O3 | | **COUT60** |
| 147 | P0.2 | I/O0 | A1/ PU | **Port 0 General Purpose I/O Line 2** |
| | IN2 | I | | **GPTA0 Input 2** |
| | HWCFG2 | I | | **Hardware Configuration Input 2** |
| | OUT2 | O1 | | **GPTA0 Output 2** |
| | OUT58 | O2 | | **GPTA0 Output 58** |
| | Reserved | O3 | | **-** |
| 148 | P0.3 | I/O0 | A1+/ PU | **Port 0 General Purpose I/O Line 3** |
| | IN3 | I | | **GPTA0 Input 3** |
| | HWCFG3 | I | | **Hardware Configuration Input 3** |
| | OUT3 | O1 | | **GPTA0 Output 3** |
| | OUT59 | O2 | | **GPTA0 Output 59** |
| | Reserved | O3 | | **-** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 166 | P0.4 | I/O0 | A1/ PD | **Port 0 General Purpose I/O Line 4** |
| | IN4 | I | | **GPTA0 Input 4** |
| | HWCFG4 | I | | **Hardware Configuration Input 4** |
| | OUT4 | O1 | | **GPTA0 Output 4** |
| | OUT60 | O2 | | **GPTA0 Output 60** |
| | EVTO0 | O3 | | **MCDS event output 0** |
| 167 | P0.5 | I/O0 | A1/ PD | **Port 0 General Purpose I/O Line 5** |
| | IN5 | I | | **GPTA0 Input 5** |
| | HWCFG5 | I | | **Hardware Configuration Input 5** |
| | OUT5 | O1 | | **GPTA0 Output 5** |
| | OUT61 | O2 | | **GPTA0 Output 61** |
| | EVTO1 | O3 | | **MCDS event output 1** |
| 173 | P0.6 | I/O0 | A1/ PU | **Port 0 General Purpose I/O Line 6** |
| | IN6 | I | | **GPTA0 Input 6** |
| | HWCFG6 | I | | **Hardware Configuration Input 6** |
| | REQ2 | I | | **External Request Input 2** |
| | OUT6 | O1 | | **GPTA0 Output 6** |
| | OUT62 | O2 | | **GPTA0 Output 62** |
| | EVTO2 | O3 | | **MCDS event output 2** |
| 174 | P0.7 | I/O0 | A1/ PU | **Port 0 General Purpose I/O Line 7** |
| | IN7 | I | | **GPTA0 Input 7** |
| | HWCFG7 | I | | **Hardware Configuration Input 7** |
| | REQ3 | I | | **External Request Input 3** |
| | OUT7 | O1 | | **GPTA0 Output 7** |
| | OUT63 | O2 | | **GPTA0 Output 63** |
| | EVTO3 | O3 | | **MCDS event output 3** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 149 | P0.8 | I/O0 | A1/ PU | **Port 0 General Purpose I/O Line 8** |
| | IN8 | I | | **GPTA0 Input 8** |
| | OUT8 | O1 | | **GPTA0 Output 8** |
| | OUT64 | O2 | | **GPTA0 Output 64** |
| | GPT121 | O3 | | **T3OUT** |
| 150 | P0.9 | I/O0 | A1/ PU | **Port 0 General Purpose I/O Line 9** |
| | IN9 | I | | **GPTA0 Input 9** |
| | OUT9 | O1 | | **GPTA0 Output 9** |
| | OUT65 | O2 | | **GPTA0 Output 65** |
| | GPT121 | O3 | | **T6OUT** |
| 151 | P0.10 | I/O0 | A2/ PU | **Port 0 General Purpose I/O Line 10** |
| | IN10 | I | | **GPTA0 Input 10** |
| | OUT10 | O1 | | **GPTA0 Output 10** |
| | OUT66 | O2 | | **GPTA0 Output 66** |
| | Reserved | O3 | | **-** |
| 152 | P0.11 | I/O0 | A2/ PU | **Port 0 General Purpose I/O Line 11** |
| | IN11 | I | | **GPTA0 Input 11** |
| | REQ9 | I | | **External Request Input 9** |
| | OUT11 | O1 | | **GPTA0 Output 11** |
| | OUT67 | O2 | | **GPTA0 Output 67** |
| | Reserved | O3 | | **-** |
| 168 | P0.12 | I/O0 | A2/ PU | **Port 0 General Purpose I/O Line 12** |
| | IN12 | I | | **GPTA0 Input 12** |
| | CCU60 | I | | **$\overline{\text{CTRAPB}}$** |
| | CCU61 | I | | **T13HRE** |
| | OUT12 | O1 | | **GPTA0 Output 12** |
| | OUT68 | O2 | | **GPTA0 Output 68** |
| | TXENA | O3 | | **E-Ray Channel A transmit Data Output enable**[1)] |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 169 | P0.13 | I/O0 | A2/ PU | **Port 0 General Purpose I/O Line 13** |
| | IN13 | I | | **GPTA0 Input 13** |
| | OUT13 | O1 | | **GPTA0 Output 13** |
| | OUT69 | O2 | | **GPTA0 Output 69** |
| | TXENB | O3 | | **E-Ray Channel B transmit Data Output enable**[1)] |
| 175 | P0.14 | I/O0 | A1+/ PU | **Port 0 General Purpose I/O Line 14** |
| | IN14 | I | | **GPTA0 Input 14** |
| | REQ4 | I | | **External Request Input 4** |
| | CCU61 | I | | **CC61INC** |
| | OUT14 | O1 | | **GPTA0 Output 14** |
| | OUT70 | O2 | | **GPTA0 Output 70** |
| | CCU60 | O3 | | **CC61** |
| 176 | P0.15 | I/O0 | A1+/ PU | **Port 0 General Purpose I/O Line 15** |
| | IN15 | I | | **GPTA0 Input 15** |
| | REQ5 | I | | **External Request Input 5** |
| | OUT15 | O1 | | **GPTA0 Output 15** |
| | OUT71 | O2 | | **GPTA0 Output 71** |
| | CCU60 | O3 | | **COUT61** |
| **Port 1** | | | | |
| 116 | P1.0 | I/O0 | A2/ PU | **Port 1 General Purpose I/O Line 0** |
| | REQ15 | I | | **External Request Input 15** |
| | IN16 | I | | **GPTA0 Input 16** |
| | $\overline{\text{BRKIN}}$ | I | | **Break Input** |
| | OUT16 | O1 | | **GPTA0 Output 16** |
| | OUT72 | O2 | | **GPTA0 Output 72** |
| | GPT120 | O3 | | **T3OUT** |
| | $\overline{\text{BRKOUT}}$ | O | | **Break Output (controlled by OCDS module)** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 119 | P1.1 | I/O0 | A1/ PU | **Port 1 General Purpose I/O Line 1** |
| | IN17 | I | | **GPTA0 Input 17** |
| | CCU60 | I | | **T13HRE** |
| | CCU61 | I | | **$\overline{\text{CTRAPB}}$** |
| | OUT17 | O1 | | **GPTA0 Output 17** |
| | OUT73 | O2 | | **GPTA0 Output 73** |
| | Reserved | O3 | | **-** |
| 93 | P1.2 | I/O0 | A1/ PU | **Port 1 General Purpose I/O Line 2** |
| | IN18 | I | | **GPTA0 Input 18** |
| | OUT18 | O1 | | **GPTA0 Output 18** |
| | OUT74 | O2 | | **GPTA0 Output 74** |
| | Reserved | O3 | | **-** |
| 98 | P1.3 | I/O0 | A1/ PU | **Port 1 General Purpose I/O Line 3** |
| | IN19 | I | | **GPTA0 Input 19** |
| | OUT19 | O1 | | **GPTA0 Output 19** |
| | OUT75 | O2 | | **GPTA0 Output 75** |
| | CCU61 | O3 | | **COUT63** |
| 99 | P1.4 | I/O0 | A1/ PU | **Port 1 General Purpose I/O Line 4** |
| | IN20 | I | | **GPTA0 Input 20** |
| | EMGSTOP | I | | **Emergency Stop Input** |
| | OUT20 | O1 | | **GPTA0 Output 20** |
| | OUT76 | O2 | | **GPTA0 Output 76** |
| | CCU61 | O3 | | **COUT61** |
| 108 | P1.5 | I/O0 | A1/ PU | **Port 1 General Purpose I/O Line 35** |
| | IN21 | I | | **GPTA0 Input 21** |
| | OUT21 | O1 | | **GPTA0 Output 21** |
| | OUT77 | O2 | | **GPTA0 Output 77** |
| | Reserved | O3 | | **-** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 109 | P1.6 | I/O0 | A1/ PU | **Port 1 General Purpose I/O Line 6** |
| | IN22 | I | | **GPTA0 Input 22** |
| | OUT22 | O1 | | **GPTA0 Output 22** |
| | OUT78 | O2 | | **GPTA0 Output 78** |
| | Reserved | O3 | | **-** |
| 110 | P1.7 | I/O0 | A1/ PU | **Port 1 General Purpose I/O Line 7** |
| | IN23 | I | | **GPTA0 Input 23** |
| | OUT23 | O1 | | **GPTA0 Output 23** |
| | OUT79 | O2 | | **GPTA0 Output 79** |
| | Reserved | O3 | | **-** |
| 94 | P1.8 | I/O0 | A1+/ PU | **Port 1 General Purpose I/O Line 8** |
| | IN24 | I | | **GPTA0 Input 24** |
| | IN48 | I | | **GPTA0 Input 48** |
| | MTSR1B | I | | **SSC1 Slave Receive Input B (Slave Mode)** |
| | CCU61 | I | | **CCPOS2C** |
| | GPT120 | I | | **T4EUDB** |
| | GPT121 | I | | **T4EUDA** |
| | OUT24 | O1 | | **GPTA0 Output 24** |
| | OUT48 | O2 | | **GPTA0 Output 48** |
| | MTSR1B | O3 | | **SSC1 Master Transmit Output B (Master Mode)** |
| 95 | P1.9 | I/O0 | A1+/ PU | **Port 1 General Purpose I/O Line 9** |
| | IN25 | I | | **GPTA0 Input 25** |
| | IN49 | I | | **GPTA0 Input 49** |
| | MRST1B | I | | **SSC1 Master Receive Input B (Master Mode)** |
| | CCU61 | I | | **CCPOS1C** |
| | GPT120 | I | | **T2EUDB** |
| | GPT121 | I | | **T2EUDA** |
| | OUT25 | O1 | | **GPTA0 Output 25** |
| | OUT49 | O2 | | **GPTA0 Output 49** |
| | MRST1B | O3 | | **SSC1 Slave Transmit Output B (Slave Mode)** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 96 | P1.10 | I/O0 | A1+/ PU | **Port 1 General Purpose I/O Line 10** |
| | IN26 | I | | **GPTA0 Input 26** |
| | IN50 | I | | **GPTA0 Input 50** |
| | OUT26 | O1 | | **GPTA0 Output 26** |
| | OUT50 | O2 | | **GPTA0 Output 50** |
| | SLSO17 | O3 | | **SSC1 Slave Select Output 7** |
| 97 | P1.11 | I/O0 | A1+/ PU | **Port 1 General Purpose I/O Line 11** |
| | IN27 | I | | **GPTA0 Input 27** |
| | IN51 | I | | **GPTA0 Input 51** |
| | SCLK1B | I | | **SSC1 Clock Input B** |
| | CCU61 | I | | **CCPOS0C** |
| | GPT120 | I | | **T2INB** |
| | GPT121 | I | | **T2INA** |
| | OUT27 | O1 | | **GPTA0 Output 27** |
| | OUT51 | O2 | | **GPTA0 Output 51** |
| | SCLK1B | O3 | | **SSC1 Clock Output B** |
| 73 | P1.12 | I/O0 | A1/ PU | **Port 1 General Purpose I/O Line 12** |
| | AD0EMUX0 | O1 | | **ADC0 External Multiplexer Control Output 0** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |
| 72 | P1.13 | I/O0 | A1/ PU | **Port 1 General Purpose I/O Line 13** |
| | AD0EMUX1 | O1 | | **ADC0 External Multiplexer Control Output 1** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |
| 71 | P1.14 | I/O0 | A1/ PU | **Port 1 General Purpose I/O Line 14** |
| | AD0EMUX2 | O1 | | **ADC0 External Multiplexer Control Output 2** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 117 | P1.15 | I/O0 | A2/ PU | **Port 1 General Purpose I/O Line 15** |
| | $\overline{\text{BRKIN}}$ | I | | **Break Input** |
| | Reserved | O1 | | **-** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |
| | $\overline{\text{BRKOUT}}$ | O | | **Break Output (controlled by OCDS module)** |
| **Port 2** | | | | |
| 74 | P2.0 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 0** |
| | IN32 | I | | **GPTA0 Input 32** |
| | CCU60 | I | | **CC62INB** |
| | CCU61 | I | | **CC62INA** |
| | OUT32 | O1 | | **GPTA0 Output 32** |
| | TCLK0 | O2 | | **MLI0 Transmitter Clock Output 0** |
| | CCU61 | O3 | | **CC62** |
| 75 | P2.1 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 1** |
| | IN33 | I | | **GPTA0 Input 33** |
| | TREADY0A | I | | **MLI0 Transmitter Ready Input A** |
| | CCU61 | I | | **CCPOS0A** |
| | CCU60 | I | | **T12HRB** |
| | GPT120 | I | | **T2INA** |
| | GPT121 | I | | **T2INB** |
| | OUT33 | O1 | | **GPTA0 Output 33** |
| | SLSO03 | O2 | | **SSC0 Slave Select Output Line 3** |
| | SLSO13 | O3 | | **SSC1 Slave Select Output Line 3** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 76 | P2.2 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 2** |
| | IN34 | I | | **GPTA0 Input 34** |
| | CCU60 | I | | **CC61INB** |
| | CCU61 | I | | **CC61INA** |
| | OUT34 | O1 | | **GPTA0 Output 34** |
| | TVALID0A | O2 | | **MLI0 Transmitter Valid Output** |
| | CCU61 | O3 | | **CC61** |
| 77 | P2.3 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 3** |
| | IN35 | I | | **GPTA0 Input 35** |
| | CCU60 | I | | **T12HRC** |
| | CCU60 | I | | **T13HRC** |
| | CCU61 | I | | **CCPOS2A** |
| | GPT120 | I | | **T4EUDA** |
| | GPT121 | I | | **T4EUDB** |
| | OUT35 | O1 | | **GPTA0 Output 35** |
| | TDATA0 | O2 | | **MLI0 Transmitter Data Output** |
| | Reserved | O3 | | **-** |
| 78 | P2.4 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 4** |
| | IN36 | I | | **GPTA0 Input 36** |
| | RCLK0A | I | | **MLI Receiver Clock Input A** |
| | OUT36 | O1 | | **GPTA0 Output 36** |
| | CCU61 | O2 | | **COUT63** |
| | Reserved | O3 | | **-** |
| 79 | P2.5 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 5** |
| | IN37 | I | | **GPTA0 Input 37** |
| | CCU60 | I | | **CC60INB** |
| | CCU61 | I | | **CC60INA** |
| | OUT37 | O1 | | **GPTA0 Output 37** |
| | RREADY0A | O2 | | **MLI0 Receiver Ready Output A** |
| | CCU61 | O3 | | **CC60** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 80 | P2.6 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 6** |
| | IN38 | I | | **GPTA0 Input 38** |
| | RVALID0A | I | | **MLI Receiver Valid Input A** |
| | OUT38 | O1 | | **GPTA0 Output 38** |
| | CCU61 | O2 | | **COUT62** |
| | Reserved | O3 | | **-** |
| 81 | P2.7 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 7** |
| | RDATA0A | I | | **MLI Receiver Data Input A** |
| | IN39 | I | | **GPTA0 Input 39** |
| | OUT39 | O1 | | **GPTA0 Output 39** |
| | CCU61 | O2 | | **COUT60** |
| | Reserved | O3 | | **-** |
| 164 | P2.8 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 8** |
| | SLSO04 | O1 | | **SSC0 Slave Select Output 4** |
| | SLSO14 | O2 | | **SSC1 Slave Select Output 4** |
| | EN00 | O3 | | **MSC0 Enable Output 0** |
| 160 | P2.9 | I/O0 | A2/ PU | **Port 2 General Purpose I/O Line 9** |
| | SLSO05 | O1 | | **SSC0 Slave Select Output 5** |
| | SLSO15 | O2 | | **SSC1 Slave Select Output 5** |
| | EN01 | O3 | | **MSC0 Enable Output 1** |
| 161 | P2.10 | I/O0 | A1+/ PU | **Port 2 General Purpose I/O Line 10** |
| | MRST1A | I | | **SSC1 Master Receive Input A** |
| | MRST1A | O1 | | **SSC1 Slave Transmit Output** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |
| 162 | P2.11 | I/O0 | A1+/ PU | **Port 2 General Purpose I/O Line 11** |
| | SCLK1A | I | | **SSC1 Clock Input A** |
| | SCLK1A | O1 | | **SSC1 Clock Output A** |
| | Reserved | O2 | | **-** |
| | FCLP0B | O3 | | **MSC0 Clock Output Positive B** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 163 | P2.12 | I/O0 | A1+/ PU | **Port 2 General Purpose I/O Line 12** |
| | MTSR1A | I | | **SSC1 Slave Receive Input A** |
| | MTSR1A | O1 | | **SSC1 Master Transmit Output A** |
| | Reserved | O2 | | **-** |
| | SOP0B | O3 | | **MSC0 Serial Data Output Positive B** |
| 165 | P2.13 | I/O0 | A1+/ PU | **Port 2 General Purpose I/O Line 13** |
| | SLSI11 | I | | **SSC1 Slave Select Input 1** |
| | SDI0 | I | | **MSC0 Serial Data Input 0** |
| | CCU60 | I | | **CTRAPA** |
| | CCU61 | I | | **T12HRE** |
| | Reserved | O1 | | **-** |
| | SLSO16 | O2 | | **SSC1 Slave Select Output 6** |
| | GPT120 | O3 | | **T6OUT** |
| **Port 3** | | | | |
| 136 | P3.0 | I/O0 | A1+/ PU | **Port 3 General Purpose I/O Line 0** |
| | RXD0A | I | | **ASC0 Receiver Input A (Async. & Sync. Mode)** |
| | REQ6 | I | | **External Request Input 6** |
| | RXD0A | O1 | | **ASC0 Output (Sync. Mode)** |
| | Reserved | O2 | | **-** |
| | OUT84 | O3 | | **GPTA0 Output 84** |
| 135 | P3.1 | I/O0 | A1+/ PU | **Port 3 General Purpose I/O Line 1** |
| | TXD0 | O1 | | **ASC0 Output** |
| | Reserved | O2 | | **-** |
| | OUT85 | O3 | | **GPTA0 Output 85** |
| 129 | P3.2 | I/O0 | A1+/ PU | **Port 3 General Purpose I/O Line 2** |
| | SCLK0 | I | | **SSC0 Clock Input (Slave Mode)** |
| | SCLK0 | O1 | | **SSC0 Clock Output (Master Mode)** |
| | Reserved | O2 | | **-** |
| | OUT86 | O3 | | **GPTA0 Output 86** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 130 | P3.3 | I/O0 | A1+/ PU | **Port 3 General Purpose I/O Line 3** |
| | MRST0 | I | | **SSC0 Master Receive Input (Master Mode)** |
| | MRST0 | O1 | | **SSC0 Slave Transmit Output (Slave Mode)** |
| | Reserved | O2 | | **-** |
| | OUT87 | O3 | | **GPTA0 Output 87** |
| 132 | P3.4 | I/O0 | A2/ PU | **Port 3 General Purpose I/O Line 4** |
| | MTSR0 | I | | **SSC0 Slave Receive Input (Slave Mode)** |
| | MTSR0 | O1 | | **SSC0 Master Transmit Output (Master Mode)** |
| | Reserved | O2 | | **-** |
| | OUT88 | O3 | | **GPTA0 Output 88** |
| 126 | P3.5 | I/O0 | A1+/ PU | **Port 3 General Purpose I/O Line 5** |
| | SLSO00 | O1 | | **SSC0 Slave Select Output 0** |
| | SLSO10 | O2 | | **SSC1 Slave Select Output 0** |
| | SLSOANDO0 | O3 | | **SSC0 AND SSC1 Slave Select Output 0** |
| 127 | P3.6 | I/O0 | A1+/ PU | **Port 3 General Purpose I/O Line 6** |
| | SLSO01 | O1 | | **SSC0 Slave Select Output 1** |
| | SLSO11 | O2 | | **SSC1 Slave Select Output 1** |
| | SLSOANDO1 | O3 | | **SSC0 AND SSC1 Slave Select Output 1** |
| 131 | P3.7 | I/O0 | A2/ PU | **Port 3 General Purpose I/O Line 7** |
| | SLSI0 | I | | **SSC0 Slave Select Input 1** |
| | SLSO02 | O1 | | **SSC0 Slave Select Output 2** |
| | SLSO12 | O2 | | **SSC1 Slave Select Output 2** |
| | OUT89 | O3 | | **GPTA0 Output 89** |
| 128 | P3.8 | I/O0 | A2/ PU | **Port 3 General Purpose I/O Line 8** |
| | REQ14 | I | | **External Request Input 14** |
| | SLSO06 | O1 | | **SSC0 Slave Select Output 6** |
| | TXD1 | O2 | | **ASC1 Transmit Output** |
| | OUT90 | O3 | | **GPTA0 Output 90** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 138 | P3.9 | I/O0 | A1/ PU | **Port 3 General Purpose I/O Line 9** |
| | RXD1A | I | | **ASC1 Receiver Input A** |
| | RXD1A | O1 | | **ASC1 Receiver Output A (Synchronous Mode)** |
| | Reserved | O2 | | **-** |
| | OUT91 | O3 | | **GPTA0 Output 91** |
| 137 | P3.10 | I/O0 | A1/ PU | **Port 3 General Purpose I/O Line 10** |
| | REQ0 | I | | **External Request Input 0** |
| | Reserved | O1 | | **-** |
| | Reserved | O2 | | **-** |
| | OUT92 | O3 | | **GPTA0 Output 92** |
| 144 | P3.11 | I/O0 | A1/ PU | **Port 3 General Purpose I/O Line 11** |
| | REQ1 | I | | **External Request Input 1** |
| | Reserved | O1 | | **-** |
| | Reserved | O2 | | **-** |
| | OUT93 | O3 | | **GPTA0 Output 93** |
| 143 | P3.12 | I/O0 | A1/ PU | **Port 3 General Purpose I/O Line 12** |
| | RXDCAN0 | I | | **CAN Node 0 Receiver Input** |
| | RXD0B | I | | **ASC0 Receiver Input B** |
| | RXD0B | O1 | | **ASC0 Receiver Output B (Synchronous Mode)** |
| | Reserved | O2 | | **-** |
| | OUT94 | O3 | | **GPTA0 Output 94** |
| 142 | P3.13 | I/O0 | A2/ PU | **Port 3 General Purpose I/O Line 13** |
| | TXDCAN0 | O1 | | **CAN Node 0 Transmitter Output** |
| | TXD0 | O2 | | **ASC0 Transmit Output** |
| | OUT95 | O3 | | **GPTA0 Output 95** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 134 | P3.14 | I/O0 | A1/ PU | **Port 3 General Purpose I/O Line 14** |
| | RXDCAN1 | I | | **CAN Node 1 Receiver Input** |
| | RXD1B | I | | **ASC1 Receiver Input B** |
| | SDI2 | I | | **MSC0 Serial Data Input 2** |
| | RXD1B | O1 | | **ASC1 Receiver Output B (Synchronous Mode)** |
| | Reserved | O2 | | **-** |
| | OUT96 | O3 | | **GPTA0 Output 96** |
| 133 | P3.15 | I/O0 | A2/ PU | **Port 3 General Purpose I/O Line 15** |
| | TXDCAN1 | O1 | | **CAN Node 1 Transmitter Output** |
| | TXD1 | O2 | | **ASC1 Transmit Output** |
| | OUT97 | O3 | | **GPTA0 Output 97** |
| **Port 4** | | | | |
| 86 | P4.0 | I/O0 | A1+/ PU | **Port 4 General Purpose I/O Line 0** |
| | IN28 | I | | **GPTA0 Input 28** |
| | IN52 | I | | **GPTA0 Input 52** |
| | RXDCAN2 | I | | **CAN Node 2 Receiver Input** |
| | OUT28 | O1 | | **GPTA0 Output 28** |
| | OUT52 | O2 | | **GPTA0 Output 52** |
| | Reserved | O3 | | **-** |
| 87 | P4.1 | I/O0 | A1+/ PU | **Port 4 General Purpose I/O Line 1** |
| | IN29 | I | | **GPTA0 Input 29** |
| | IN53 | I | | **GPTA0 Input 53** |
| | OUT29 | O1 | | **GPTA0 Output 29** |
| | OUT53 | O2 | | **GPTA0 Output 53** |
| | TXDCAN2 | O3 | | **CAN Node 2 Transmitter Output** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 88 | P4.2 | I/O0 | A2/ PU | **Port 4 General Purpose I/O Line 2** |
| | IN30 | I | | **GPTA0 Input 30** |
| | IN54 | I | | **GPTA0 Input 54** |
| | CCU60 | I | | **T13HRB** |
| | CCU61 | I | | **CCPOS1A** |
| | GPT120 | I | | **T2EUDA** |
| | GPT121 | I | | **T2EUDB** |
| | OUT30 | O1 | | **GPTA0 Output 30** |
| | OUT54 | O2 | | **GPTA0 Output 54** |
| | EXTCLK1 | O3 | | **External Clock 1 Output** |
| 90 | P4.3 | I/O0 | A2/ PU | **Port 4 General Purpose I/O Line 3** |
| | IN31 | I | | **GPTA0 Input 31** |
| | IN55 | I | | **GPTA0 Input 55** |
| | CCU60 | I | | **T12HRE** |
| | CCU61 | I | | **$\overline{\text{CTRAPA}}$** |
| | OUT31 | O1 | | **GPTA0 Output 31** |
| | OUT55 | O2 | | **GPTA0 Output 55** |
| | EXTCLK0 | O3 | | **External Clock 0 Output** |
| **Port 5** | | | | |
| 1 | P5.0 | I/O0 | A1+/ PU | **Port 5 General Purpose I/O Line 0** |
| | REQ7 | I | | **External Request Input 7** |
| | IN40 | I | | **GPTA0 Input 40** |
| | CCU60 | I | | **CC62INA** |
| | CCU61 | I | | **CC62INB** |
| | GPT120 | I | | **CAPINB** |
| | GPT121 | I | | **CAPINA** |
| | OUT40 | O1 | | **GPTA0 Output 40** |
| | CCU60 | O2 | | **CC62** |
| | SLSO20 | O3 | | **SSC2 Slave Select Output 0** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 2 | P5.1 | I/O0 | A1+/ PU | **Port 5 General Purpose I/O Line 1** |
| | IN41 | I | | **GPTA0 Input 41** |
| | OUT41 | O1 | | **GPTA0 Output 41** |
| | Reserved | O2 | | **-** |
| | SLSO21 | O3 | | **SSC2 Slave Select Output 1** |
| 3 | P5.2 | I/O0 | A1+/ PU | **Port 5 General Purpose I/O Line 2** |
| | IN42 | I | | **GPTA0 Input 42** |
| | OUT42 | O1 | | **GPTA0 Output 42** |
| | CCU60 | O2 | | **COUT62** |
| | SLSO22 | O3 | | **SSC2 Slave Select Output 2** |
| 4 | P5.3 | I/O0 | A1+/ PU | **Port 5 General Purpose I/O Line 3** |
| | IN43 | I | | **GPTA0 Input 43** |
| | OUT43 | O1 | | **GPTA0 Output 43** |
| | Reserved | O2 | | **-** |
| | SLSO23 | O3 | | **SSC2 Slave Select Output 3** |
| 5 | P5.4 | I/O0 | A1+/ PU | **Port 5 General Purpose I/O Line 4** |
| | IN44 | I | | **GPTA0 Input 44** |
| | SLSI2A | I | | **SSC2 Slave Select Input A** |
| | OUT44 | O1 | | **GPTA0 Output 44** |
| | Reserved | O2 | | **-** |
| | SLSO24 | O3 | | **SSC2 Slave Select Output 4** |
| 6 | P5.5 | I/O0 | A1+/ PU | **Port 5 General Purpose I/O Line 5** |
| | IN45 | I | | **GPTA0 Input 45** |
| | MRST2A | I | | **SSC2 Master Receive Input A (Master Mode)** |
| | OUT45 | O1 | | **GPTA0 Output 45** |
| | Reserved | O2 | | **-** |
| | MRST2 | O3 | | **SSC2 Slave Transmit Output (Slave Mode)** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 7 | P5.6 | I/O0 | A1+/ PU | **Port 5 General Purpose I/O Line 6** |
| | IN46 | I | | **GPTA0 Input 46** |
| | MTSR2A | I | | **SSC2 Slave Receive Input (Slave Mode)** |
| | OUT46 | O1 | | **GPTA0 Output 46** |
| | Reserved | O2 | | **-** |
| | MTSR2 | O3 | | **SSC2 Master Transmit Output (Master Mode)** |
| 8 | P5.7 | I/O0 | A1+/ PU | **Port 5 General Purpose I/O Line 7** |
| | IN47 | I | | **GPTA0 Input 47** |
| | SCLK2A | I | | **SSC2 Clock Input A (Slave Mode)** |
| | OUT47 | O1 | | **GPTA0 Output 47** |
| | Reserved | O2 | | **-** |
| | SCLK2 | O3 | | **SSC2 Clock Output (Master Mode)** |
| 13 | P5.8 | I/O0 | A2/ PU | **Port 5 General Purpose I/O Line 8** |
| | CCU60 | I | | **CC61INA** |
| | CCU61 | I | | **CC61INB** |
| | OUT6 | O1 | | **GPTA0 Output 6** |
| | TXDA1 | O2 | | **E-Ray Channel A transmit Data Output[1)]** |
| | CCU60 | O3 | | **CC61** |
| 14 | P5.9 | I/O0 | A2/ PU | **Port 5 General Purpose I/O Line 9** |
| | RXDCAN0 | I | | **CAN Node 0 Receiver Input** |
| | OUT7 | O1 | | **GPTA0 Output 7** |
| | TXDB1 | O2 | | **E-Ray Channel B transmit Data Output[1)]** |
| | Reserved | O3 | | **-** |
| 15 | P5.10 | I/O0 | A2/ PU | **Port 5 General Purpose I/O Line 10** |
| | OUT8 | O1 | | **GPTA0 Output 8** |
| | TXENA | O2 | | **E-Ray Channel A transmit Data Output enable[1)]** |
| | CCU60 | O3 | | **COUT61** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 16 | P5.11 | I/O0 | A2/ PU | **Port 5 General Purpose I/O Line 11** |
| | OUT9 | O1 | | **GPTA0 Output 9** |
| | TXENB | O2 | | **E-Ray Channel B transmit Data Output enable**[1)] |
| | CCU60 | O3 | | **COUT63** |
| 17 | P5.12 | I/O0 | A1+/ PU | **Port 5 General Purpose I/O Line 12** |
| | CCU60 | I | | **CCPOS0A** |
| | CCU61 | I | | **T12HRB** |
| | GPT120 | I | | **T3INA** |
| | GPT121 | I | | **T3INB** |
| | OUT19 | O1 | | **GPTA0 Output 19** |
| | SLSO07 | O2 | | **SSC0 Slave Select Output 7** |
| | AD1EMUX0 | O3 | | **ADC1 External Multiplexer Control Output 0** |
| 18 | P5.13 | I/O0 | A1+/ PU | **Port 5 General Purpose I/O Line 13** |
| | CCU60 | I | | **CCPOS1A** |
| | CCU61 | I | | **T13HRB** |
| | GPT120 | I | | **T3EUDA** |
| | GPT121 | I | | **T3EUDB** |
| | OUT20 | O1 | | **GPTA0 Output 20** |
| | Reserved | O2 | | **-** |
| | AD1EMUX1 | O3 | | **ADC1 External Multiplexer Control Output 1** |
| 19 | P5.14 | I/O0 | A1+/ PU | **Port 5 General Purpose I/O Line 14** |
| | RXDA1 | I | | **E-Ray Channel A Receive Data Input 1**[1)] |
| | CCU60 | I | | **CCPOS2A** |
| | CCU61 | I | | **T12HRC** |
| | CCU61 | I | | **T13HRC** |
| | GPT120 | I | | **T4INA** |
| | GPT121 | I | | **T4INB** |
| | OUT36 | O1 | | **GPTA0 Output 36** |
| | Reserved | O2 | | **-** |
| | AD1EMUX2 | O3 | | **ADC1 External Multiplexer Control Output 2** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 9 | P5.15 | I/O0 | A1+/ PU | **Port 5 General Purpose I/O Line 15** |
| | RXDB1 | I | | **E-Ray Channel B Receive Data Input 1[1)]** |
| | OUT37 | O1 | | **GPTA0 Output 37** |
| | Reserved | O2 | | **-** |
| | TXDCAN0 | O3 | | **CAN Node 0 Transmitter Output** |
| **Port 6** | | | | |
| 156 | P6.0 | I/O0 | F/ PU | **Port 6 General Purpose I/O Line 0** |
| | FCLN0 | O1 | | **MSC0 Clock Output Negative** |
| | OUT80 | O2 | | **GPTA0 Output 80** |
| | Reserved | O3 | | **-** |
| 157 | P6.1 | I/O0 | F/ PU | **Port 6 General Purpose I/O Line 1** |
| | FCLP0A | O1 | | **MSC0 Clock Output Positive A** |
| | OUT81 | O2 | | **GPTA0 Output 81** |
| | Reserved | O3 | | **-** |
| 158 | P6.2 | I/O0 | F/ PU | **Port 6 General Purpose I/O Line 2** |
| | SON0 | O1 | | **MSC0 Serial Data Output Negative** |
| | OUT82 | O2 | | **GPTA0 Output 82** |
| | Reserved | O3 | | **-** |
| 159 | P6.3 | I/O0 | F/ PU | **Port 6 General Purpose I/O Line 3** |
| | SOP0A | O1 | | **MSC0 Serial Data Output Positive A** |
| | OUT83 | O2 | | **GPTA0 Output 83** |
| | Reserved | O3 | | **-** |
| **Port 8** | | | | |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 141 | P8.0 | I/O0 | A2/ PU | **Port 8 General Purpose I/O Line 0** |
| | SCLK3 | I | | **SSC3 Clock Input (Slave Mode)** |
| | CCU60 | I | | **CCPOS0C** |
| | GPT120 | I | | **T3INB** |
| | GPT121 | I | | **T3INA** |
| | Reserved | O1 | | **-** |
| | OUT48 | O2 | | **GPTA0 Output 48** |
| | SCLK3 | O3 | | **SSC3 Clock Output (Master Mode)** |
| 140 | P8.1 | I/O0 | A2/ PU | **Port 8 General Purpose I/O Line 1** |
| | MRST3 | I | | **SSC3 Master Receive Input (Master Mode)** |
| | CCU60 | I | | **CCPOS1C** |
| | GPT120 | I | | **T3EUDB** |
| | GPT121 | I | | **T3EUDA** |
| | Reserved | O1 | | **-** |
| | OUT49 | O2 | | **GPTA0 Output 49** |
| | MRST3 | O3 | | **SSC3 Slave Transmit Output (Slave Mode)** |
| 139 | P8.2 | I/O0 | A2/ PU | **Port 8 General Purpose I/O Line 2** |
| | MTSR3 | I | | **SSC3 Slave Receive Input (Slave Mode)** |
| | CCU60 | I | | **CCPOS2C** |
| | GPT120 | I | | **T4INB** |
| | GPT121 | I | | **T4INA** |
| | Reserved | O1 | | **-** |
| | OUT50 | O2 | | **GPTA0 Output 50** |
| | MTSR3 | O3 | | **SSC3 Master Transmit Output (Master Mode)** |
| 124 | P8.3 | I/O0 | A2/ PU | **Port 8 General Purpose I/O Line 3** |
| | SLSI3 | I | | **SSC3 Slave Select Input B** |
| | CCU60 | I | | **CC61INC** |
| | CCU61 | O1 | | **CC61** |
| | OUT51 | O2 | | **GPTA0 Output 51** |
| | SLSO30 | O3 | | **SSC3 Slave Select Output 0** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 123 | P8.4 | I/O0 | A2/ PU | **Port 8 General Purpose I/O Line 4** |
| | OUT99 | O1 | | **GPTA0 Output 99** |
| | CCU61 | O2 | | **COUT62** |
| | SLSO31 | O3 | | **SSC3 Slave Select Output 1** |
| 82 | P8.5 | I/O0 | A2/ PU | **Port 8 General Purpose I/O Line 5** |
| | CCU60 | I | | **CC60INC** |
| | OUT100 | O1 | | **GPTA0 Output 100** |
| | CCU61 | O2 | | **CC60** |
| | SLSO32 | O3 | | **SSC3 Slave Select Output 2** |
| 83 | P8.6 | I/O0 | A2/ PU | **Port 8 General Purpose I/O Line 6** |
| | OUT101 | O1 | | **GPTA0 Output 101** |
| | Reserved | O2 | | **-** |
| | CCU61 | O3 | | **COUT61** |
| 84 | P8.7 | I/O0 | A2/ PU | **Port 8 General Purpose I/O Line 7** |
| | CCU60 | I | | **CC62INC** |
| | OUT102 | O1 | | **GPTA0 Output 102** |
| | Reserved | O2 | | **-** |
| | CCU61 | O3 | | **CC62** |
| 85 | P8.8 | I/O0 | A2/ PU | **Port 8 General Purpose I/O Line 8** |
| | Reserved | O1 | | **-** |
| | OUT56 | O2 | | **GPTA0 Output 56** |
| | SLSO33 | O3 | | **SSC3 Slave Select Output 3** |
| 89 | P8.9 | I/O0 | A2/ PU | **Port 8 General Purpose I/O Line 9** |
| | Reserved | O1 | | **-** |
| | OUT57 | O2 | | **GPTA0 Output 57** |
| | SLSO34 | O3 | | **SSC3 Slave Select Output 4** |
| 91 | P8.10 | I/O0 | A2/ PU | **Port 8 General Purpose I/O Line 10** |
| | OUT105 | O1 | | **GPTA0 Output 105** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 92 | P8.11 | I/O0 | A2/ PU | **Port 8 General Purpose I/O Line 11** |
| | OUT106 | O1 | | **GPTA0 Output 106** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |
| 100 | P8.12 | I/O0 | A2/ PU | **Port 8 General Purpose I/O Line 12** |
| | OUT107 | O1 | | **GPTA0 Output 107** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |
| 125 | P8.13 | I/O0 | A2/ PU | **Port 8 General Purpose I/O Line 13** |
| | OUT4 | O1 | | **GPTA0 Output 4** |
| | Reserved | O2 | | **-** |
| | CCU61 | O3 | | **COUT60** |
| **Port 9** | | | | |
| 172 | P9.2 | I/O0 | A1/ PU | **Port 9 General Purpose I/O Line 2** |
| | Reserved | O1 | | **-** |
| | OUT82 | O2 | | **GPTA0 Output 82** |
| | CCU60 | O3 | | **COUT63** |
| 171 | P9.3 | I/O0 | A1/ PU | **Port 9 General Purpose I/O Line 3** |
| | Reserved | O1 | | **-** |
| | OUT83 | O2 | | **GPTA0 Output 83** |
| | CCU60 | O3 | | **COUT62** |
| 170 | P9.4 | I/O0 | A1/ PU | **Port 9 General Purpose I/O Line 4** |
| | CCU61 | I | | **CC62INC** |
| | Reserved | O1 | | **-** |
| | OUT84 | O2 | | **GPTA0 Output 84** |
| | CCU60 | O3 | | **CC62** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 111 | P9.5 | I/O0 | A2/ PU | **Port 9 General Purpose I/O Line 5** |
| | TDI | I | | **JTAG Serial Data Input** |
| | $\overline{\text{BRKIN}}$ | I | | **OCDS Break Input** |
| | Reserved | O1 | | **-** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |
| | $\overline{\text{BRKOUT}}$ | O | | **OCDS Break Output (controlled by OCDS module)** |
| 113 | P9.6 | I/O0 | A2/ PU | **Port 9 General Purpose I/O Line 6** |
| | TDO | I | | **JTAG Serial Data Output** |
| | $\overline{\text{BRKIN}}$ | I | | **OCDS Break Input** |
| | Reserved | O1 | | **-** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |
| | BRKOUT | O | | **OCDS Break Output (controlled by OCDS module)** |
| | TDO | O | | **JTAG Serial Data Output (controlled by OCDS module)** |
| 11 | P9.7 | I/O0 | A1/ PU | **Port 9 General Purpose I/O Line 7** |
| | CCU61 | I | | **CC60INC** |
| | Reserved | O1 | | **-** |
| | OUT87 | O2 | | **GPTA0 Output 87** |
| | CCU60 | O3 | | **CC60** |
| 12 | P9.8 | I/O0 | A1/ PU | **Port 9 General Purpose I/O Line 7** |
| | Reserved | O1 | | **-** |
| | OUT88 | O2 | | **GPTA0 Output 88** |
| | CCU60 | O3 | | **COUT60** |
| **Port 10** | | | | |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 23 | P10.0 | I/O0 | A2/ PU | **Port 10 General Purpose I/O Line 0** |
| | MRST2B | I | | **SSC2 Master Receive Input B (Master Mode)** |
| | MRST2 | O1 | | **SSC2 Slave Transmit Output (Slave Mode)** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |
| 24 | P10.1 | I/O0 | A2/ PU | **Port 10 General Purpose I/O Line 1** |
| | MTSR2B | I | | **SSC2 Slave Receive Input B (Slave Mode)** |
| | MTSR2 | O1 | | **SSC2 Master Transmit Output (Master Mode)** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |
| 25 | P10.2 | I/O0 | A2/ PU | **Port 10 General Purpose I/O Line 2** |
| | SCLK2B | I | | **SSC2 Clock Input B (Slave Mode)** |
| | SCLK2 | O1 | | **SSC2 Clock Output (Master Mode)** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |
| 26 | P10.3 | I/O0 | A2/ PU | **Port 10 General Purpose I/O Line 3** |
| | SLSI2B | I | | **SSC2 Slave Select Input B** |
| | SLSO20 | O1 | | **SSC2 Slave Select Output 0** |
| | Reserved | O2 | | **-** |
| | Reserved | O3 | | **-** |
| **Port 11** | | | | |
| 48 | P11.0 | I | D / S | **Port 11 General Purpose I/O Line 0**[2] |
| | Dig0 | I | | **Digital Input 0** |
| | AN16 | I | | **Analog Input : ADC1.CH0** [3] |
| 47 | P11.1 | I | D / S | **Port 11 General Purpose I/O Line 1**[2] |
| | Dig1 | I | | **Digital Input 1** |
| | AN17 | I | | **Analog Input : ADC1.CH1** [3] |
| 46 | P11.2 | I | D / S | **Port 11 General Purpose I/O Line 2**[2] |
| | Dig2 | I | | **Digital Input 2** |
| | AN18 | I | | **Analog Input : ADC1.CH2** [3] |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 45 | P11.3 | I | D / S | **Port 11 General Purpose I/O Line 3**[2] |
| | Dig3 | I | | **Digital Input 3** |
| | AN19 | I | | **Analog Input : ADC1.CH3** [3] |
| 44 | P11.4 | I | D / S | **Port 11 General Purpose I/O Line 4**[2] |
| | Dig4 | I | | **Digital Input 4** |
| | AN20 | I | | **Analog Input : ADC1.CH4** [3] |
| 43 | P11.5 | I | D / S | **Port 11 General Purpose I/O Line 5**[2] |
| | Dig5 | I | | **Digital Input 5** |
| | AN21 | I | | **Analog Input : ADC1.CH5** [3] |
| 42 | P11.6 | I | D / S | **Port 11 General Purpose I/O Line 6**[2] |
| | Dig6 | I | | **Digital Input 6** |
| | AN22 | I | | **Analog Input : ADC1.CH6** [3] |
| 41 | P11.7 | I | D / S | **Port 11 General Purpose I/O Line 7**[2] |
| | Dig7 | I | | **Digital Input 7** |
| | AN23 | I | | **Analog Input : ADC1.CH7** [3] |
| 40 | P11.8 | I | D / S | **Port 11 General Purpose I/O Line 8**[2] |
| | Dig8 | I | | **Digital Input 8** |
| | AN24 | I | | **Analog Input : ADC1.CH8** [3] |
| 39 | P11.9 | I | D / S | **Port 11 General Purpose I/O Line 9**[2] |
| | Dig9 | I | | **Digital Input 9** |
| | AN25 | I | | **Analog Input : ADC1.CH9** [3] |
| 38 | P11.10 | I | D / S | **Port 11 General Purpose I/O Line 10**[2] |
| | Dig10 | I | | **Digital Input 10** |
| | AN26 | I | | **Analog Input : ADC1.CH10** [3] |
| 37 | P11.11 | I | D / S | **Port 11 General Purpose I/O Line 11**[2] |
| | Dig11 | I | | **Digital Input 11** |
| | AN27 | I | | **Analog Input : ADC1.CH11** [3] |
| 35 | P11.12 | I | D / S | **Port 11 General Purpose I/O Line 12**[2] |
| | Dig12 | I | | **Digital Input 12** |
| | AN28 | I | | **Analog Input : ADC1.CH12** [3] |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 34 | P11.13 | I | D / S | **Port 11 General Purpose I/O Line 13**[2] |
| | Dig13 | I | | **Digital Input 13** |
| | AN29 | I | | **Analog Input : ADC1.CH13** [3] |
| 33 | P11.14 | I | D / S | **Port 11 General Purpose I/O Line 14**[2] |
| | Dig14 | I | | **Digital Input 14** |
| | AN30 | I | | **Analog Input : ADC1.CH14** [3] |
| 32 | P11.15 | I | D / S | **Port 11 General Purpose I/O Line 15**[2] |
| | Dig15 | I | | **Digital Input 15** |
| | AN31 | I | | **Analog Input : ADC1.CH15** [3] |
| **Analog Input Port** | | | | |
| 67 | AN0 | I | D | **Analog Input 0: ADC0.CH0** [3] |
| 66 | AN1 | I | D | **Analog Input 1: ADC0.CH1** [3] |
| 65 | AN2 | I | D | **Analog Input 2: ADC0.CH2** [3] |
| 64 | AN3 | I | D | **Analog Input 3: ADC0.CH3** [3] |
| 63 | AN4 | I | D | **Analog Input 4: ADC0.CH4** [3] |
| 62 | AN5 | I | D | **Analog Input 5: ADC0.CH5** [3] |
| 61 | AN6 | I | D | **Analog Input 6: ADC0.CH6** [3] |
| 36 | AN7 | I | D | **Analog Input 7: ADC0.CH7** [3] |
| 60 | AN8 | I | D | **Analog Input 8: ADC0.CH8** [3] |
| 59 | AN9 | I | D | **Analog Input 9: ADC0.CH9** [3] |
| 58 | AN10 | I | D | **Analog Input 10: ADC0.CH10** [3] |
| 57 | AN11 | I | D | **Analog Input 11: ADC0.CH11** [3] |
| 56 | AN12 | I | D | **Analog Input 12: ADC0.CH12** [3] |
| 55 | AN13 | I | D | **Analog Input 13: ADC0.CH13** [3] |
| 50 | AN14 | I | D | **Analog Input 14: ADC0.CH14** [3] |
| 49 | AN15 | I | D | **Analog Input 15: ADC0.CH15** [3] |
| 48 | AN16 | I | D / S | **Analog Input 16: ADC1.CH0, Dig0** [3] |
| 47 | AN17 | I | D / S | **Analog Input 17: ADC1.CH1, Dig1** [3] |
| 46 | AN18 | I | D / S | **Analog Input 18: ADC1.CH2, Dig2** [3] |
| 45 | AN19 | I | D / S | **Analog Input 19: ADC1.CH3, Dig3** [3] |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 44 | AN20 | I | D / S | **Analog Input 20: ADC1.CH4, Dig4** [3] |
| 43 | AN21 | I | D / S | **Analog Input 21: ADC1.CH5, Dig5** [3] |
| 42 | AN22 | I | D / S | **Analog Input 22: ADC1.CH6, Dig6** [3] |
| 41 | AN23 | I | D / S | **Analog Input 23: ADC1.CH7, Dig7** [3] |
| 40 | AN24 | I | D / S | **Analog Input 24: ADC1.CH8, Dig8** [3] |
| 39 | AN25 | I | D / S | **Analog Input 25: ADC1.CH9, Dig9** [3] |
| 38 | AN26 | I | D / S | **Analog Input 26: ADC1.CH10, Dig10** [3] |
| 37 | AN27 | I | D / S | **Analog Input 27: ADC1.CH11, Dig11** [3] |
| 35 | AN28 | I | D / S | **Analog Input 28: ADC1.CH12, Dig12** [3] |
| 34 | AN29 | I | D / S | **Analog Input 29: ADC1.CH13, Dig13** [3] |
| 33 | AN30 | I | D / S | **Analog Input 30: ADC1.CH14, Dig14** [3] |
| 32 | AN31 | I | D / S | **Analog Input 31: ADC1.CH15, Dig15** [3] |
| 31 | AN32 | I | D | **Analog Input 32: FADC_FADIN0P** [4] |
| 30 | AN33 | I | D | **Analog Input 33: FADC_FADIN0N** [4] |
| 29 | AN34 | I | D | **Analog Input 34: FADC_FADIN1P** [4] |
| 28 | AN35 | I | D | **Analog Input 35: FADC_FADIN1N** [4] |
| 54 | $V_{DDM}$ | - | - | **ADC Analog Part Power Supply (3.3V - 5V)** |
| 53 | $V_{SSM}$ | - | - | **ADC Analog Part Ground** |
| 52 | $V_{AREF0}$ | - | - | **ADC0 and ADC1 Reference Voltage** |
| 51 | $V_{AGND0}$ | - | - | **ADC Reference Ground** |
| 10, 21[5], 68, 105, 153 | $V_{DD}$ | - | - | **Digital Core Power Supply (1.3V)** |
| 20, 69, 106, 154 | $V_{DDP}$ | - | - | **Port Power Supply (3.3V)** |

**Table 3-1 Pin Definitions and Functions (**PG-LQFP-176-6 **Package**) (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 22, 70, 107, 155 | $V_5$ | - | - | **EVR Power Supply (5V)** |
| 27 | $V_{PDG}$ | - | - | **EVR Pass Device Gate**<br>If this pin is connected to ground, the internal pass devices are used and the external pass device bypassed. |
| 101, 104 | $V_{SS}$ | - | - | **Digital Ground** |
| 102 | XTAL1 | I | | **Main Oscillator Input** |
| 103 | XTAL2 | O | | **Main Oscillator Output** |
| 112 | TMS | I | A2/ PD | **JTAG State Machine Control Input** |
| | DAP1 | I/O | | **Device Access Port Line 1** |
| 114 | TRST | I | A1/ PD | **JTAG Reset Input** |
| 115 | TCK | I | A1/ PD | **JTAG Clock Input** |
| | DAP0 | I | | **Device Access Port Line 0** |
| 118 | TESTMODE | I | I/PU | **Test Mode Select Input** |
| 120 | ESR1 | I/O | A2/ PD | **External System Request Reset Input 1** |
| 121 | PORST | I | I/PU | **Power On Reset** |
| 122 | ESR0 | I/O | A2 | **External System Request Reset Input 0**<br>Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. |

1) Only applicable for SAK-TC1728F-192F133HR.

2) Analog input overlayed with digital input functionality. The related port logic is used to configure the input as either analog input (default after reset) or digital input. The related port logic supports only the port input features as the connected pads are input only pads.

3) IOZ1 valid for this pin is the parameter with overlayed = No in the ADC parameter table.

4) IOZ1 valid for this pin is the parameter with overlayed = Yes in the ADC parameter table.

5) For the emulation device (ED), this pin is bonded to $VDD_{SB}$ (ED Stand By RAM supply). In the production devide device, this pin is bonded to a VDD pad.

**Legend for Table 3-1**

Column “**Ctrl.**”:

I = Input (for GPIO port lines with IOCR bit field selection PCx = $0XXX_B$)

O = Output
O0 = Output with IOCR bit field selection PCx = $1X00_B$
O1 = Output with IOCR bit field selection PCx = $1X01_B$ (ALT1)
O2 = Output with IOCR bit field selection PCx = $1X10_B$(ALT2)
O3 = Output with IOCR bit field selection PCx = 1X11(ALT3)

Column “**Type**”:

A1 = Pad class A1 (LVTTL)
A1+ = Pad class A1+ (LVTTL)
A2 = Pad class A2 (LVTTL)
F = Pad class F (LVDS/CMOS)
D = Pad class D (ADC)
I = Pad class I (LVTTL)

S = Pad class S (CMOS)

PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)
TR = tri-state during reset ($\overline{\text{PORST}}$ = 0)

# 4 Identification Registers

The Identification Registers uniquely identify the device.

**Table 2 SAK-TC1728N-192F133HL Identification Registers**

| Short Name | Value | Address | Stepping |
|---|---|---|---|
| CBS_JDPID | 0000 6350$_H$ | F000 0408$_H$ | AB |
| CBS_JTAGID | 101D 0083$_H$ | F000 0464$_H$ | AB |
| SCU_CHIPID | 0300 9C01$_H$ | F000 0640$_H$ | AB |
| SCU_MANID | 0000 1820$_H$ | F000 0644$_H$ | AB |
| SCU_RTID | 0000 0001$_H$ | F000 0648$_H$ | AB |

**Table 3 SAK-TC1728N-192F133HR Identification Registers**

| Short Name | Value | Address | Stepping |
|---|---|---|---|
| CBS_JDPID | 0000 6350$_H$ | F000 0408$_H$ | AC |
| CBS_JTAGID | 101D 0083$_H$ | F000 0464$_H$ | AC |
| SCU_CHIPID | 8300 9C01$_H$ | F000 0640$_H$ | AC |
| SCU_MANID | 0000 1820$_H$ | F000 0644$_H$ | AC |
| SCU_RTID | 0000 0002$_H$ | F000 0648$_H$ | AC |

**Table 4 SAK-TC1728F-192F133HR Identification Registers**

| Short Name | Value | Address | Stepping |
|---|---|---|---|
| CBS_JDPID | 0000 6350$_H$ | F000 0408$_H$ | AC |
| CBS_JTAGID | 101D 0083$_H$ | F000 0464$_H$ | AC |
| SCU_CHIPID | 8300 AD01$_H$ | F000 0640$_H$ | AC |
| SCU_MANID | 0000 1820$_H$ | F000 0644$_H$ | AC |
| SCU_RTID | 0000 0002$_H$ | F000 0648$_H$ | AC |

**Table 5 SAK-TC1728F-192F133HL Identification Registers**

| Short Name | Value | Address | Stepping |
|---|---|---|---|
| CBS_JDPID | 0000 6350$_H$ | F000 0408$_H$ | AB |
| CBS_JTAGID | 101D 0083$_H$ | F000 0464$_H$ | AB |
| SCU_CHIPID | 0300 AD01$_H$ | F000 0640$_H$ | AB |

**Table 5 SAK-TC1728F-192F133HL Identification Registers** (cont'd)

| Short Name | Value | Address | Stepping |
|---|---|---|---|
| SCU_MANID | 0000 $1820_H$ | F000 $0644_H$ | AB |
| SCU_RTID | 0000 $0001_H$ | F000 $0648_H$ | AB |

# 5 Electrical Parameters

This specification provides all electrical parameters of the TC1728.

## 5.1 General Parameters

### 5.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC1728 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC1728 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC1728 designed in.

### 5.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 5.2.1**.

**Table 6 Pad Driver and Pad Classes Overview**

| Class | Power Supply | Type | Sub Class | Speed Grade | Load | Leakage[1] 150°C | Termination |
|---|---|---|---|---|---|---|---|
| **A** | 3.3 V | LVTTL I/O, LVTTL outputs | **A1** (e.g. GPIO) | 6 MHz | 100 pF | 500 nA | No |
| | | | **A1+** (e.g. serial I/Os) | 25 MHz | 50 pF | 1 µA | Series termination recommended |
| | | | **A2** (e.g. serial I/Os) | 40 MHz | 50 pF | 3 µA | Series termination recommended |
| **F** | 3.3 V | LVDS | – | 50 MHz | – | – | [2] |
| | | CMOS | – | 50 MHz | – | – | Parallel termination, 100 Ω ± 10% |
| **DE** | 5 V | ADC | – | – | – | – | |
| **I** | 3.3 V | LVTTL (input only) | – | – | – | – | |

1) Two values are given: for $T_J$ = 150 °C and a 50% higher value for $T_J$ = 160 °C.

2) In applications where the LVDS pins are not used (disabled), these pins must be either left unconnected, or properly terminated with the differential parallel termination of 100 Ω ± 10%.

### 5.1.3 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 7 Absolute Maximum Rating Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Storage temperature | $T_{ST}$ | SR | -65 | – | 160 | °C | – |
| Voltage at 1.3 V power supply pins with respect to $V_{SS}$ | $V_{DD}$ | SR | – | – | 2.0 | V | – |
| Voltage at 3.3 V power supply pins with respect to $V_{SS}$ | $V_{DDP}$ | SR | – | – | 4.33 | V | – |
| Voltage at 5 V power supply pins with respect to $V_{SS}$ | $V_{DDM}$ | SR | – | – | 7.0 | V | – |
| Voltage on any Class A input pin and dedicated input pins with respect to $V_{SS}$ | $V_{IN}$ | SR | -0.6 | – | $V_{DDP}$ + 0.5 or max. 4.33 | V | Whatever is lower |
| Voltage on any Class D analog input pin with respect to $V_{AGND}$ | $V_{AIN}$ $V_{AREFx}$ | SR | -0.6 | – | 7.0 | V | – |
| Voltage on any shared Class D analog input pin with respect to $V_{SSAF}$, if the FADC is switched through to the pin. | $V_{AINF}$ | SR | -0.6 | – | 7.0 | V | – |
| Input current on any pin during overload condition | $I_{IN}$ | | -10 | – | +10 | mA | |
| Absolute maximum sum of all input circuit currents for one port group during overload condition[1)] | $I_{IN}$ | | -75 | – | +75 | mA | |
| Absolute maximum sum of all input circuit currents during overload condition | $\Sigma I_{IN}$ | | – | – | \|200\| | mA | |

1) The port groups are defined in **Table 12**.

### 5.1.4 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

**Table 8** defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time (24000 h) is not exceeded
- **Operating Conditions** are met for
  - pad supply levels ($V_{DDP}$ or $V_{DDM}$)
  - temperature

If a pin current is out of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

*Note: An overload condition on one or more pins does not require a reset.*

**Table 8 Overload Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input current on any digital pin during overload condition except LVDS pins | $I_{IN}$ | -5 | – | +5 | mA | |
| Input current on LVDS pins | $I_{INLVDS}$ | -3 | – | +3 | mA | |
| Absolute sum of all input circuit currents for one port group during overload condition[1)] | $I_{ING}$ | -70 | – | +70 | mA | |
| Input current on analog pins | $I_{INANA}$ | -3 | – | +3 | mA | |
| Absolute sum of all analog input currents for analog inputs of a single ADC during overload condition | $I_{INSAS}$ | -15 | – | +15 | mA | |
| Absolute sum of all input circuit currents during overload condition | $\Sigma I_{INS}$ | -100 | – | 100 | mA | |

1) The port groups are defined in **Table 12**.

*Note: FADC input pins count as analog pin as they are overlayed with an ADC pins.*

**Table 9 PN-Junction Characterisitics for positive Overload**

| Pad Type | $I_{IN}$ = 3 mA | $I_{IN}$ = 5 mA |
|---|---|---|
| A1 / A1+ / F | $U_{IN} = V_{DDP} + 0.6$ V | $U_{IN} = V_{DDP} + 0.7$ V |
| A2 | $U_{IN} = V_{DDP} + 0.5$ V | $U_{IN} = V_{DDP} + 0.6$ V |
| LVDS | $U_{IN} = V_{DDP} + 0.7$ V | - |
| D / S | $U_{IN} = V_{DDM} + 0.6$ V | - |

**Table 10 PN-Junction Characterisitics for negative Overload**

| Pad Type | $I_{IN}$ = -3 mA | $I_{IN}$ = -5 mA |
|---|---|---|
| A1 / A1+ / F | $U_{IN} = V_{SS} - 0.6$ V | $U_{IN} = V_{SS} - 0.7$ V |
| A2 | $U_{IN} = V_{SS} - 0.5$ V | $U_{IN} = V_{SS} - 0.6$ V |
| LVDS | $U_{IN} = V_{SS} - 0.7$ V | - |
| D / S | $U_{IN} = V_{SSM} - 0.6$ V | - |

*Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery without having any negative reliability impact on the operational life-time.*

### 5.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC1728. All parameters specified in the following tables refer to these operating conditions, unless otherwise noticed.

Digital supply voltages applied to the TC1728 from external must be static regulated voltages which allow a typical voltage swing of ± 5 %.

All parameters specified in the following tables refer to these operating conditions (**Table 11**), unless otherwise noticed in the Note / Test Condition column.

**Table 11 Operating Conditions Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Overload coupling factor for analog inputs, negative | $K_{OVAN}$ | CC | – | – | 0.0001 | | $I_{OV} \geq$ -2 mA; $I_{OV} \leq$ 0 mA; analog pad= 5.0 V |
| Overload coupling factor for analog inputs, positive | $K_{OVAP}$ | CC | – | – | 0.00001 | | $I_{OV} \geq$ 0 mA; $I_{OV} \leq$ 3 mA; analog pad= 5.0 V |
| CPU Frequency | $f_{CPU}$ | SR | – | – | 133 | MHz | |
| FPI Frequency | $f_{FPI}$ | SR | – | – | 110 | MHz | |
| LMB Frequency | $f_{LMB}$ | SR | – | – | 133 | MHz | |
| PCP Frequency | $f_{PCP}$ | SR | – | – | 133 | MHz | |
| Inactive device pin current | $I_{ID}$ | SR | -1 | – | 1 | mA | *All power supply voltages* $V_{DDx}$ = 0 |
| Short circuit current of digital outputs[1)] | $I_{SC}$ | SR | -5 | – | 5 | mA | |
| Absolute sum of short circuit currents of the device | $\Sigma I_{SC\_D}$ | CC | – | – | 100 | mA | |
| Absolute sum of short circuit currents per pin group | $\Sigma I_{SC\_PG}$ | CC | – | – | 70 | mA | |
| Ambient Temperature | $T_A$ | SR | -40 | – | 125 | °C | |

**Table 11 Operating Conditions Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Junction temperature | $T_J$ | SR | -40 | – | 160 | °C | |
| Core Supply Voltage | $V_{DD}$ | SR | 1.17 | 1.3 | 1.43[2] | V | Only required if externally supplied[5] |
| ADC analog supply voltage | $V_{DDM}$ | SR | 2.97 | 5.0 | 5.5[3] | V | |
| EVR supply voltage | $V_5$ | SR | 4.00 | 5.0 | 5.5 | V | 5.0V single supply |
| | | | 2.97 | 3.3 | 3.63 | V | 3.3V single supply |
| Digital supply voltage for IO pads | $V_{DDP}$ | SR | 2.97 | 3.3 | 3.63[4] | V | Only required if externally supplied[5] |
| VDDP voltage to ensure defined pad states[6] | $V_{DDPPA}$ | CC | 0.65 | – | – | V | |
| Digital ground voltage | $V_{SS}$ | SR | 0 | – | – | V | |
| Analog ground voltage for $V_{DDM}$ | $V_{SSM}$ | SR | -0.1 | 0 | 0.1 | V | |

1) Applicable for digital outputs.

2) Voltage overshoot to 1.7V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

3) Voltage overshoot to 6.5V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

4) Voltage overshoot to 4.0V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

5) No external inductive load permissable if EVR is used.

6) This parameter is valid under the assumption the $\overline{\text{PORST}}$ signal is constantly at low level during the power-up/power-down of $V_{DDP}$.

**Table 12 Pin Groups for Overload / Short-Circuit Current Sum Parameter**

| Group | Pins |
|---|---|
| 1 | P0.15, P5.[7:0], P5.[15:8], P9.[8:7], P10.[3:0] |
| 2 | P0.[14:0], P2.[13:8], P3.[1:0], P3.[4:3], P3.7, P3.[15:9], P6.[3:0], P8.[2:0], P9.[4:2] |

**Table 12 Pin Groups for Overload / Short-Circuit Current Sum Parameter** (cont'd)

| Group | Pins |
|---|---|
| 3 | P1.[1:0], P1.[7:5], P1.15, P3.2, P3.[6:5], P3.8, P8.[4:3], P8.13, P9.[6:5] |
| 4 | P1.[4:2], P1.[14:8], P2.[7:0], P4.[3:0], P8.[12:5] |

## 5.2 DC Parameters

### 5.2.1 Input/Output Pins

**Table 13 Standard_Pads Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Pin capacitance (digital inputs/outputs) | $C_{IO}$ | CC | – | – | 10 | pF | $T_A$= 25 °C; $f$= 1 MHz |
| Pull-down current | $\|I_{PDL}\|$ | CC | – | – | 150 | µA | $V_i \geq 0.6 \times V_{DDP}$ V |
| | | | 10 | – | – | µA | $V_i \geq 0.36 \times V_{DDP}$ V |
| Pull-Up current | $\|I_{PUH}\|$ | CC | 10 | – | – | µA | $V_i \leq 0.6 \times V_{DDP}$ V |
| | | | – | – | 100 | µA | $V_i \leq 0.36 \times V_{DDP}$ V |
| Spike filter always blocked pulse duration | $t_{SF1}$ | CC | – | – | 10 | ns | only PORST pin |
| Spike filter pass-through pulse duration | $t_{SF2}$ | CC | 120 | – | – | ns | only PORST pin |

**Table 14 Standard_Pads Class_A1**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Input Hysteresis for pads of all A classes[1)] | $HYSA$ | CC | 0.1 x $V_{DDP}$ | – | – | V | |
| Input Leakage Current Class A1 | $I_{OZA1}$ | CC | -500 | – | 500 | nA | $V_i \leq V_{DDP}$ V; $V_i \geq 0$ V; -40°C $\leq T_J \leq$ 150°C |
| | | | -750 | – | 750 | nA | $V_i \leq V_{DDP}$ V; $V_i \geq 0$ V; 150°C $< T_J \leq$ 160°C |
| Ratio Vil/Vih, A1 pads | $V_{ILA1}$ / $V_{IHA1}$ | CC | 0.6 | – | – | | |

**Table 14 Standard_Pads Class_A1**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| On-Resistance of the class A1 pad, weak driver | $R_{DSONW}$ CC | – | 450 | 600 | Ohm | $I_{OH}$> -0.5 mA; P_MOS |
| | | – | 210 | 340 | Ohm | $I_{OL}$< 0.5 mA; N_MOS |
| On-Resistance of the class A1 pad, medium driver | $R_{DSONM}$ CC | – | – | 155 | Ohm | $I_{OH}$> -2 mA; P_MOS |
| | | – | – | 110 | Ohm | $I_{OL}$< 2 mA; N_MOS |
| Fall time,pad type A1 | $t_{FA1}$ CC | – | – | 150 | ns | $C_L$= 20 pF; pin out driver= weak |
| | | – | – | 50 | ns | $C_L$= 50 pF; pin out driver= medium |
| | | – | – | 140 | ns | $C_L$= 150 pF; pin out driver= medium |
| | | – | – | 550 | ns | $C_L$= 150 pF; pin out driver= weak |
| | | – | – | 18000 | ns | $C_L$= 20000 pF; pin out driver= medium |
| | | – | – | 65000 | ns | $C_L$= 20000 pF; pin out driver= weak |
| Rise time, pad type A1 | $t_{RA1}$ CC | – | – | 150 | ns | $C_L$= 20 pF; pin out driver= weak |
| | | – | – | 50 | ns | $C_L$= 50 pF; pin out driver= medium |
| | | – | – | 140 | ns | $C_L$= 150 pF; pin out driver= medium |
| | | – | – | 550 | ns | $C_L$= 150 pF; pin out driver= weak |
| | | – | – | 18000 | ns | $C_L$= 20000 pF; pin out driver= medium |
| | | – | – | 65000 | ns | $C_L$= 20000 pF; pin out driver= weak |

**Table 14 Standard_Pads Class_A1**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input high voltage, class A1 pads | $V_{IHA1}$ SR | 0.6 x $V_{DDP}$ | – | min($V_{DDP}$ + 0.3, 3.6) | V | |
| Input low voltage, class A1 pads | $V_{ILA1}$ SR | -0.3 | – | 0.36 x $V_{DDP}$ | V | |
| Output voltage high, class A1 pads | $V_{OHA1}$ CC | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH}$≥ -1.4 mA; pin out driver= medium |
| | | 2.4 | – | – | V | $I_{OH}$≥ -2 mA; pin out driver= medium |
| | | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH}$≥ -400 µA; pin out driver= weak |
| | | 2.4 | – | – | V | $I_{OH}$≥ -500 µA; pin out driver= weak |
| Output voltage low, class A1 pads | $V_{OLA1}$ CC | – | – | 0.4 | V | $I_{OL}$≤ 2 mA; pin out driver= medium |
| | | – | – | 0.4 | V | $I_{OL}$≤ 500 µA; pin out driver= weak |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

**Table 15 Standard_Pads Class_A1+**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input Hysteresis for A1+ pads [1] | $HYSA1$ + CC | 0.1 x $V_{DDP}$ | – | – | V | |
| Input Leakage Current Class A1+ | $I_{OZA1+}$ CC | -1000 | – | 1000 | nA | |

**Table 15 Standard_Pads Class_A1+**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| On-Resistance of the class A1+ pad, weak driver | $R_{DSONWCC}$ | – | 450 | 600 | Ohm | $I_{OH}$> -0.5 mA; P_MOS |
| | | – | 210 | 340 | Ohm | $I_{OL}$< 0.5 mA; N_MOS |
| On-Resistance of the class A1+ pad, medium driver | $R_{DSONMCC}$ | – | – | 155 | Ohm | $I_{OH}$> -2 mA; P_MOS |
| | | – | – | 110 | Ohm | $I_{OL}$< 2 mA; N_MOS |
| On-Resistance of the class A1+ pad, strong driver | $R_{DSON1+CC}$ | – | – | 110 | Ohm | $I_{OH}$> -2 mA; P_MOS |
| | | – | – | 80 | Ohm | $I_{OL}$< 2 mA; N_MOS |
| Fall time, pad type A1+ | $t_{FA1+CCC}$ | – | – | 150 | ns | $C_L$= 20 pF; pin out driver= weak |
| | | – | – | 28 | ns | $C_L$= 50 pF; edge= slow; pin out driver= strong |
| | | – | – | 16 | ns | $C_L$= 50 pF; edge= soft ; pin out driver= strong |
| | | – | – | 50 | ns | $C_L$= 50 pF; pin out driver= medium |
| | | – | – | 140 | ns | $C_L$= 150 pF; pin out driver= medium |
| | | – | – | 550 | ns | $C_L$= 150 pF; pin out driver= weak |
| | | – | – | 18000 | ns | $C_L$= 20000 pF; pin out driver= medium |
| | | – | – | 65000 | ns | $C_L$= 20000 pF; pin out driver= weak |

**Table 15 Standard_Pads Class_A1+**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Rise time, pad type A1+ | $t_{RA1+}$ CC | – | – | 150 | ns | $C_L$= 20 pF; pin out driver= weak |
| | | – | – | 28 | ns | $C_L$= 50 pF; edge= slow ; pin out driver= strong |
| | | – | – | 16 | ns | $C_L$= 50 pF; edge= soft ; pin out driver= strong |
| | | – | – | 50 | ns | $C_L$= 50 pF; pin out driver= medium |
| | | – | – | 140 | ns | $C_L$= 150 pF; pin out driver= medium |
| | | – | – | 550 | ns | $C_L$= 150 pF; pin out driver= weak |
| | | – | – | 18000 | ns | $C_L$= 20000 pF; pin out driver= medium |
| | | – | – | 65000 | ns | $C_L$= 20000 pF; pin out driver= weak |
| Input high voltage, Class A1+ pads | $V_{IHA1+}$ SR | 0.6 x $V_{DDP}$ | – | min($V_{DDP}$ + 0.3, 3.6) | V | |
| Input low voltage, Class A1+ pads | $V_{ILA1+}$ SR | -0.3 | – | 0.36 x $V_{DDP}$ | V | |
| Ratio Vil/Vih, A1+ pads | $V_{ILA1+}$ / $V_{IHA1+}$ CC | 0.6 | – | – | | |

**Table 15 Standard_Pads Class_A1+**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output voltage high, class A1+ pads | $V_{OHA1+}$ CC | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH}$≥ -1.4 mA; pin out driver= medium |
| | | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH}$≥ -1.4 mA; pin out driver= strong |
| | | 2.4 | – | – | V | $I_{OH}$≥ -2 mA; pin out driver= medium |
| | | 2.4 | – | – | V | $I_{OH}$≥ -2 mA; pin out driver= strong |
| | | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH}$≥ -400 µA; pin out driver= weak |
| | | 2.4 | – | – | V | $I_{OH}$≥ -500 µA; pin out driver= weak |
| Output voltage low, class A1+ pads | $V_{OLA1+}$ CC | – | – | 0.4 | V | $I_{OL}$≤ 2 mA; pin out driver= medium |
| | | – | – | 0.4 | V | $I_{OL}$≤ 2 mA; pin out driver= strong |
| | | – | – | 0.4 | V | $I_{OL}$≤ 500 µA; pin out driver= weak |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

**Table 16 Standard_Pads Class_A2**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input Hysteresis for A2 pads [1] | *HYSA2* CC | 0.1 x $V_{DDP}$ | – | – | V | |

**Table 16 Standard_Pads Class_A2**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input Leakage current Class A2 | $I_{OZA2}$ CC | -6000 | – | 6000 | nA | $V_i < V_{DDP} / 2 - 1$ V; $V_i > V_{DDP} / 2 + 1$ V; $V_i \geq 0$ V; $V_i \leq V_{DDP}$ V |
| | | -3000 | – | 3000 | nA | $V_i > V_{DDP} / 2 - 1$ V; $V_i < V_{DDP} / 2 + 1$ V |
| Ratio Vil/Vih, A2 pads | $V_{ILA2}$ / $V_{IHA2}$ CC | 0.6 | – | – | | |
| On-Resistance of the class A2 pad, weak driver | $R_{DSONW}$ CC | – | 450 | 600 | Ohm | $I_{OH} > -0.5$ mA; P_MOS |
| | | – | 210 | 340 | Ohm | $I_{OL} < 0.5$ mA; N_MOS |
| On-Resistance of the class A2 pad, medium driver | $R_{DSONM}$ CC | – | – | 155 | Ohm | $I_{OH} > -2$ mA; P_MOS |
| | | – | – | 110 | Ohm | $I_{OL} < 2$ mA; N_MOS |
| On-Resistance of the class A2 pad, strong driver | $R_{DSON2}$ CC | – | – | 42 | Ohm | $I_{OH} > -2$ mA; P_MOS |
| | | – | – | 22 | Ohm | $I_{OL} < 2$ mA; N_MOS |

**Table 16 Standard_Pads Class_A2**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Fall time, pad type A2 | $t_{FA2}$ CC | – | – | 150 | ns | $C_L$= 20 pF; pin out driver= weak |
| | | – | – | 7 | ns | $C_L$= 50 pF; edge= medium ; pin out driver= strong |
| | | – | – | 10 | ns | $C_L$= 50 pF; edge= medium-minus ; pin out driver= strong |
| | | – | – | 3.7 | ns | $C_L$= 50 pF; edge= sharp ; pin out driver= strong |
| | | – | – | 5 | ns | $C_L$= 50 pF; edge= sharp-minus ; pin out driver= strong |
| | | – | – | 16 | ns | $C_L$= 50 pF; edge= soft ; pin out driver= strong |
| | | – | – | 50 | ns | $C_L$= 50 pF; pin out driver= medium |
| | | – | – | 7.5 | ns | $C_L$= 100 pF; edge= sharp ; pin out driver= strong |
| | | – | – | 140 | ns | $C_L$= 150 pF; pin out driver= medium |

**Table 16 Standard_Pads Class_A2**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| | | – | – | 550 | ns | $C_L$= 150 pF; pin out driver= weak |
| | | – | – | 18000 | ns | $C_L$= 20000 pF; pin out driver= medium |
| | | – | – | 65000 | ns | $C_L$= 20000 pF; pin out driver= weak |
| Rise time, pad type A2 | $t_{RA2}$ CC | – | – | 150 | ns | $C_L$= 20 pF; pin out driver= weak |
| | | – | – | 7.0 | ns | $C_L$= 50 pF; edge= medium ; pin out driver= strong |
| | | – | – | 10 | ns | $C_L$= 50 pF; edge= medium-minus ; pin out driver= strong |
| | | – | – | 3.7 | ns | $C_L$= 50 pF; edge= sharp ; pin out driver= strong |
| | | – | – | 5 | ns | $C_L$= 50 pF; edge= sharp-minus ; pin out driver= strong |
| | | – | – | 16 | ns | $C_L$= 50 pF; edge= soft ; pin out driver= strong |
| | | – | – | 50 | ns | $C_L$= 50 pF; pin out driver= medium |
| | | – | – | 7.5 | ns | $C_L$= 100 pF; edge= sharp ; pin out driver= strong |
| | | – | – | 140 | ns | $C_L$= 150 pF; pin out driver= medium |

**Table 16 Standard_Pads Class_A2**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| | | – | – | 550 | ns | $C_L$= 150 pF; pin out driver= weak |
| | | – | – | 18000 | ns | $C_L$= 20000 pF; pin out driver= medium |
| | | – | – | 65000 | ns | $C_L$= 20000 pF; pin out driver= weak |
| Input high voltage, class A2 pads | $V_{IHA2}$ SR | 0.6 x $V_{DDP}$ | – | min($V_{DDP}$ + 0.3, 3.6) | V | |
| Input low voltage, Class A2 pads | $V_{ILA2}$ SR | -0.3 | – | 0.36 x $V_{DDP}$ | V | |
| Output voltage high, class A2 pads | $V_{OHA2}$ CC | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH}$≥ -1.4 mA; pin out driver= medium |
| | | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH}$≥ -1.4 mA; pin out driver= strong |
| | | 2.4 | – | – | V | $I_{OH}$≥ -2 mA; pin out driver= medium |
| | | 2.4 | – | – | V | $I_{OH}$≥ -2 mA; pin out driver= strong |
| | | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH}$≥ -400 µA; pin out driver= weak |
| | | 2.4 | – | – | V | $I_{OH}$≥ -500 µA; pin out driver= weak |
| Output voltage low, class A2 pads | $V_{OLA2}$ CC | – | – | 0.4 | V | $I_{OL}$≤ 2 mA; pin out driver= medium |
| | | – | – | 0.4 | V | $I_{OL}$≤ 2 mA; pin out driver= strong |
| | | – | – | 0.4 | V | $I_{OL}$≤ 500 µA; pin out driver= weak |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

**Table 17 Standard_Pads Class_F**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input Hysteresis F[1] | $HYSF$ CC | 0.05 x $V_{DDP}$ | – | – | V | |
| Input Leakage Current Class F | $I_{OZF}$ CC | -6000 | – | 6000 | nA | $V_i \leq V_{DDP}$ V; $V_i \geq 0$ V; $V_i < V_{DDP} / 2$ - 1 V; $V_i > V_{DDP} / 2$ + 1 V |
| | | -3000 | – | 3000 | nA | $V_i < V_{DDP} / 2$ + 1 V; $V_i > V_{DDP} / 2$ - 1 V |
| Ratio Vil/ Vih, F pads | $V_{ILF}$ / $V_{IHF}$ CC | 0.6 | – | – | | |
| On-Resistance of the class F pad, medium driver | $R_{DSONM}$ CC | – | – | 175 | Ohm | $I_{OH} > -2$ mA; P_MOS |
| | | – | – | 160 | Ohm | $I_{OL} < 2$ mA; N_MOS |
| Fall time, pad type F, CMOS mode | $t_{FF}$ CC | – | – | 60 | ns | $C_L = 50$ pF |
| Rise time, pad type F, CMOS mode | $t_{RF}$ CC | – | – | 60 | ns | $C_L = 50$ pF |
| Input high voltage, pad class F, CMOS mode | $V_{IHF}$ SR | 0.6 x $V_{DDP}$ | – | min($V_{DDP}$ + 0.3, 3.6) | V | |
| Input low voltage, Class F pads, CMOS mode | $V_{ILF}$ SR | -0.3 | – | 0.36 x $V_{DDP}$ | V | |
| Output high voltage, class F pads, CMOS mode | $V_{OHF}$ CC | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH} \geq -1.4$ mA |
| | | 2.4 | – | – | V | $I_{OH} \geq -2$ mA |
| Output low voltage, class F pads, CMOS mode | $V_{OLF}$ CC | – | – | 0.4 | V | $I_{OL} \leq 2$ mA |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

**Table 18 Standard_Pads Class_I**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input Hysteresis Class I[1] | $HYSI$ CC | 0.1 x $V_{DDP}$ | – | – | V | |
| Input Leakage Current | $I_{OZI}$ CC | -1000 | – | 1000 | nA | -40°C ≤ $T_J$ ≤ 150°C |
| | | -1500 | – | 1500 | nA | 150°C < $T_J$ ≤ 160°C |
| Ratio between low and high input threshold | $V_{ILI}$ / $V_{IHI}$ CC | 0.6 | – | – | | |
| Input high voltage, class I pins | $V_{IHI}$ SR | 0.6 x $V_{DDP}$ | – | min($V_{DDP}$ + 0.3, 3.6) | V | |
| Input low voltage, Class I pads | $V_{ILI}$ SR | -0.3 | – | 0.36 x $V_{DDP}$ | V | |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

LVDS parameter are valid for $V_{DD}$ = 1.235 V to 1.365 V; $V_{DDP}$ = 3.135 V to 3.465 V.

**Table 19 LVDS_Pads Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output impedance, pad class F, LVDS mode | $R_O$ CC | 40 | – | 140 | Ohm | |
| Fall time, pad type LVDS | $t_{FL}$ CC | – | – | 2 | ns | termination 100 Ω ± 1 %; |
| Rise time, pad type LVDS | $t_{RL}$ CC | – | – | 2 | ns | termination 100 Ω ± 1 %; |
| Pad set-up time | $t_{SET\_LVDS}$ CC | – | – | 13 | µs | termination 100 Ω ± 1 % |
| Output Differential Voltage | $V_{OD}$ CC | 150 | – | 400 | mV | termination 100 Ω ± 1 % |

**Table 19 LVDS_Pads Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output voltage high, pad class F, LVDS mode | $V_{OH}$ CC | – | – | 1525 | mV | termination 100 Ω ± 1 % |
| Output voltage low, pad class F, LVDS mode | $V_{OL}$ CC | 875 | – | – | mV | termination 100 Ω ± 1 % |
| Output Offset Voltage | $V_{OS}$ CC | 1075 | – | 1325 | mV | termination 100 Ω ± 1 % |

Class S pad parameters are only valid for $V_{DDM}$ = 4.75 V to 5.25 V.

**Table 20 Standard_Pads Class_S**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input Hysteresis for class S pads[1] | $HYSS$ CC | 0.3 | – | – | V | |
| Input leakage current | $I_{OZS}$ CC | –300 | – | 300 | nA | |
| Input voltage high | $V_{IHS}$ CC | – | – | 3.6 | V | |
| Input voltage low | $V_{ILS}$ CC | 1.9 | – | – | V | |
| $V_{ILS}$ Delta [2] | $V_{ILSD}$ CC | -50 | – | 50 | mV | Maximum input low state treshold variation over 1ms ($V_{DDP}$ = constant) |

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

2) $V_{ILSD}$ is implemented to ensure J2716 specification. It can't be guaranteed that it suppresses switching due to external noise.

### 5.2.2 Analog to Digital Converters (ADCx)

ADC parameter in **Table 21** are valid for $V_{DD}$ = 1.235 V to 1.365 V; $V_{DDM}$ = 4.75 V to 5.25 V; $T_J$ = 150°C.

**Table 21 5V ADC Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Switched capacitance at the analog voltage inputs[1] | $C_{AINSW}$ CC | – | 9 | 20 | pF | |
| Total capacitance of an analog input | $C_{AINTOT}$ CC | – | 20 | 30 | pF | |
| Switched capacitance at the positive reference voltage input[2][3] | $C_{AREFSW}$ CC | – | 15 | 30 | pF | |
| Total capacitance of the voltage reference inputs[2] | $C_{AREFTOT}$ CC | – | 20 | 40 | pF | |
| Differential Non-Linearity Error[4][5][6][7] | $EA_{DNL}$ CC | -3 | – | 3 | LSB | ADC resolution= 12-bit [8] [9] |
| Gain Error[4][5][6][7] | $EA_{GAIN}$ CC | -3.5 | – | 3.5 | LSB | ADC resolution= 12-bit [8] [9] |
| Integral Non-Linearity[4][5][6][7] | $EA_{INL}$ CC | -3 | – | 3 | LSB | ADC resolution= 12-bit[8] [9] |
| Offset Error[4][5][6][7] | $EA_{OFF}$ CC | -4 | – | 4 | LSB | ADC resolution= 12-bit [8] [9] |
| Converter clock | $f_{ADC}$ SR | 4 | – | 110 | MHz | $f_{ADC}$= $f_{FPI}$ |
| Internal ADC clock | $f_{ADCI}$ CC | 1 | – | 20 | MHz | [10] |
| Charge consumption per conversion | $Q_{CONV}$ CC | 70 | 85[11] | 100 | pC | charge needs to be provided via $V_{AREF0}$ |

**Table 21 5V ADC Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input leakage at analog inputs[12)] | $I_{OZ1}$ CC | -100 | – | 500 | nA | $V_i \geq$ 0.97 x $V_{DDM}$ V; $V_i \leq V_{DDM}$ V; overlayed= No |
| | | -100 | – | 600 | nA | $V_i \geq$ 0.97 x $V_{DDM}$ V; $V_i \leq V_{DDM}$ V; overlayed= Yes |
| | | -500 | – | 100 | nA | $V_i \geq$ 0 V; $V_i \leq$ 0.03 x $V_{DDM}$ V; overlayed= No |
| | | -600 | – | 100 | nA | $V_i \leq$ 0.03 x $V_{DDM}$ V; $V_i \geq$ 0 V; overlayed= Yes |
| | | -100 | – | 200 | nA | $V_i >$ 0.03 x $V_{DDM}$ V; $V_i <$ 0.97 x $V_{DDM}$ V; overlayed= No |
| | | -100 | – | 300 | nA | $V_i >$ 0.03 x $V_{DDM}$ V; $V_i <$ 0.97 x $V_{DDM}$ V; overlayed= Yes |
| Input leakage current at Varef0 | $I_{OZ2}$ CC | -2 | – | 2 | µA | $V_{AREF0} \geq$ 0V; $V_{AREF0} \leq V_{DDM}$ V |
| Input leakage current at Vagnd0 | $I_{OZ3}$ CC | -2 | – | 2 | µA | $V_{AGND0} \geq$ 0V; $V_{AGND0} \leq V_{DDM}$ V |
| ON resistance of the transmission gates in the analog voltage path | $R_{AIN}$ CC | – | 900 | 1500 | Ohm | |

**Table 21 5V ADC Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ON resistance for the ADC test (pull down for AIN7) | $R_{AIN7T}$ CC | 180 | 550 | 900 | Ohm | Test feature available only for odd AINx pins |
| Resistance of the reference voltage input path | $R_{AREF}$ CC | – | 500 | 1000 | Ohm | 500 Ohm increased if AIN[1:0] used as reference input |
| Broken wire detection delay against VAGND | $t_{BWG}$ CC | – | – | 50 | [13] | |
| Broken wire detection delay against VAREF | $t_{BWR}$ CC | – | – | 50 | [14] | |
| Sample time | $t_S$ CC | 2 | – | 257 | $T_{ADCI}$ | |
| Calibration time after bit ADC_GLOBCFG.SUCAL is set | $t_{CAL}$ CC | – | – | 4352 | cycles | |
| Total Unadjusted Error[5][6][15] | $TUE$ CC | -4 | – | 4[16] | LSB | ADC resolution= 12-bit |
| Wakeup time from analog powerdown, fast mode | $t_{AWAF}$ CC | – | – | 5 | µs | |
| Wakeup time from analog powerdown, slow mode | $t_{AWAS}$ CC | – | – | 10 | µs | |
| Analog reference ground[2] | $V_{AGND0}$ SR | $V_{SSM}$ - 0.05 | – | $V_{AREF0}$ - $V_{DDM}$/2 | V | |
| Analog input voltage | $V_{AIN}$ SR | $V_{AGND0}$ | – | $V_{AREF0}$ | V | |
| Analog reference voltage[2] | $V_{AREF0}$ SR | $V_{AGND0}$ + $V_{DDM}$/2 | – | $V_{DDM}$ + 0.05[17][18] | V | |
| Analog reference voltage range[5][6][2] | $V_{AREF0}$ - $V_{AGND0}$ SR | $V_{DDM}$/2 | – | $V_{DDM}$ + 0.05 | V | |

1) The sampling capacity of the conversion C-network is pre-charged to $V_{AREF}$/2 before the sampling moment. Because of the parasitic elements the voltage measured at AINx can deviate from $V_{AREF}$/2.
2) Applies to AINx, when used as auxiliary reference input.
3) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead smaller capacitances are successively switched to the reference voltage.
4) The sum of DNL/INL/GAIN/OFF errors does not exceed the related TUE total unadjusted error.
5) If the analog reference voltage range is below $V_{DDM}$ but still in the defined range of $V_{DDM}$ / 2 and $V_{DDM}$ is used, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE,DNL,INL,Gain, and Offset errors increase also by the factor 1/k.
6) If a reduced analog reference voltage between 1V and $V_{DDM}$ / 2 is used, then there are additonal decrease in the ADC speed and accuracy.
7) If the analog reference voltage is > $V_{DDM}$, then the ADC converter errors increase.
8) For 10-bit conversions the error value must be multiplied with a factor 0.25.
9) For 8-bit conversions the error value must be multiplied with a factor 0.0625.
10) If the alternate reference is used or $f_{ADCI}$ is more than 16 MHz, the accuracy of the ADC may decrease.
11) For a conversion time of 1 µs a rms value of 85µA result for $I_{AREF0}$.
12) The leakage current definition is a continous function,as shown in figure ADCx Analoge Input Leakage. The numerical values defined determine the characteristic points of the given countinuous linear approximation - they do not define step function.
13) The broken wire detection delay against $V_{AGND}$ is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 250µs. Results below 10% ($199_H$).
14) The broken wire detection delay against $V_{AREF}$ is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 10µs. This function is influenced by leakage current, in particular at high temperature.Results above 60% ($999_H$).
15) Measured without noise.
16) For 10-bit conversion the TUE is ±2LSB; for 8-bit conversion the TUE is ±1LSB
17) A running conversion may become inexact in case of violating the normal conditions (voltage overshoot).
18) If the reference voltage $V_{AREF}$ increase or the $V_{DDM}$ decrease, so that $V_{AREF}$ = ($V_{DDM}$ + 0.05V to $V_{DDM}$ + 0.07V), then the accuracy of the ADC decrease by 4LSB12.

ADC parameter in **Table 22** are valid for $V_{DD}$ = 1.235 V to 1.365 V; $V_{DDM}$ = 3.135 V to 3.465 V; $T_J$ = 150°C.

**Table 22 3.3V ADC Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Switched capacitance at the analog voltage inputs[1)] | $C_{AINSW}$ CC | – | 9 | 20 | pF | |
| Total capacitance of an analog input | $C_{AINTOT}$ CC | – | 20 | 30 | pF | |

**Table 22 3.3V ADC Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Switched capacitance at the positive reference voltage input[2)3)] | $C_{AREFSW}$ CC | – | 15 | 30 | pF | |
| Total capacitance of the voltage reference inputs[2)] | $C_{AREFOT}$ CC | – | 20 | 40 | pF | |
| Differential Non-Linearity Error[4)5)6)7)] | $EA_{DNL}$ CC | -4 | – | 4 | LSB | ADC resolution= 12-bit 8) 9) |
| Gain Error[4)5)6)7)] | $EA_{GAIN}$ CC | -3.5 | – | 3.5 | LSB | ADC resolution= 12-bit 8) 9) |
| Integral Non-Linearity[4)5)6)7)] | $EA_{INL}$ CC | -4 | – | 4 | LSB | ADC resolution= 12-bit[8) 9)] |
| Offset Error[4)5)6)7)] | $EA_{OFF}$ CC | -4 | – | 4 | LSB | ADC resolution= 12-bit 8) 9) |
| Converter clock | $f_{ADC}$ SR | 4 | – | 110 | MHz | $f_{ADC}$= $f_{FPI}$ |
| Internal ADC clock | $f_{ADCI}$ CC | 1 | – | 20 | MHz | 10) |
| Charge consumption per conversion[11)] | $Q_{CONV}$ CC | – | – | 70 | pC | charge needs to be provided via $V_{AREF0}$ |

**Table 22 3.3V ADC Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input leakage at analog inputs[12)] | $I_{OZ1}$ C C | -100 | – | 500 | nA | $V_i \geq 0.97 \times V_{DDM}$ V; $V_i \leq V_{DDM}$ V; overlayed= No |
| | | -100 | – | 600 | nA | $V_i \geq 0.97 \times V_{DDM}$ V; $V_i \leq V_{DDM}$ V; overlayed= Yes |
| | | -500 | – | 100 | nA | $V_i \geq 0$ V; $V_i \leq 0.03 \times V_{DDM}$ V; overlayed= No |
| | | -600 | – | 100 | nA | $V_i \leq 0.03 \times V_{DDM}$ V; $V_i \geq 0$ V; overlayed= Yes |
| | | -100 | – | 200 | nA | $V_i > 0.03 \times V_{DDM}$ V; $V_i < 0.97 \times V_{DDM}$ V; overlayed= No |
| | | -100 | – | 300 | nA | $V_i > 0.03 \times V_{DDM}$ V; $V_i < 0.97 \times V_{DDM}$ V; overlayed= Yes |
| Input leakage current at Varef | $I_{OZ2}$ CC | -2 | – | 2 | µA | $V_{AREF0} \leq V_{DDM}$ V |
| Input leakage current at Vagnd | $I_{OZ3}$ CC | -2 | – | 2 | µA | $V_{AGND0} \leq V_{DDM}$ V |
| ON resistance of the transmission gates in the analog voltage path | $R_{AIN}$ C C | – | 3500 | 9000 | Ohm | |
| ON resistance for the ADC test (pull down for AIN7) | $R_{AIN7T}$ CC | 180 | 800 | 1800 | Ohm | Test feature available only for odd AINx pins |

**Table 22 3.3V ADC Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Resistance of the reference voltage input path | $R_{AREF}$ CC | – | 1700 | 3000 | Ohm | 500 Ohm increased if AIN[1:0] used as reference input |
| Broken wire detection delay against VAGND | $t_{BWG}$ CC | – | – | 50 | 13) | |
| Broken wire detection delay against VAREF | $t_{BWR}$ CC | – | – | 50 | 14) | |
| Sample time | $t_S$ CC | 2 | – | 257 | $T_{ADCI}$ | |
| Calibration time after bit ADC_GLOBCFG.SUCAL is set | $t_{CAL}$ CC | – | – | 4352 | cycles | |
| Total Unadjusted Error[5)6)15)] | $TUE$ CC | -4.5 | – | 4.5[16)] | LSB | ADC resolution= 12-bit |
| Analog reference ground[2)] | $V_{AGND0}$ SR | $V_{SSM}$ - 0.05 | – | $V_{AREF0}$ - $V_{DDM}$/2 | V | |
| Analog input voltage | $V_{AIN}$ SR | $V_{AGND0}$ | – | $V_{AREF0}$ | V | |
| Analog reference voltage[2)] | $V_{AREF0}$ SR | $V_{AGND0}$ + $V_{DDM}$/2 | – | $V_{DDM}$ + 0.05[17) 18)] | V | |
| Analog reference voltage range[5)6)2)] | $V_{AREF0}$ - $V_{AGND0}$ SR | $V_{DDM}$/2 | – | $V_{DDM}$ + 0.05 | V | |

1) The sampling capacity of the conversion C-network is pre-charged to $V_{AREF}$/2 before the sampling moment. Because of the parasitic elements the voltage measured at AINx can deviate from $V_{AREF}$/2.

2) Applies to AINx, when used as auxiliary reference input.

3) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead smaller capacitances are successively switched to the reference voltage.

4) The sum of DNL/INL/GAIN/OFF errors does not exceed the related TUE total unadjusted error.

5) If the analog reference voltage range is below $V_{DDM}$ but still in the defined range of $V_{DDM}$ / 2 and $V_{DDM}$ is used, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE,DNL,INL,Gain, and Offset errors increase also by the factor 1/k.

6) If a reduced analog reference voltage between 1V and $V_{DDM}$ / 2 is used, then there are additonal decrease in the ADC speed and accuracy.
7) If the analog reference voltage is > $V_{DDM}$, then the ADC converter errors increase.
8) For 10-bit conversions the error value must be multiplied with a factor 0.25.
9) For 8-bit conversions the error value must be multiplied with a factor 0.0625.
10) If the alternate reference is used, or $f_{ADCI}$ is more than 16 MHz, or STC is lower than 8, the accuracy of the ADC may decrease.
11) $Q_{CONV}$ is calculated as $Q_{CONV} = C_{AREF} * V_{AREF}$.
12) The leakage current definition is a continous function,as shown in figure ADCx Analoge Input Leakage. The numerical values defined determine the characteristic points of the given countinuous linear approximation - they do not define step function.
13) The broken wire detection delay against $V_{AGND}$ is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 250µs. Results below 10% ($199_H$).
14) The broken wire detection delay against $V_{AREF}$ is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 10µs. This function is influenced by leakage current, in particular at high temperature.Results above 60% ($999_H$).
15) Measured without noise.
16) For 10-bit conversion the TUE is ±2LSB; for 8-bit conversion the TUE is ±1LSB
17) A running conversion may become inexact in case of violating the normal conditions (voltage overshoot).
18) If the reference voltage $V_{AREF}$ increase or the $V_{DDM}$ decrease, so that $V_{AREF}$ = ($V_{DDM}$ + 0.05V to $V_{DDM}$ + 0.07V), then the accuracy of the ADC decrease by 4LSB12.

**Table 23 Conversion Time** (Operating Conditions apply)

| Parameter | Symbol | Values | Unit | Note |
|---|---|---|---|---|
| Conversion time with post-calibration | $t_C$ CC | $2 \times T_{ADC} + (4 + STC + n) \times T_{ADCI}$ | µs | n = 8, 10, 12 for n - bit conversion<br>$T_{ADC} = 1 / f_{FPI}$<br>$T_{ADCI} = 1 / f_{ADCI}$ |
| Conversion time without post-calibration | | $2 \times T_{ADC} + (2 + STC + n) \times T_{ADCI}$ | | |

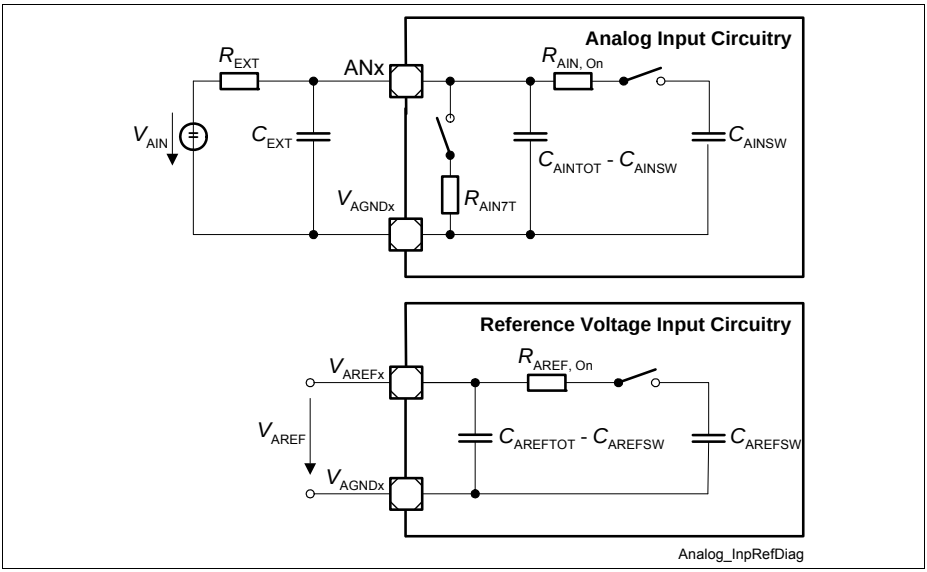



**Figure 3 ADCx Input Circuits**

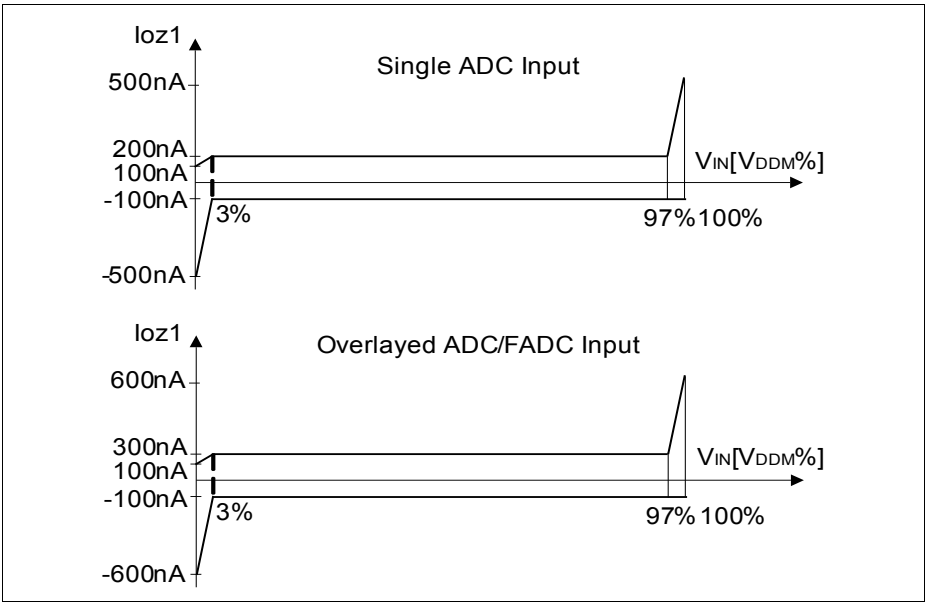



**Figure 4 ADCx Analog Inputs Leakage**

### 5.2.3 Fast Analog to Digital Converter (FADC)

FADC parameter are valid for $V_{DDM}$ = 4.75 V to 5.25 V;$T_J$ = 150°C.

**Table 24 FADC Parameters with $V_{DDM}$ = 5V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| DNL error | $EF_{DNL}$ CC | -1 | – | 1 | LSB | $V_{IN}$ mode= differential Gain = 1, 2 |
| | | -1 | – | 1 | LSB | $V_{IN}$ mode= single ended Gain = 1, 2 |
| | | -2 | – | 2 | LSB | $V_{IN}$ mode= differential Gain = 4, 8 $T_J$ = 150°C 1) |
| | | -2.5 | – | 2.5 | LSB | $V_{IN}$ mode= differential Gain = 4, 8 $T_J$ = 160°C 1) |
| | | -2 | – | 2 | LSB | $V_{IN}$ mode= single ended Gain = 4, 8 $T_J$ = 150°C 1) |
| | | -2.5 | – | 2.5 | LSB | $V_{IN}$ mode= single ended Gain = 4, 8 $T_J$ = 160°C 1) |

**Table 24 FADC Parameters with $V_{DDM}$ = 5V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| GRADient error | $EF_{GRAD}$ CC | -5 | – | 5 | % | $V_{IN}$ mode= differential ; Gain< 4 |
| | | -5 | – | 5 | % | $V_{IN}$ mode= single ended ; Gain< 4 |
| | | -5.5 | – | 5 | % | $V_{IN}$ mode= differential ; Gain= 4 |
| | | -5.5 | – | 5 | % | $V_{IN}$ mode= single ended ; Gain= 4 |
| | | -6 | – | 6 | % | $V_{IN}$ mode= differential ; Gain= 8 |
| | | -6 | – | 6 | % | $V_{IN}$ mode= single ended ; Gain= 8 |
| INL error | $EF_{INL}$ CC | -4 | – | 4 | LSB | $V_{IN}$ mode= differential |
| | | -4 | – | 4 | LSB | $V_{IN}$ mode= single ended |

**Table 24 FADC Parameters with $V_{DDM}$ = 5V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Offset error | $EF_{OFF}$ CC | -90 | – | 90 | mV | $V_{IN}$ mode= differential ; Calibration= No |
| | | -90 | – | 90 | mV | $V_{IN}$ mode= single ended ; Calibration= No |
| | | -20 | – | 20 | mV | $V_{IN}$ mode= differential ; Calibration= Yes 2)3) |
| | | -20 | – | 20 | mV | $V_{IN}$ mode= single ended ; Calibration= Yes 2)3) |
| Error of common mode voltage $V_{FAREFI}$/2 | $EF_{REFI}$ CC | -80 | – | 80 | mV | |
| Channel amplifier cutoff frequency | $f_{COFF}$ CC | 2 | – | – | MHz | |
| Converter clock | $f_{FADC}$ SR | 4 | – | 110 | MHz | $f_{FADC}$= $f_{FPI}$ |
| Conversion time | $t_C$ CC | – | – | 21 | 1 / $f_{FADC}$ | For 10-bit conversion |
| Input resistance of the analog voltage path (Rn, Rp) | $R_{FAIN}$ CC | 100 | – | 200 | kOhm | |
| Settling time of a channel amplifier after changing ENN or ENP | $t_{SET}$ CC | – | – | 5 | µs | |
| Analog input voltage range[4)] | $V_{AINF}$ SR | $V_{SSM}$ | – | $V_{DDP}$ | V | |
| Wakeup time from analog powerdown, fast mode | $t_{FWAF}$ CC | – | – | 5 | µs | |
| Wakeup time from analog powerdown, slow mode | $t_{FWAS}$ CC | – | – | 10 | µs | |

**Table 24 FADC Parameters with $V_{DDM}$ = 5V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Analog reference ground | $V_{FAGNDI}$ CC | – | 0 | – | V | Internally generated |
| Analog reference voltage | $V_{FAREFI}$ CC | – | 3.3 | –[5)6)] | V | Internally generated |

1) No missing codes.

2) Calibration should be preformed at each power-up. In case of a continous operation, it should be performed minimium once per week.

3) The offser error voltage drifts over the whole temperature range maximum +-3LSB.

4) The accuracy values is valid between 5% and 90%of $V_{AINF}$

5) Voltage overshoot to 4V is permissible, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

6) A running conversion may become inexact in case of violating the nomal operating conditions (voltage overshoots).

The calibration procedure should run after each power-up, when all power supply voltages and the reference voltage have stabilized.

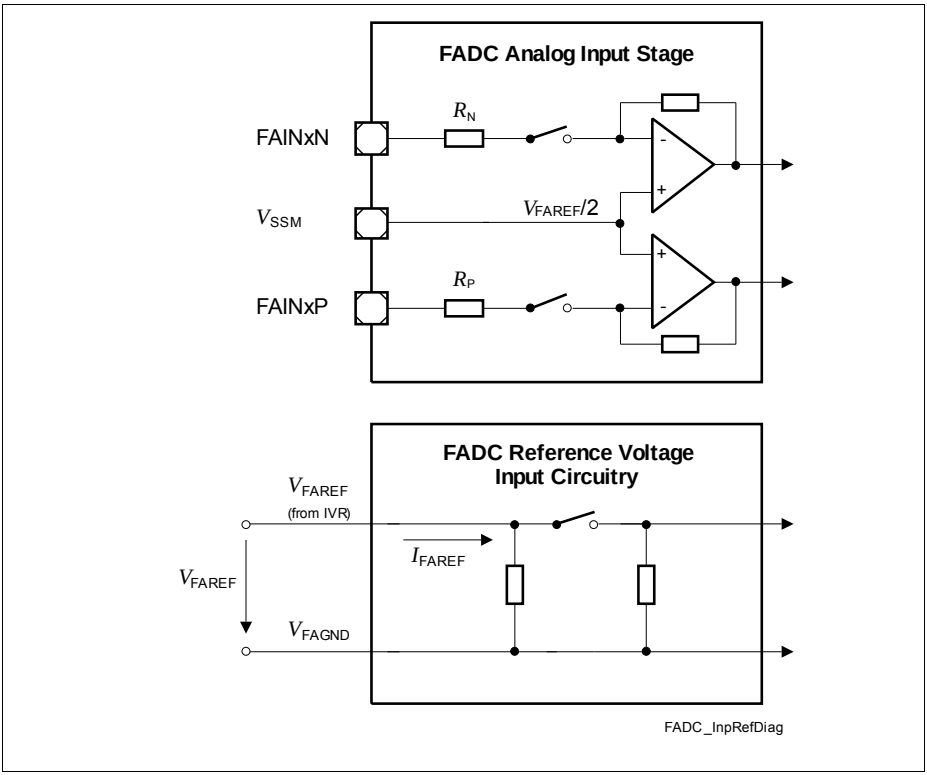



**Figure 5 FADC Input Circuits**

### 5.2.4 Oscillator Pins

**Table 25 OSC_XTAL Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Input current at XTAL1 | $I_{IX1}$ | CC | -25 | – | 25 | µA | $V_{IN}$> 0 V; $V_{IN}$<$V_{DDP}$ |
| Input frequency | $f_{OSC}$ | SR | 4 | – | 40 | MHz | Direct Input Mode selected |
| | | | 8 | – | 25 | MHz | External Crystal Mode selected |
| Oscillator start-up time[1] | $t_{OSCS}$ | CC | – | – | 10 | ms | |
| Input high voltage at XTAL1[2] | $V_{IHX}$ | SR | 0.7 x $V_{DDP}$ | – | $V_{DDP}$ + 0.5 | V | |
| Input low voltage at XTAL1 | $V_{ILX}$ | SR | -0.5 | – | 0.3 x $V_{DDP}$ | V | |
| Input hysteresis for XTAL1 pad[3] | $HYSAX$ | CC | – | – | 200 | mV | |

1) $t_{OSCS}$ is defined from the moment when $V_{DDP}$ = 3.13V until the oscillations reach an amplitude at XTAL1 of 0.3 * $V_{DDP}$. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystral suppliers.

2) If the XTAL1 pin is driven by a crystal, reaching a minimum amplitude (peak-to-peak) of 0.3 * $V_{DDP}$ is necessary.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

*Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.*

### 5.2.5 Power Supply Current

The total power supply current defined below consists of leakage and switching component.

Application relevant values are typically lower than those given in the following two tables and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

The operating conditions for the parameters in the following table are:
$V_{DD}$=1.365 V, $V_{DDP}$=3.47 V, $V_{DDM}$=5.1 V, $f_{LMB}$=133 / 80 MHz, $T_J$=160 °C

The realisic power pattern defines the following conditions:

- $T_J$=150 °C
- $f_{LMB}$ = $f_{PCP}$ = $f_{CPU}$ = 133 / 80 MHz
- $f_{FPI}$ = 66.5 / 80 MHz
- $V_{DD}$ = 1.326 V
- $V_{DDP}$ = 3.366 V
- $V_{DDM}$ = 5.1 V

The max power pattern defines the following conditions:

- $T_J$=160 °C
- $f_{LMB}$ = $f_{PCP}$ = $f_{CPU}$ = 133 / 80 MHz
- $f_{FPI}$ = 66.5 / 80MHz
- $V_{DD}$ = 1.37 V
- $V_{DDP}$ = 3.47 V
- $V_{DDM}$ = 5.25 V

**Table 26 Power Supply Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Core active mode supply current[1] | $I_{DD}$ CC | – | – | 310[2] | mA | power pattern= max |
| | | – | – | 212[3] | mA | power pattern= realistic |
| $I_{DD}$ current at PORST Low | $I_{DD\_PORST}$ CC | – | – | 110 | mA | |
| PORST pad output current | $I_{DDPORST}$ CC | 13 | – | – | mA | |
| Sum of all 1.3 V supply currents | $I_{DDSUM}$ CC | – | – | 212[4] | mA | power pattern= realistic |
| $I_{DDP}$ current at PORST Low | $I_{DDP\_PORST}$ CC | – | – | 6 | mA | |

**Table 26 Power Supply Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $I_{DDP}$ current no pad activity, LVDS off[5] | $I_{DDP}$ CC | – | – | $I_{DDP\_PORST}$ + 83 | mA | including flash read current |
| | | – | – | $I_{DDP\_PORST}$ + 62 | mA | including flash programming current [6] |
| | | – | – | $I_{DDP\_PORST}$ + 91[7] | mA | including flash erase verify current [6] |
| ADC 5V power supply current | $I_{DDM}$ CC | – | – | 32 | mA | |
| Current Consumption of LVDS Pad Pairs | $I_{LVDS}$ CC | – | – | 12 | mA | for all LVDS pads in total |
| EVR Supply current | $I_{V5}$ CC | – | – | 387 | mA | power pattern= max; mode = 5V only with ext. pass device; SAK-TC1728F-192F133HL SAK-TC1728F-192F133HR |
| | | | | 382 | mA | power pattern= max; mode = 5V only with ext. pass device; SAK-TC1728N-192F133HL SAK-TC1728N-192F133HR |
| | | – | – | 292 | mA | power pattern= real; mode = 5V only with ext. pass device; SAK-TC1728F-192F133HL SAK-TC1728F-192F133HR |
| | | | | 287 | mA | power pattern= real; mode = 5V only with ext. pass device; SAK-TC1728N-192F133HL SAK-TC1728N-192F133HR |

**Table 26 Power Supply Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum power dissipation | $PD_{CC}$ | – | – | 902 | mW | power pattern= max; mode = all external |
| | | – | – | 744 | mW | power pattern= realistic mode = all external |
| Maximum power dissipation | $PD_{CC}$ | – | – | 2032 | mW | power pattern= max; mode = 5V only with ext. pass device; SAK-TC1728F-192F133HL SAK-TC1728F-192F133HR |
| | | | | 2006 8) | mW | power pattern= max; mode = 5V only with ext. pass device; SAK-TC1728N-192F133HL SAK-TC1728N-192F133HR |
| | | – | – | 1490 | mW | power pattern= realistic mode = 5V only with ext. pass device; SAK-TC1728F-192F133HL SAK-TC1728F-192F133HR |
| | | – | – | 1464 9) | mW | power pattern= realistic mode = 5V only with ext. pass device; SAK-TC1728N-192F133HL SAK-TC1728N-192F133HR |

1) Infineon Power Loop: CPU and PCP running, all peripherals active. The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.

2) The $I_{DD}$ decreases typically by 62mA if the $f_{CPU}$ decreases by 50MHz, at constant $T_j$.

3) The $I_{DD}$ decreases typically by 52mA if the $f_{CPU}$ decreases by 50MHz, at constant $T_j$.

4) The $I_{DD}$ decreases typically by 52mA if the $f_{CPU}$ decreases by 50MHz, at constant $T_j$.

5) For operations including the D-Flash the required current is always lower than the current for non-DFlash operations.

6) Relevant for the power supply dimensioning, not for thermal considerations.

7) In case of erase of Program Flash PF, internal flash array loading effects may generate transient current spikes of up to 15 mA for maximum 5 ms per flash module.

8) Maximum power dissipation for $f_{CPU}$ = 80 MHz and no external pass device is 1695mW.

9) Maximum power dissipation for $f_{CPU}$ = 80 MHz and no external pass device is 1260 mW.

### 5.2.5.1 Calculating the 1.3 V Current Consumption

The current consumption of the 1.3 V rail compose out of two parts:

- Static current consumption
- Dynamic current consumption

The static current consumption is related to the device temperature $T_J$ and the dynamic current consumption depends of the configured clocking frequencies and the software application executed. These two parts needs to be added in order to get the rail current consumption.

(1)

$$I_0 = 0,674\left[\frac{mA}{C}\right] \times e^{0,02592 \times T_J[C]}$$

(2)

$$I_0 = 3,9\left[\frac{mA}{C}\right] \times e^{0,02085 \times T_J[C]}$$

Function 1 defines the typical static current consumption and Function 2 defines the maximum static current consumption. Both functions are valid for $V_{DD}$ = 1.326 V.

For the dynamic current consumption using the application pattern and $f_{LMB}$ = $f_{PCP}$ = 2 * $f_{FPI}$ the function 4 applies:

(3)

$$I_{Dym} = 0,76\left[\frac{mA}{MHz}\right] \times f_{CPU}[MHz]$$

For the dynamic current consumption using the application pattern and $f_{LMB}$ = $f_{PCP}$ = $f_{FPI}$ the function 5 applies:

(4)

$$I_{Dym} = 0,9\left[\frac{mA}{MHz}\right] \times f_{CPU}[MHz]$$

and this finally results in

(5)

$$I_{DD} = I_0 + I_{DYM}$$

## 5.3 AC Parameters

All AC parameters are defined with maximum driver strength unless otherwise stated.

### 5.3.1 Testing Waveforms

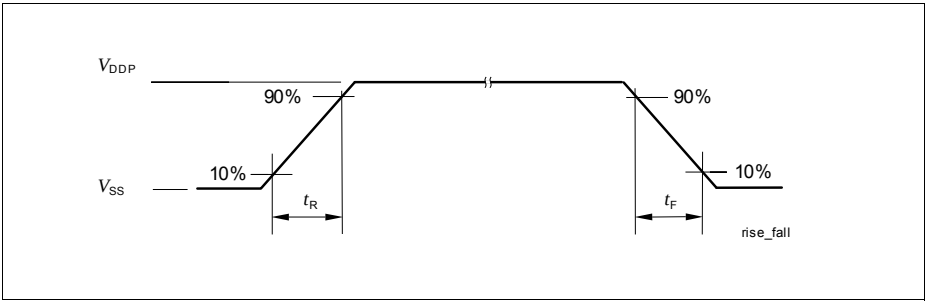



**Figure 6 Rise/Fall Time Parameters**

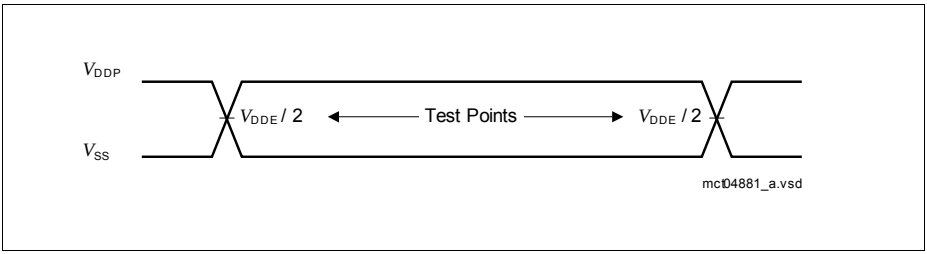



**Figure 7 Testing Waveform, Output Delay**

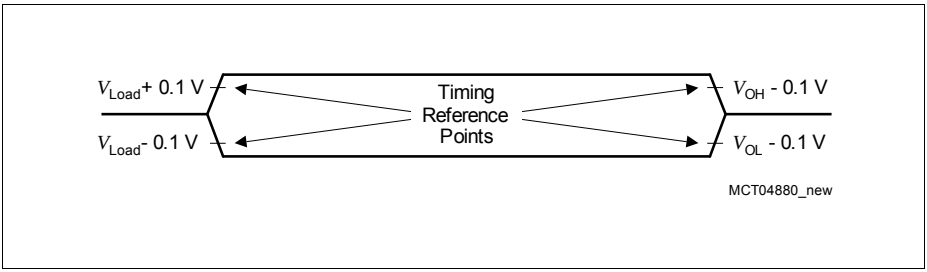



**Figure 8 Testing Waveform, Output High Impedance**

### 5.3.2 Power Sequencing 5V Supply Only

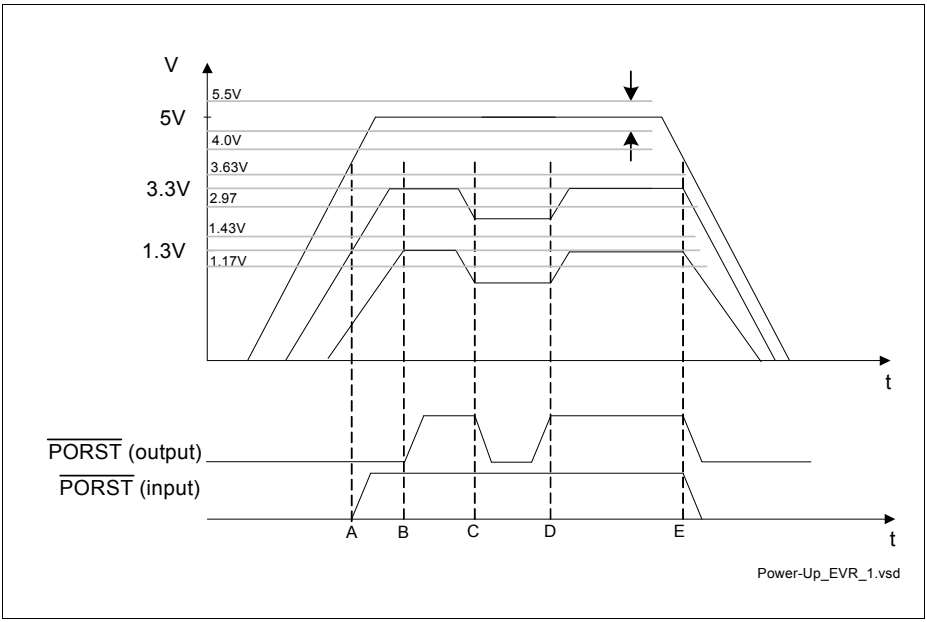



**Figure 9 5 V / 3.3 V / 1.3 V Power-Up/Down Sequence**

The events for the above points in the power-up/down sequence

- A :external supplied voltage reaches operating level
- B: external supplied and internal generated voltages reaches operating levels
- C: internal generated voltage drops below operating level
- D: internal generated voltage resumes operating level
- E: external supplied voltage leaves operating level

P0.4 and P0.5 should be kept at the selected setting of '0' or '1' until external supplied voltage has reached its operating level.

The following list of rules applies to the power-up/down sequence:

- All ground pins $V_{SS}$ must be externally connected to one single star point in the system. Regarding the DC current component, all ground pins are internally directly connected.
- The latch-up risk is minimized if the I/O currents are limited to:
  - 20 mA for one pin group
  - AND 100 mA for the completed device I/Os

  - AND additionally before power-up / after power-down:
    1 mA for one pin in inactive mode (0 V on all power supplies)
- The PORST signal may be deactivated after all VDD5, and VAREF0 power-supplies and the oscillator have reached stable operation, within the normal operating conditions.
- At normal power down the PORST signal should be activated within the normal operating range, and then the power supplies may be switched off. Care must be taken that all Flash write or delete sequences have been completed.
- In case of a power-loss at any power-supply, all power supplies must be powered-down, conforming at the same time to the rule number 2.
- Although not necessary, it is additionally recommended that all power supplies are powered-up/down together in a controlled way, as tight to each other as possible.
- Additionally, regarding the ADC reference voltage VAREF0:
  - VAREF0 must power-up at the same time or later then VDDM, and
  - VAREF0 must power-down either earlier or at latest to satisfy the condition VAREF0 < VDDM + 0.5 V. This is required in order to prevent discharge of VAREF0 filter capacitance through the ESD diodes through the VDDM power supply. In case of discharging the reference capacitance through the ESD diodes, the current must be lower than 5 mA.

### 5.3.3 Power Sequencing 3.3V Supply Only

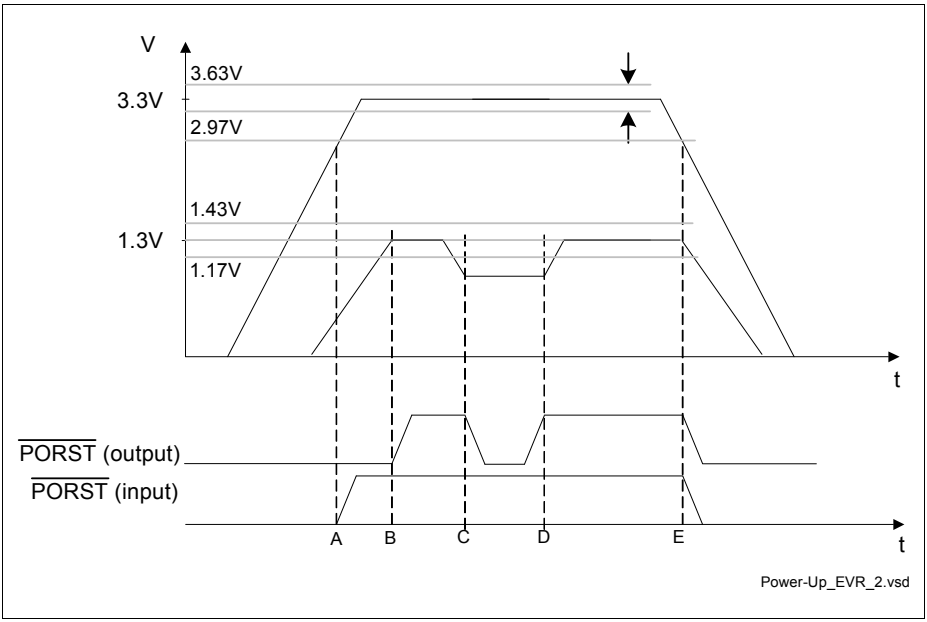



**Figure 10 3.3 V / 1.3 V Power-Up/Down Sequence**

The events for the above points in the power-up/down sequence

- A :external supplied voltage reaches operating level
- B: external supplied and internal generated voltages reaches operating levels
- C: internal generated voltage drops below operating level
- D: internal generated voltage resumes operating level
- E: external supplied voltage leaves operating level

P0.4 and P0.5 should be kept at the selected setting of '0' or '1' until external supplied voltage has reached its operating level.

The following list of rules applies to the power-up/down sequence:

- All ground pins $V_{SS}$ must be externally connected to one single star point in the system. Regarding the DC current component, all ground pins are internally directly connected.
- The latch-up risk is minimized if the I/O currents are limited to:
  – 20 mA for one pin group
  – AND 100 mA for the completed device I/Os

  - AND additionally before power-up / after power-down:
    1 mA for one pin in inactive mode (0 V on all power supplies)
- The PORST signal may be deactivated after all VDD3.3, and VAREF0 power-supplies and the oscillator have reached stable operation, within the normal operating conditions.
- At normal power down the PORST signal should be activated within the normal operating range, and then the power supplies may be switched off. Care must be taken that all Flash write or delete sequences have been completed.
- In case of a power-loss at any power-supply, all power supplies must be powered-down, conforming at the same time to the rule number 2.
- Although not necessary, it is additionally recommended that all power supplies are powered-up/down together in a controlled way, as tight to each other as possible.
- Additionally, regarding the ADC reference voltage VAREF0:
  - VAREF0 must power-up at the same time or later then VDDM, and
  - VAREF0 must power-down either earlier or at latest to satisfy the condition VAREF0 < VDDM + 0.5 V. This is required in order to prevent discharge of VAREF0 filter capacitance through the ESD diodes through the VDDM power supply. In case of discharging the reference capacitance through the ESD diodes, the current must be lower than 5 mA.

### 5.3.4 Power Sequencing all Voltages supplied from External

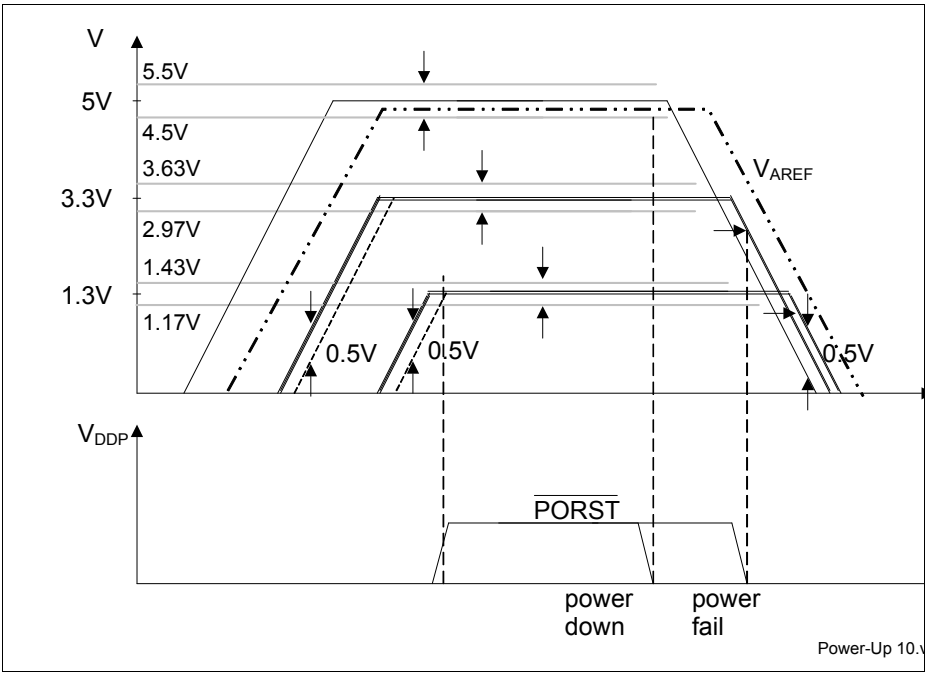



**Figure 11 5 V / 3.3 V / 1.3 V Power-Up/Down Sequence**

P0.4 and P0.5 should be kept at the selected setting until external supplied voltage has reached its operating level.

The following list of rules applies to the power-up/down sequence:

- All ground pins $V_{SS}$ must be externally connected to one single star point in the system. Regarding the DC current component, all ground pins are internally directly connected.
- At any moment in time to avoid increased latch-up risk,
  each power supply must be higher then any lower_power_supply - 0.5 V, or:
  VDD5 > VDDP - 0.5 V; VDD5 > VDD - 0.5 V;VDDP > VDD - 0.5 V, see **Figure 11**.
  – The latch-up risk is minimized if the I/O currents are limited to:
  – 20 mA for one pin group
  – AND 100 mA for the completed device I/Os
  – AND additionally before power-up / after power-down:
  1 mA for one pin in inactive mode (0 V on all power supplies)

- During power-up and power-down, the voltage difference between the power supply pins of the same voltage (3.3 V, 1.3 V, and 5 V) with different names, that are internally connected via diodes, must be lower than 100 mV. On the other hand, all power supply pins with the same name (for example all VDDP), are internally directly connected. It is recommended that the power pins of the same voltage are driven by a single power supply.
- The PORST signal may be deactivated after all VDD5, VDDP, VDD, and VAREF0 power-supplies and the oscillator have reached stable operation, within the normal operating conditions.
- At normal power down the PORST signal should be activated within the normal operating range, and then the power supplies may be switched off. Care must be taken that all Flash write or delete sequences have been completed.
- At power fail the PORST signal must be activated at latest when any 3.3 V or 1.3 V power supply voltage falls 10% below the nominal level. If, under these conditions, the PORST is activated during a Flash write, only the memory row that was the target of the write at the moment of the power loss will contain unreliable content. In order to ensure clean power-down behavior, the PORST signal should be activated as close as possible to the normal operating voltage range.
- In case of a power-loss at any power-supply, all power supplies must be powered-down, conforming at the same time to the rules number 2 and 4.
- Although not necessary, it is additionally recommended that all power supplies are powered-up/down together in a controlled way, as tight to each other as possible.
- Additionally, regarding the ADC reference voltage VAREF0:
  – VAREF0 must power-up at the same time or later then VDDM, and
  – VAREF0 must power-down either earlier or at latest to satisfy the condition VAREF0 < VDDM + 0.5 V. This is required in order to prevent discharge of VAREF0 filter capacitance through the ESD diodes through the VDDM power supply. In case of discharging the reference capacitance through the ESD diodes, the current must be lower than 5 mA.

### 5.3.5 Power, Pad and Reset Timing

**Table 27 Reset Timings Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Application Reset Boot Time[1)2)] | $t_B$ CC | 150 | – | 810 | µs | |
| Power on Reset Boot Time[3)4)] | $t_{BP}$ CC | – | – | 2.5 | ms | |
| EVR Startup time from Supply ramp-up till PORST release | $t_{EVR}$ CC | – | 860 | 1100 | µs | |
| HWCFG pins hold time from ESR0 rising edge | $t_{HDH}$ SR | 16 / $f_{FPI}$ | – | – | ns | |
| HWCFG pins setup time to ESR0 rising edge | $t_{HDS}$ CC | 0 | – | – | ns | |
| Ports inactive after ESR0 reset active | $t_{PI}$ CC | – | – | 8/$f_{FPI}$ | ns | |
| Ports inactive after PORST reset active[5)] | $t_{PIP}$ CC | – | – | 150 | ns | |
| Minimum PORST active time after power supplies are stable at operating levels | $t_{POA}$ CC | 4.5 | – | – | ms | 6) |
| $\overline{\text{TESTMODE}}$ / $\overline{\text{TRST}}$ hold time from PORST rising edge | $t_{POH}$ SR | 100 | – | – | ns | |
| PORST rise time | $t_{POR}$ SR | – | – | 50 | ms | |

**Table 27 Reset Timings Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $\overline{\text{TESTMODE}}$ / $\overline{\text{TRST}}$ setup time to PORST rising edge | $t_{POS}$ SR | 0 | – | – | ns | |
| Application Reset inactive after PORST deassertion | $t_{POR\_APP}$ SR | – | – | 40 [7] | µs | |

1) The duration of the boot time is defined between the rising edge of the internal application reset and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.

2) The given time includes the time of the internal reset extension for a configured value of SCU_RSTCNTCON.RELSA = 0x05BE.

3) The duration of the boot time is defined between the rising edge of the $\overline{\text{PORST}}$ and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.

4) The given time includes the internal reset extension time for the System and Application Reset which is visible through ESR0.

5) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.

6) This parameter represents the additional time required to ensure that external crystal is stable and operational at $\overline{\text{PORST}}$.

7) Application Reset is assumed not to be extended from external, otherwise the time extends by the time the Application Reset is extended.

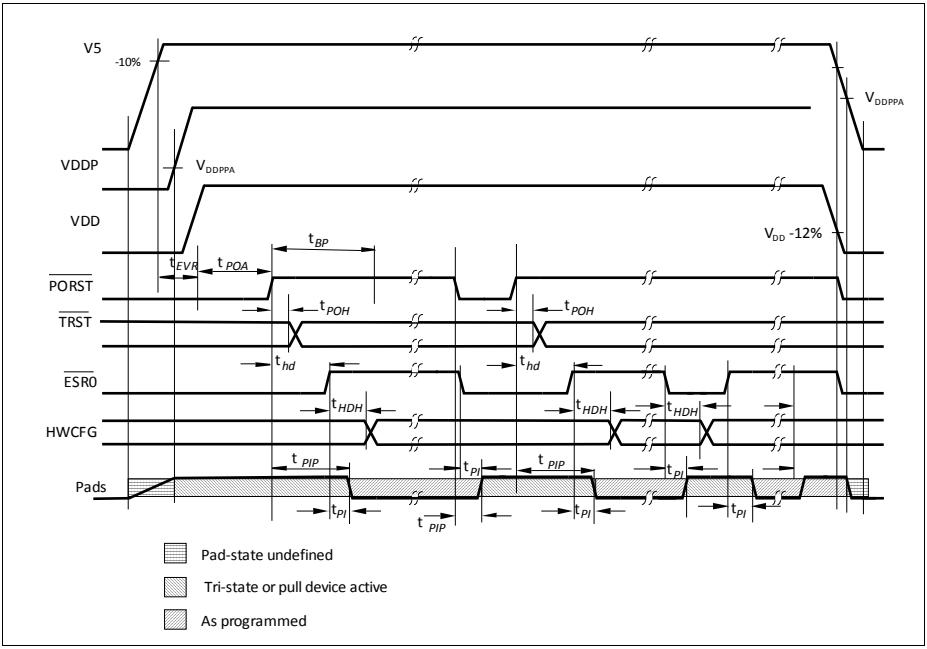



**Figure 12 Power, Pad and Reset Timing**

### 5.3.6 EVR Parameter

**Table 28 Pass device detector**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Pull-up current at VDPG | $I_{PU\_VDPG}$ SR | 0.7 | – | 2.0 | mA | $V_{DD5} \geq$ 4.5V; $V_{DD5} \leq$ 5.5V |
| Input low voltage | $V_{IL}$ SR | 0 | – | 1.5 | V | |

**Table 29 EVR Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output Capacitance on $V_{DDP}$ | $C_{OUT33}$ CC | – | 6.8 | – | µF | $I_{LOAD}$ > 310 mA; ESR < 50mΩ;a with external pass device, additional decoupling capacitor on each supply pin |
| Output Capacitance on $V_{DD}$ | $C_{OUT13}$ CC | – | 6.8 | – | µF | $I_{LOAD}$ < 250 mA; ESR < 50mΩ; additional decoupling capacitor on each supply pin |
| Input Capacitance on $V_5$ | $C_{IN5}$ CC | – | 6.8 | – | µF | depending on ext. regulator |
| Undervoltage Reset threshold for external supply | $V_{RST5}$ CC | – | – | 2.97 | V | 3.3V single supply |
| | | – | – | 4.5 | V | 5.0 single supply |
| Output accuracy of EVR33 after trimming | $\Delta V_{OUT33}$ CC | -80 | – | +80 | mV | $4.5 \leq V_{IN} \leq 5.5V$; $1\ mA \leq I_{OUT} \leq 310mA$ |
| Dynamic Load Regulation of EVR33 | $\Delta V_{LOREG33}$ CC | -225 | – | +225 | mV | dI / dt = 150mA /10 ns |

**Table 29 EVR Parameters** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Dynamic Line Regulation of EVR33 | $\Delta V_{LIREG\_33}$ CC | -25 | – | +25 | mV | dV5 / dt = 1V / ms<br>1 … 310mA,<br>4.5V … 5.5V |
| Undervoltage Reset threshold for EVR33 | $V_{RST33}$ CC | – | – | 2.97 | V | |
| Current drawn from EVR33 for external devices with internal pass devices. | $EXI_{33}$ SR | – | – | 30 | mA | No inductive loads allowed.<br>Decoupling capacitor > 330 nF |
| Output accuracy of EVR13 after trimming | $\Delta V_{OUT13}$ CC | -30 | – | +30 | mV | 2.97V ≤ $V_{IN}$ ≤ 3.63V;<br>1 mA ≤ $I_{OUT}$ ≤ 250mA |
| Dynamic Load Regulation of EVR13 | $\Delta V_{LOREG\_13}$ CC | -100 | – | +100 | mV | 5.0V/3.3V single supply,<br>dI / dt = 150mA /10 ns |
| Dynamic Line Regulation of EVR13 | $\Delta V_{LIREG\_13}$ CC | -10 | – | +10 | mV | 5.0V/3.3V single supply,<br>dV5 / dt=1V / ms<br>1 … 250mA, 2.97V … 3.63V |
| Undervoltage Reset threshold for EVR13 | $V_{RST13}$ CC | – | – | 1.17 | V | |
| Current drawn from EVR13 for external devices | $EXI_{13}$ SR | – | – | 10 | mA | No inductive loads allowed.<br>Decoupling capacitor > 100 nF |
| Supply ramp-up | $SR$ SR | – | – | 50 | V/ms | |

### 5.3.7 Phase Locked Loop (PLL)

**Table 30 PLL_SysClk Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Accumulated Jitter | $D_P$ | CC | -7 | – | 7 | ns | |
| PLL base frequency | $f_{PLLBASE}$ | CC | 50 | 200 | 320 | MHz | |
| VCO input frequency | $f_{REF}$ | CC | 8 | – | 16 | MHz | |
| VCO frequency range | $f_{VCO}$ | CC | 400 | – | 720 | MHz | |
| PLL lock-in time | $t_L$ | CC | 14 | – | 200 | µs | N > 32 |
| | | | 14 | – | 400 | µs | N ≤ 32 |

**Phase Locked Loop Operation**

When PLL operation is enabled and configured, the PLL clock $f_{VCO}$ (and with it the LMB-Bus clock $f_{LMB}$) is constantly adjusted to the selected frequency. The PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or clock source), resulting in an accumulated jitter that is limited. This means that the relative deviation for periods of more than one clock cycle is lower than for a single clock cycle.

This is especially important for bus cycles using wait states and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

Two formulas are defined for the (absolute) approximate maximum value of jitter $D_m$ in [ns] dependent on the K2 - factor, the LMB clock frequency $f_{LMB}$ in [MHz], and the number $m$ of consecutive $f_{LMB}$ clock periods.

$$\text{for} \quad (K2 \le 100) \quad \text{and} \quad (m \le (f_{LMB}[MHz])/2)$$

$$|Dm[ns]| = \left(\frac{740}{K2 \times f_{LMB}[MHz]} + 5\right) \times \left(\frac{(1 - 0,01 \times K2) \times (m - 1)}{0,5 \times f_{LMB}[MHz] - 1} + 0,01 \times K2\right) \quad (6)$$

$$\text{else} \quad |Dm[ns]| = \frac{740}{K2 \times f_{LMB}[MHz]} + 5 \quad (7)$$

With rising number $m$ of clock cycles the maximum jitter increases linearly up to a value of $m$ that is defined by the K2-factor of the PLL. Beyond this value of $m$ the maximum accumulated jitter remains at a constant value. Further, a lower LMB-Bus clock frequency $f_{LMB}$ results in a higher absolute maximum jitter value.

*Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L$ = 20 pF with the maximum driver and sharp edge.*

### Oscillator Watchdog (OSC_WDT)

The expected input frequency is selected via the bit field SCU_OSCCON.OSCVAL. The OSC_WDT checks for too low frequencies and for too high frequencies.

The frequency that is monitored is $f_{OSCREF}$ which is derived for $f_{OSC}$.

(8)

$$f_{OSCREF} = \frac{f_{OSC}}{OSCVAL + 1}$$

The divider value SCU_OSCCON.OSCVAL has to be selected in a way that $f_{OSCREF}$ is 2.5 MHz.

*Note: $f_{OSCREF}$ has to be within the range of 2 MHz to 3 MHz and should be as close as possible to 2.5 MHz.*

The monitored frequency is too low if it is below 1.25 MHz and too high if it is above 7.5 MHz. This leads to the following two conditions:

- Too low: $f_{OSC}$ < 1.25 MHz × (SCU_OSCCON.OSCVAL+1)
- Too high: $f_{OSC}$ > 7.5 MHz × (SCU_OSCCON.OSCVAL+1)

*Note: The accuracy is 30% for these boundaries.*

### 5.3.8 ERAY Phase Locked Loop (ERAY_PLL)

**Table 31 PLL_ERAY Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Accumulated jitter at SYSCLK pin | $D_{PP}$ | CC | -0.8 | – | 0.8 | ns | |
| Accumulated_Jitter | $D_P$ | CC | -0.5 | – | 0.5 | ns | |
| PLL Base Frequency of the ERAY PLL | $f_{PLLBASE\_ERAY}$ | CC | 50 | 250 | 360 | MHz | |
| VCO input frequency of the ERAY PLL | $f_{REF}$ | CC | 20 | – | 40 | MHz | |
| VCO frequency range of the ERAY PLL | $f_{VCO\_ERAY}$ | CC | 450 | – | 500 | MHz | |
| PLL lock-in time | $t_L$ | CC | 5.6 | – | 200 | µs | |

*Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L$ = 20 pF with the maximum driver and sharp edge.*

### 5.3.9 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

**Table 32 JTAG Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TCK clock period | $t_1$ SR | 25 | – | – | ns | |
| TCK high time | $t_2$ SR | 10 | – | – | ns | |
| TCK low time | $t_3$ SR | 10 | – | – | ns | |
| TCK clock rise time | $t_4$ SR | – | – | 4 | ns | |
| TCK clock fall time | $t_5$ SR | – | – | 4 | ns | |
| TDI/TMS setup to TCK rising edge | $t_6$ SR | 6.0 | – | – | ns | |
| TDI/TMS hold after TCK rising edge | $t_7$ SR | 6.0 | – | – | ns | |
| TDO valid after TCK falling edge[1] | $t_8$ CC | 3.0 | – | – | ns | $C_L$= 20 pF |
| | | – | – | 13 | ns | $C_L$=50 pF |
| TDO high impedance to valid from TCK falling edge[2] | $t_9$ CC | – | – | 14 | ns | $C_L$= 50 pF |
| TDO valid output to high impedance from TCK falling edge | $t_{10}$ CC | – | – | 13.5 | ns | $C_L$= 50 pF |
| TDO hold after TCK falling edge | $t_{18}$ CC | 2 | – | – | ns | |

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

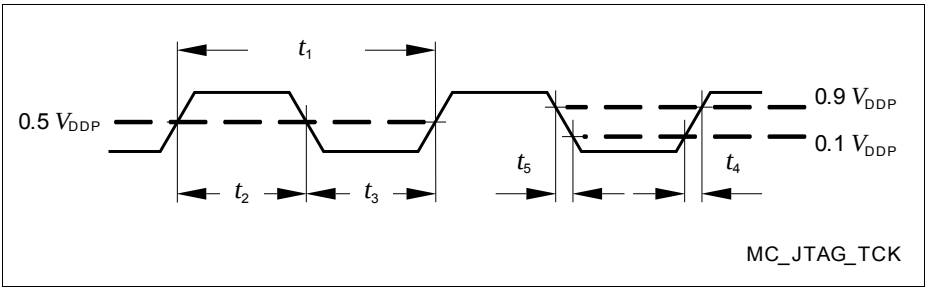



**Figure 13 Test Clock Timing (TCK)**

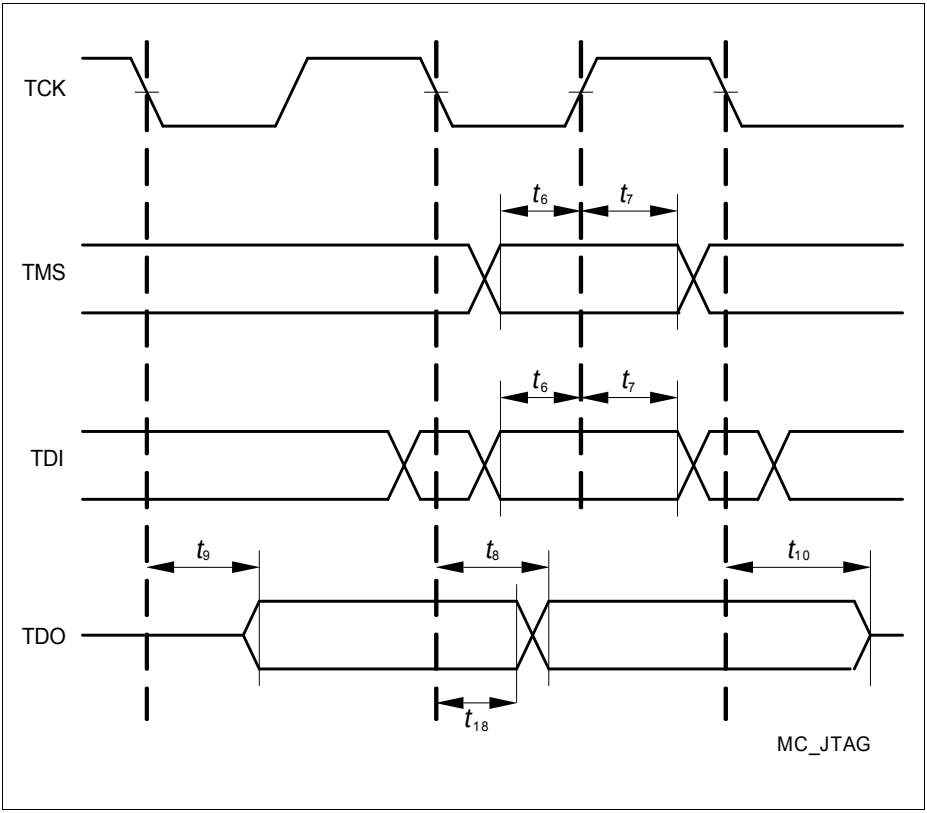



**Figure 14 JTAG Timing**

### 5.3.10 DAP Interface Timing

The following parameters are applicable for communication through the DAP debug interface.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

**Table 33 DAP Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| DAP0 clock period[1] | $t_{TCK}$ SR | 12.5 | – | – | ns | |
| DAP0 high time | $t_{12}$ SR | 4 | – | – | ns | |
| DAP0 low time[1] | $t_{13}$ SR | 4 | – | – | ns | |
| DAP0 clock rise time | $t_{14}$ SR | – | – | 2 | ns | |
| DAP0 clock fall time | $t_{15}$ SR | – | – | 2 | ns | |
| DAP1 setup to DAP0 rising edge | $t_{16}$ SR | 6.0 | – | – | ns | |
| DAP1 hold after DAP0 rising edge | $t_{17}$ SR | 6.0 | – | – | ns | |
| DAP1 valid per DAP0 clock period[2] | $t_{19}$ CC | 8 | – | – | ns | $C_L$= 20 pF; $f$= 80 MHz |
| | | 10 | – | – | ns | $C_L$= 50 pF; $f$= 40 MHz |

1) See the DAP chapter for clock rate restrictions in the Active::IDLE protocol state.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

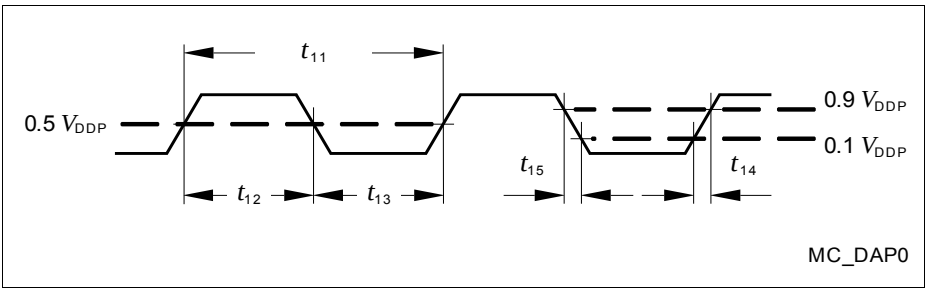



**Figure 15 Test Clock Timing (DAP0)**

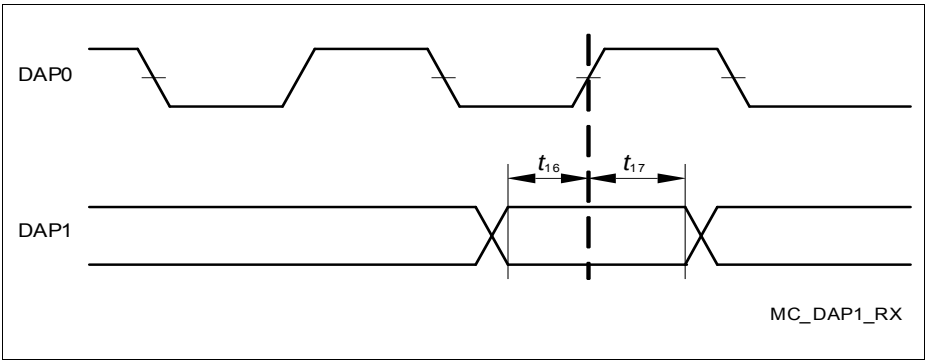



**Figure 16 DAP Timing Host to Device**

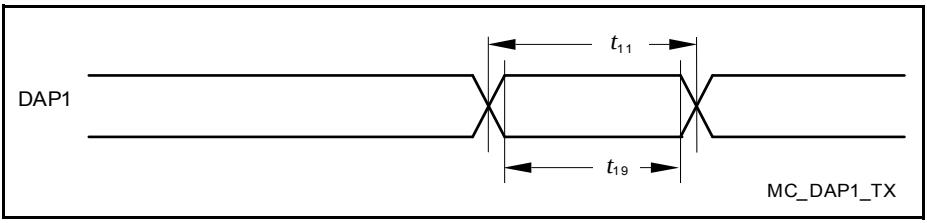



**Figure 17 DAP Timing Device to Host**

### 5.3.11 Peripheral Timings

*Note: Peripheral timings are not subjected to production test. They are verified by design / characterization.*

#### 5.3.11.1 Micro Link Interface (MLI) Timing

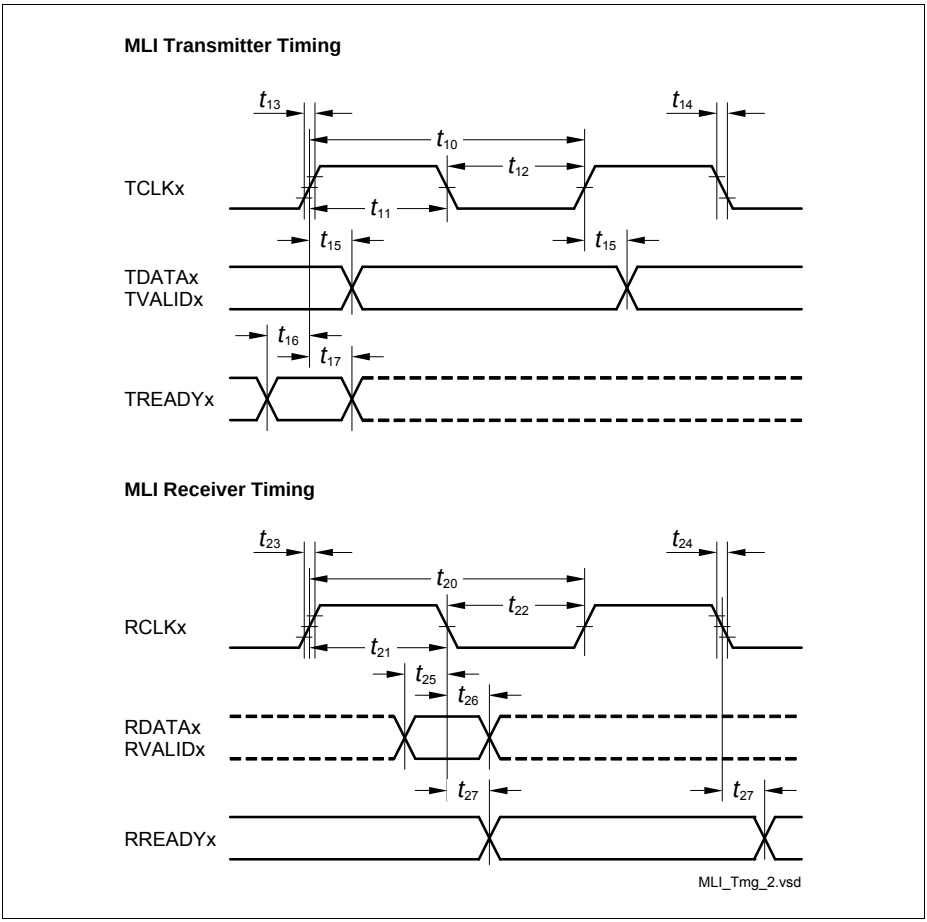



**Figure 18 MLI Interface Timing**

*Note: The generation of RREADYx is in the input clock domain of the receiver. The reception of TREADYx is asynchronous to TCLKx.*

The MLI parameters are valid for $C_L$ = 50 pF, strong driver medium edge.

**Table 34 MLI Receiver**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| RCLK clock period | $t_{20}$ SR | 1 / $f_{FPI}$ | – | – | ns | |
| RCLK high time[1)2)] | $t_{21}$ SR | – | 0.5 x $t_{20}$ | – | ns | |
| RCLK low time[1)2)] | $t_{22}$ SR | – | 0.5 x $t_{20}$ | – | ns | |
| RCLK rise time[3)] | $t_{23}$ SR | – | – | 4 | ns | |
| RCLK fall time[3)] | $t_{24}$ SR | – | – | 4 | ns | |
| RDATA/RVALID setup time before RCLK falling edge | $t_{25}$ SR | 4.2 | – | – | ns | |
| RDATA/RVALID hold time after RCLK falling edge | $t_{26}$ SR | 2.2 | – | – | ns | |
| RREADY output delay time | $t_{27}$ SR | 0 | – | 16 | ns | |

1) The following formula is valid: t21 + t22 = t20.

2) Min and Max values for this parameter can be derived from the typ. value by considering the other receiver timing parameters.

3) The RCLK max. input rise/fall times are best case parameters for fFPImax. For reduction of EMI, slower input signal rise/fall times can be used for longer RCLK clock periods.

**Table 35 MLI Transmitter**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TCLK clock period | $t_{10}$ CC | 2 x 1 / $f_{FPI}$ | – | – | ns | |
| TCLK high time[1)2)] | $t_{11}$ CC | 0.45 x $t_{10}$ | 0.5 x $t_{10}$ | 0.55 x $t_{10}$ | ns | |
| TCLK low time[1)2)] | $t_{12}$ CC | 0.45 x $t_{10}$ | 0.5 x $t_{10}$ | 0.55 x $t_{10}$ | ns | |

**Table 35 MLI Transmitter**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| TCLK rise time | $t_{13}$ CC | – | – | 0.3 x $t_{10}$[3] | ns | |
| TCLK fall time | $t_{14}$ CC | – | – | 0.3 x $t_{10}$[3] | ns | |
| TDATA/TVALID output delay time | $t_{15}$ CC | -3 | – | 4.4 | ns | |
| TREADY setup time before TCLK rising edge | $t_{16}$ SR | 18 | – | – | ns | |
| TREADY hold time after TCLK rising edge | $t_{17}$ SR | -2 | – | – | ns | |

1) The following formula is valid: t11 + t12 = t10.

2) The min./max. TCLK low/high times t11/t12 include the PLL jitter of fSYS. Fractional divider settings must be regarded additionally to t11 / t12.

3) For high-speed MLI interface, strong driver sharp or medium edge selection (class A2 pad) is recommended for TCLK.

### 5.3.11.2 Micro Second Channel (MSC) Interface Timing

The MSC parameters are valid for $C_L$ = 50 pF.

**Table 36 MSC Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| FCLP clock period[1)2)] | $t_{40}$ CC | 2 x $T_{MSC}$[3)] | – | – | ns | |

**Table 36 MSC Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SOP[4]/ENx outputs delay from FCLP[4] rising edge | $t_{45}$ CC | -2 | – | 5 | ns | ENx with strong driver and sharp (minus ) edge; LVDS mode |
| | | -5 | – | 5 | ns | ENx with strong driver and sharp (minus ) edge; CMOS mode |
| | | -2 | – | 10 | ns | ENx with strong driver and medium (minus) edge |
| | | 0 | – | 21 | ns | ENx with strong driver and soft edge |
| SDI bit time | $t_{46}$ CC | 8 x $T_{MSC}$ | – | – | ns | |
| SDI rise time | $t_{48}$ SR | – | – | 200 | ns | |
| SDI fall time | $t_{49}$ SR | – | – | 200 | ns | |

1) FCLP signal rise/fall times are only defined by the pad rise/fall times.

2) FCLP signal high and low can be minimum 1 / TMSC

3) TMSC = TSYS = 1 / fSYS.

4) SOP / FCLP either propagated by LVDS or by CMOS strong driver and non soft edge.

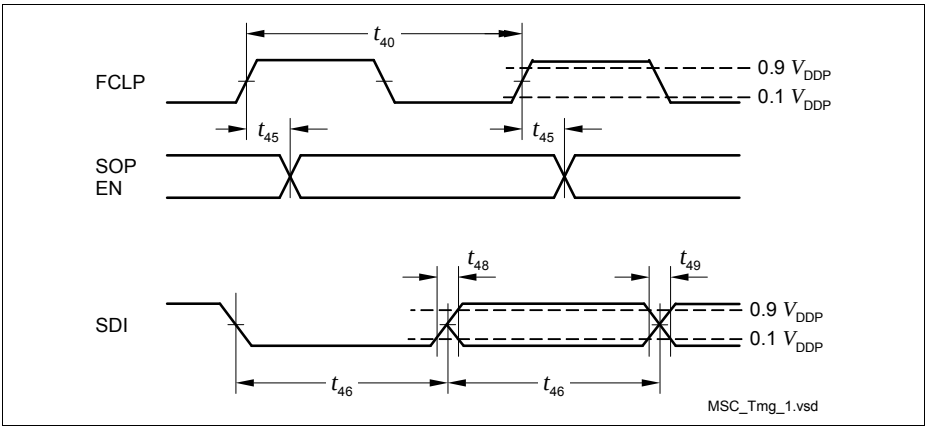



**Figure 19 MSC Interface Timing**

*Note: The data at SOP should be sampled with the falling edge of FCLP in the target device.*

### 5.3.11.3 SSC Master/Slave Mode Timing

The SSC parameters are valid for $C_L$ = 50 pF, strong driver medium edge.

**Table 37 Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| SCLK clock period[1)2)3)] | $t_{50}$ CC | 2 x 1 / $f_{FPI}$ | – | – | ns | |
| MTSR/SLSOx delay from SCLK rising edge | $t_{51}$ CC | 0 | – | 8 | ns | |
| MRST setup to SCLK latching edge[3)] | $t_{52}$ SR | 16.5 | – | – | ns | |
| MRST hold from SCLK latching edge[3)] | $t_{53}$ SR | 0 | – | – | ns | |
| SCLK input clock period[1)3)] | $t_{54}$ SR | 4 x 1 / $f_{FPI}$ | – | – | ns | |
| SCLK input clock duty cycle | $t_{55}$_$t_{54}$ SR | 45 | – | 55 | % | |
| MTSR setup to SCLK latching edge[3)4)] | $t_{56}$ SR | 1 / $f_{FPI}$ + 1 | – | – | ns | |
| MTSR hold from SCLK latching edge | $t_{57}$ SR | 1 / $f_{FPI}$ + 5 | – | – | ns | |
| SLSI setup to first SCLK latching edge | $t_{58}$ SR | 1 / $f_{FPI}$ + 5 | – | – | ns | |
| SLSI hold from last SCLK latching edge[5)] | $t_{59}$ SR | 7 | – | – | ns | |
| MRST delay from SCLK shift edge | $t_{60}$ CC | 0 | – | 16.5 | ns | |
| SLSI to valid data on MRST | $t_{61}$ CC | – | – | 16.5 | ns | |

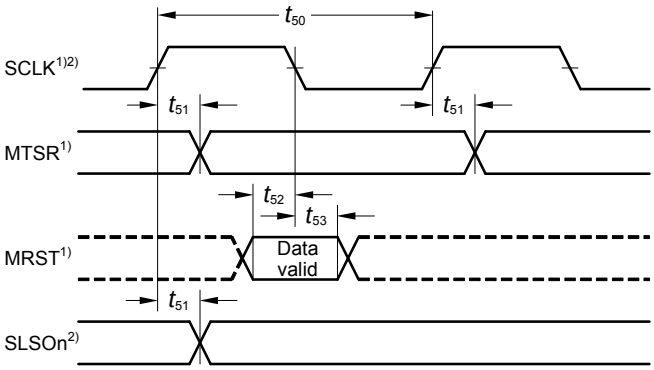
1) SCLK signal rise/fall times are the same as the rise/fall times of the pad.

2) SCLK signal high and low times can be minimum 1xT.

3) Tmin = TSYS = 1/fSYS.

4) Fractional divider switched off, internal baud rate generation used.

5) For CON.PH=1 slave select must not be removed before the following shifting edge. This mean, that what ever is configured (shifting / latching first), SLSI must not be de-actived before the last trailing edge from the pair of shifting / latching edges.




1) This timing is based on the following setup: CON.PH = CON.PO = 0.

2) The transition at SLSOn is based on the following setup: SSOTC.TRAIL = 0 and the first SCLK high pulse is in the first one of a transmission.

SSC_TmgMM

**Figure 20 Master Mode Timing**

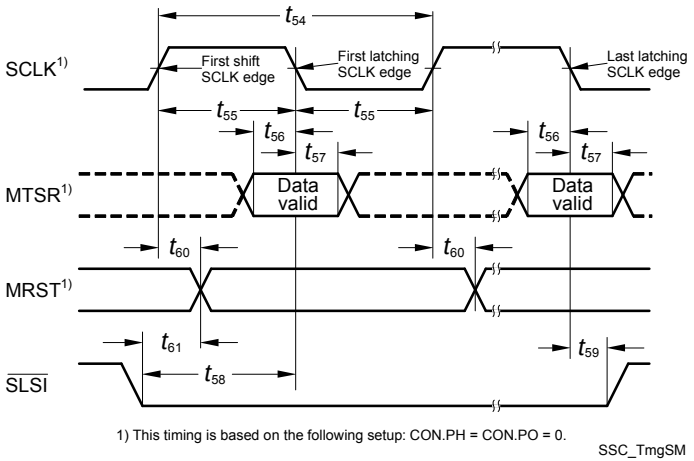



**Figure 21 Slave Mode Timing**

### 5.3.11.4 ERAY Interface Timing

The timings of this section are valid for the strong driver and either sharp edge or medium edge settings of the output drivers with $C_L$ = 25 pF.

The ERAY interface is only available for SAK-TC1728F-192F133HR / SAK-TC1728F-192F133HR.

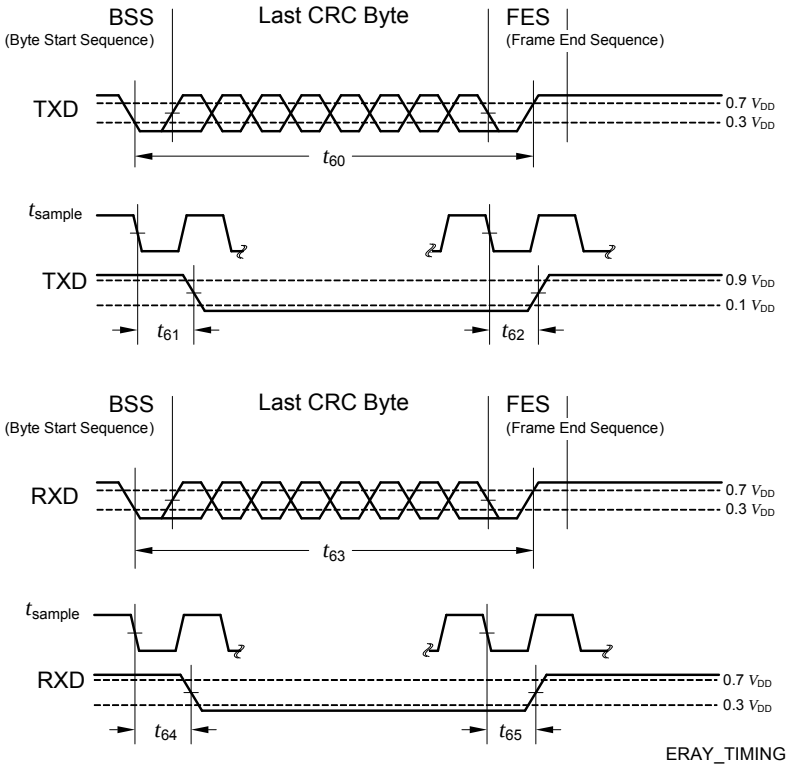



**Figure 22 ERAY Timing**

## 5.4 Package and Reliability

### 5.4.1 Package Parameters

**Table 38 Thermal Characteristics of the Package**

| Device | Package | RΘJCT 1) | RΘJCB 1) | RΘJCL 1) | Unit | Note |
|---|---|---|---|---|---|---|
| TC1728 | PG-LQFP-176-6 | 7.6 | 0.6 | 32.5 | K/W | |

1) The top and bottom thermal resistances between the case and the ambient ($R_{TCAT}$, $R_{TCAB}$) are to be combined with the thermal resistances between the junction and the case given above ($R_{TJCT}$, $R_{TJCB}$), in order to calculate the total thermal resistance between the junction and the ambient ($R_{TJA}$). The thermal resistances between the case and the ambient ($R_{TCAT}$, $R_{TCAB}$) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the $R_{TJA}$ is the total thermal resistance between the junction and the ambient. This total junction ambient resistance $R_{TJA}$ can be obtained from the upper four partial thermal resistances.

### 5.4.2 Package Outline

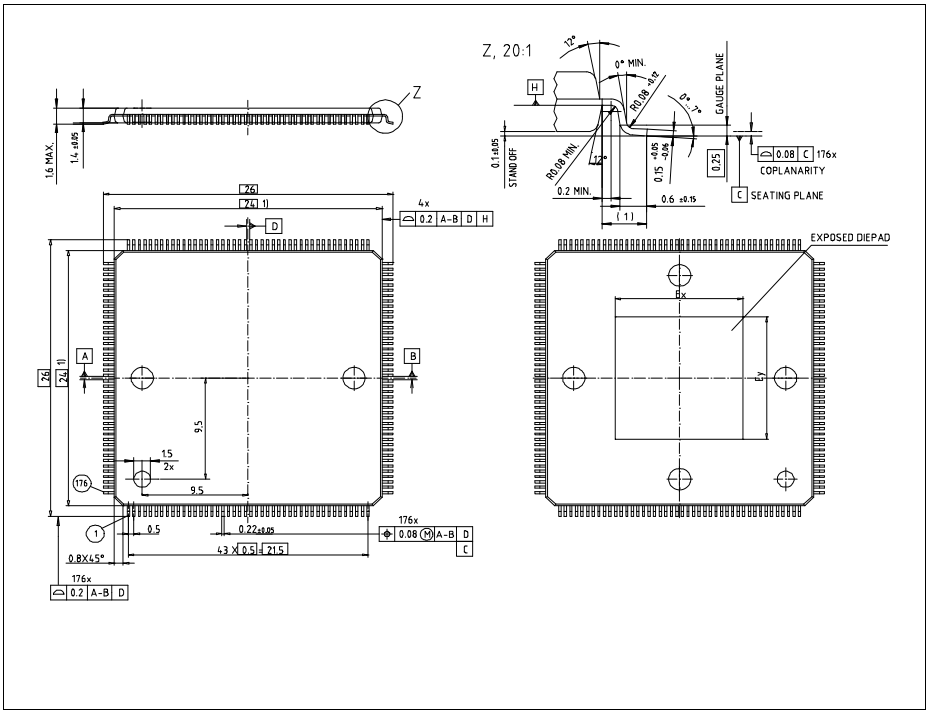



**Figure 23 Package Outlines PG-LQFP-176-6**

**Table 39 Exposed pad Dimensions**

| | |
|---|---|
| **Ex** | **7.5 mm** |
| **Ey** | **7.5 mm** |

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

### 5.4.3 Flash Memory Parameters

The data retention time of the TC1728’s Flash memory depends on the number of times the Flash memory has been erased and programmed.

**Table 40 FLASH32 Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Data Flash Erase Time per Sector | $t_{ERD}$ | CC | – | – | 3[1)] | s | |
| Program Flash Erase Time per 256 KByte Sector | $t_{ERP}$ | CC | – | – | 5 | s | |
| Program time data flash per page[2)] | $t_{PRD}$ | CC | – | – | 5.3 | ms | without reprogramming |
| | | | – | – | 15.9 | ms | with two reprogramming cycles |
| Program time program flash per page[3)] | $t_{PRP}$ | CC | – | – | 5.3 | ms | without reprogramming |
| | | | – | – | 10.6 | ms | with one reprogramming cycle |
| Data Flash Endurance | $N_E$ | CC | 60000 [4)] | – | – | cycles | Min. data retention 5 years |
| Erase suspend delay | $t_{FL\_ErSusp}$ | CC | – | – | 15 | ms | |
| Wait time after margin change | $t_{FL\_MarginDel}$ | SR | 10 | – | – | µs | |
| Program Flash Retention Time, Physical Sector[5)6)] | $t_{RET}$ | CC | 20 | – | – | years | Max. 1000 erase/ program cycles |
| Program Flash Retention Time, Logical Sector[5)6)] | $t_{RETL}$ | CC | 20 | – | – | years | Max. 100 erase/ program cycles |
| UCB Retention Time[5)6)] | $t_{RTU}$ | CC | 20 | – | – | years | Max. 4 erase/ program cycles per UCB |
| Wake-Up time[2)] | $t_{WU}$ | CC | – | – | 270 | µs | |

**Table 40 FLASH32 Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| DFlash wait state configuration | $WS_{DF}$ | SR | $50ns \times f_{LMB}$ | – | – | | |
| PFlash wait state configuration | $WS_{PF}$ | SR | $26ns \times f_{LMB}$ | – | – | | |

1) In case of wordline oriented defects (see robust EEPROM emulation in the User's Manual) this erase time can increase by up to 100%.

2) In case the Program Verify feature detects weak bits, these bits will be programmed up to twice more. Each reprogramming takes additional 5 ms.

3) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes additional 5 ms.

4) Only valid when a robust EEPROM emulation algorithm is used. For more details see the User´s Manual.

5) Storage and inactive time included.

6) At average weighted junction temperature $T_j$ = 100°C, or the retention time at average weighted temperature of $T_j$ = 110°C is minimum 10 years, or the retention time at average weighted temperature of $T_j$ = 150°C is minimum 0.7 years.

## 5.4.4 Quality Declarations

**Table 41 Quality Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operation Lifetime[1)] | $t_{OP}$ | – | – | 24000 | hours | –[2)] |
| ESD susceptibility according to Human Body Model (HBM) | $V_{HBM}$ | – | – | 2000 | V | Conforming to JESD22-A114-B |
| ESD susceptibility of the LVDS pins | $V_{HBM1}$ | – | – | 500 | V | – |
| ESD susceptibility according to Charged Device Model (CDM) | $V_{CDM}$ | – | – | 500 | V | Conforming to JESD22-C101-C |
| Moisture Sensitivity Level | MSL | – | – | 3 | – | Conforming to Jedec J-STD-020C for 240°C |

1) This lifetime refers only to the time when the device is powered on.
2) For worst-case temperature profile equivalent to:
   1200 hours at $T_j$ = 125...160°C
   3600 hours at $T_j$ = 110...125°C
   7200 hours at $T_j$ = 100...110°C
   11000 hours at $T_j$ = 25...110°C
   1000 hours at $T_j$ = -40...25°C

# 6 Revision History

Changes from V0.3 to V0.4D1

- Operating Conditions
  - Added footnote 3 and 4
  - Updated $K_{OVAN}$ and $K_{OVAP}$ max values
  - Added $f_{CPU}$, $f_{LMB}$, $f_{PCP}$, $f_{FPI}$max for SAK-TC1724F-192F133HL, SAK-TC1724F-192F133HR, SAK-TC1724N-192F80HR, SAK-TC1724N-128F80HR.
  - Updated limits for $V_{DD,}$ $V_{DDM,}$ $V_{DDP}$.
  - Added $I_{IN,}$ $\Sigma I_{IN}$
  - Updated $\Sigma I_{SC\_PG}$
- Standard Pad Class A1
  - Changed $R_{DSON1}$ *to* $R_{DSONM}$, added new condition “PMOS” for 140ohms, added a new condition for “NMOS” with a max value of 100ohms
  - Added $R_{DSONW}$
  - Changed min value of $V_{IHA1}$ to 0.6 x $V_{DDP}$
  - Changed min value of $V_{ILA1}$ / $V_{IHA1}$ to 0.6
- Standard Pad Class A1+
  - Added HYSA1+
  - Added $V_{ILA1+}$ / $V_{IHA1+}$
  - Added $R_{DSONW}$, $R_{DSONM}$
  - $R_{DSON1+}$, added new condition “PMOS” for 85ohms, added a new condition for “NMOS” with a max value of 70ohms
  - Changed min value of $V_{IHA1+}$ to 0.6 x $V_{DDP}$
  - Deleted -2000nA to 2000nA limits for $I_{OZA1+}$
- Standard Pad Class A2
  - Added HYSA2
  - Added $R_{DSONW}$, $R_{DSONM}$
  - $R_{DSON2}$, added new condition “PMOS” for 25ohms, added a new condition for “NMOS” with a max value of 20ohms
  - $t_{FA2}$, added max 18000ns for CL=20000pF; pinout driver=medium, 65000ns for CL=20000pF;pinout driver=weak
  - $t_{RA2}$, removed 140ns for CL=150pF;pinout driver=weak
  - $t_{RA2}$, added 550ns for CL=150pF,pinout driver=weak, 18000ns for CL=20000pF, pinout driver=medium, 65000ns for CL=20000pF, pinoutdriver=weak
- Standard Pad Class F
  - Added HYSF
  - Changed min value of VIHF to 0.6 x VDDP
  - Added min value of $V_{ILF}$ / $V_{IHF}$ as 0.6
  - Added $R_{DSONW}$, $R_{DSONM}$
  - Deleted note for $t_{FF}$, $t_{RF}$
- Standard Pad Class I
  - Changed min value of $V_{IHI}$ to 0.6 x $V_{DDP}$

  - Changed min value of $V_{ILI}$ / $V_{IHI}$ as 0.6
- LVDS Pads
  - Removed input hysteresis F, HYSF
  - Added note “Parallel termination 100 Ohm +-1%” for $t_{FL}$, $t_{RL,}$ $t_{SET\_LVDS}$
- Standard Pad Class S
  - Changed max value of $V_{IHS}$ to 3.6
  - Changed min value of $V_{ILS}$ to 2.1
  - Added input leakage current, $I_{OZS}$
- ADC parameters
  - Changed typ value of $C_{AINSW}$ to 9pF
  - Changed typ value of $C_{AINTOT}$ to 20pF
  - Updated notes for $EA_{DNL}$,$EA_{GAIN}$,TUE,$EA_{INL}$,$EA_{OFF}$
  - Changed $f_{ADCI}$ to max 20MHz
  - Added $f_{ADC}$ of 110MHz where ffpimax=110MHz
  - Added $f_{ADC}$ of 80MHz where ffpimax=80MHz
  - Updated $f_{ADC}$ min of 4MHz
  - Added sample time, $t_S$, 2 to 255 tADCI
  - Added calibration time after reset, $t_{CAL}$ max 4352 cycles
  - Included footnote for TUE for 10-bit and 8-bit conversion
  - Removed $I_{AIN7T}$ (covered by $R_{AIN7T}$ )
  - Removed $I_{AREF}$, added $Q_{CONV}$
  - Updated notes for $I_{OZ2}$ and $I_{OZ3}$
  - Updated typ value of 900Ohm for $R_{AIN}$
- FADC parameters
  - Updated note for $EF_{GRAD}$
  - Updated *note for* $EF_{OFF}$
  - Added $f_{FADC}$ of 110MHz where ffpimax=110MHz
  - Added $f_{FADC}$ of 80MHz where ffpimax=80MHz
  - Added conversion time, $t_C$
  - Added analog input voltage range,$V_{AINF}$
- OSC XTAL parameters
  - Added $f_{OSC}$
  - Changed max value of $V_{IHX}$ to $V_{DDP}$+0.5V
  - Changed min value of $V_{ILX}$ to -0.5V
  - Added typ values for internal load capacitors, $C_{L0}$ to $C_{L3}$, 2.5pF, 2.5pF, 4pF, 6.5pF
  - Added HYSAX
- Power Supply parameters
  - Updated $I_{DDP,}$ $I_{DDM,}$ $I_{DDP\_FP}$
  - Added $I_{DD}$ for $f_{CPU}$=80MHz for max and realistic patterns
  - Updated PD values for max and real patterns, all external, $f_{CPU}$=133MHz
  - Added text to of $f_{CPU}$=133MHz to the note for the PD parameter.
  - Added PD for $f_{CPU}$=80Mhz for max and realistic patterns for both all external mode and 5V only with ext.pass device mode

  - Current consumption for LVDS pad pairs is updated for all LVDS pads in total
  - Deleted the redundant $I_{DDP}$
  - Updated $I_{DDP\_FP}$, $I_{DDP\_PORST}$, $I_{DD\_PORST}$
  - Deleted $R_{THJA}$ parameter
- Power Sequencing
  - Added Power Sequencing for 3.3V Supply Only section
- Power, Pad and Reset Timing parameters
  - Removed redundant note for $t_{HDH}$, $t_{HDS}$
  - Added text from note “TESTMODE/TRST” to the name of $t_{POH}$ and $t_{POS}$, deleted note
- EVR Parameters
  - Added $I_{PU\_VDPG}$, $V_{IH}$ and $V_{IL}$ parameters in Pass Device Detector Table
  - Added EVR Parameter Table
- PLL SYSCLK parameters
  - Changed max value for $f_{VCO}$
  - Added min value of 50us for $t_L$
  - Included formula 1 and 2
  - Removed note for peak-to-peak noise on pad supply voltage
- PLL ERAY parameters
  - Changed typ value to 250MHz for $f_{PLLBASE}$
  - Added min value of 50us for $t_L$
  - Removed note for peak-to-peak noise on pad supply voltage
- JTAG Interface parameters
  - Changed to ‘=’ signs in the notes for $t_8$, $t_9$ and $t_{10}$
- DAP parameters
- Peripheral Timings
  - Removed note for Peripheral Timings “Peripheral timing parameters are not subject to production test. They are verified by design/characterization.”
- MLI Timing
  - Added text for MLI parameters valid for CL=25pF
- MLI Receiver parameters
  - Changed $f_{SYS}$ to 110MHz in footnote 3
- MLI Tranmitter parameters
  - Changed $t_{13}$, TCLK rise time and $t_{14}$, TCLK fall time to 0.3 x t10
- MSC parameters
  - Added text for MSC parameters valid for CL=25pF
  - Added limits for different pad drive strength of $t_{45}$
- parameters
  - Changed min value of t$t_{52}$ to 16.5ns
- ERAY parameters
  - Changed min value of $t_{60}$
  - Changed max value of $t_{61}$-$t_{62}$
  - Changed min and max values of $t_{63}$

  - Changed max value of $t_{64}$-$t_{65}$
  - Added $dTxdly$, dRxdly
  - Updated ERAY timing figure
- Flash32 parameters
  - Updated $t_{PRD}$, $t_{PRP}$
  - Changed min value of $WS_{DF}$ to 50ns x $f_{LMB}$
  - Updated footnote 3
- Package parameters
  - Added $R_{THJCT}$, $R_{THJCB}$, $R_{THJCL}$ for LQFP144
- Package outline
  - Added package outline for LQFP176

Changes from V0.5 to V0.6

- Added max limit for $V_{RST5\ for\ 5.0V\ single\ supply}$
- Removed note above MLI Transmitter table
- Updated conditions for $t_{FL}$ and $t_{RL}$ for LVDS pad parameters
- Updated limits for $R_{DSONW}$ and $R_{DSONM}$ for Class A1 pads
- Updated limits for $R_{DSONW}$ and $R_{DSONM}$ and $R_{DSON1+}$ for Class A1+ pads
- Updated limits for $R_{DSONW}$ and $R_{DSONM}$ and $R_{DSON2}$ for Class A2 pads
- Updated limits for $R_{DSONW}$ and $R_{DSONM}$ for Class F pads
- Updated conditions for $t_{RF}$ and $t_{FF}$ for Class F pad parameters
- Added footnote 7 to ADC table
- Updated $Q_{CONV}$of ADC table
- Updated conditions to $t_L$ of PLL Sysclk
- Changed $t_{19}$ of DAP from SR to CC
- Removed condition for $V_5$
- Added FADC input circuit
- Updated max limit for $V_{AGND0}$ and min limit for $V_{AREF0}$
- $t_{BWG}$ and $t_{BWR}$ are added to ADC table
- Updated description of $t_{CAL}$
- Added a placeholder for $R_{AIN}$, $R_{AIN7T}$, $R_{AREF}$, $t_S$, $f_{ADCI}$, $EA_{DNL}$, $EA_{INL}$, $EA_{GAIN}$, $EA_{OFF}$, $TUE$ at a separate ADC table for $V_{DDM}$=3.3V
- Added a placeholder for $t_{AWAF}$, $t_{AWAS}$ to both ADC tables for $V_{DDM}$=5V *and* $V_{DDM}$=3.3V
- Added a placeholder for $t_{FWAF}$, $t_{FWAS}$ to FADC table for $V_{DDM}$=5V, $V_{DDM}$=3.3V
- Removed limits of gain=8 for $EF_{GRAD}$
- Added $V_{FAREFI}$ and $V_{FAGNDI}$ parameters
- Updated limit of $t_{SF2}$ to min 120ns
- Typo in Note for $I_{V5}$ at 80MHz is corrected.
- Updated max limit of $\Sigma I_{IN}$.
- Added $I_{IN}$.
- Added Pin Reliability in Overload subchapter.
- Removed sentence “Exposure to conditions within the maximum ratings will not affect device reliability.” Replaced with the Pin Reliability in Overload subchapter.

- Removed capacitance conditions for LVDS pad parameters, $t_{RL}$, $t_{FL}$ , loads defined by interface (MSC) timing.
- Updated max limits of Flash parameters $t_{PRD}$, $t_{PRP}$
- Updated representation of $I_{DDP}$
- Updated limits of $I_{DD\_PORST}$ to max 110mA
- Updated limits of $I_{DDP\_PORST}$ to max 6mA
- Updated limits of $I_{DD}$ for real pattern, $f_{CPU=133MHz}$, to max 212mA
- Added new parameter $I_{DDSUM}$
- Updated max limit of $I_{DDM}$ to 32mA
- Updated TC1728 $I_{V5}$ for max and real patterns, $f_{CPU=133MHz}$
- Updated $PD$ for real pattern, $f_{CPU=133MHz}$, all external supplies.
- Updated TC1728 $PD$ for max and real patterns, $f_{CPU=133MHz}$, 5V only with external pass device.
- Updated limit for $R_{DSON2}$ of A2 pad, P_MOS
- Updated limits for $R_{DSONM}$ of F pad, P_MOS, N_MOS
- Removed $V_{IH}$ for Pass Device Detector
- Updated limits for $V_{IL}$ of Pass Device Detector
- Updated limits and test conditions for $\Delta V_{LOREG33}$ and $\Delta V_{LIREG33}$
- Updated test condition for 5.0V single supply $\Delta V_{LOREG13}$
- Updated limits and test condition for 5.0V single supply $\Delta V_{LIREG13}$
- Corrected typ and max limits for $C_{OUT33}$ and $C_{OUT13}$
- Added limit and test condition for 3.3V single supply $\Delta V_{LOREG13}$ and $\Delta V_{LIREG13}$
- Application reset boot time limits are updated
- Added min limit for $I_{OZS}$
- Added a new parameter $V_{ILSD}$
- Updated limits for $t_{BP}$, $STT$
- Removed typical text from load of Peripheral Timing sections.
- Limits for $EF_{GRAD}$ with Gain=4 is changed to TBD
- Min limit for $V_{DDM}$ is changed to TBD
- Added $EF_{REFI}$
- Added a placeholder for $R_{FAIN}$, $EF_{DNL}$, $EF_{INL}$, $EF_{GRAD}$, $EF_{OFF}$ at a separate ADC table for $V_{DDM}$=3.3V
- Added max and typ limits for $R_{RAIN}$ for $V_{DDM}$=3.3V
- Updated limits of $P_D$ for real pattern, $f_{CPU=80MHz}$, to max 669mW
- Updated text for Note column of $N_E$
- Corrected typo for Class D pads in PN-Junction Characteristics for positive/negative overload tables
- Updated limits of $I_{DD}$ for max pattern, $f_{CPU=133MHz}$, to max 310mA
- Updated limits of $I_{DD}$ for max pattern, $f_{CPU=80MHz}$, to max 248mA
- Updated limits of $P_D$ for max pattern, $f_{CPU=133MHz}$, to max 902mA
- Updated limits of $I_{DD}$ for max pattern, $f_{CPU=80MHz}$, to max 810mA
- Corrected typo for $C_{OUT13}$
- Updated load jump current for $C_{OUT33}$ and $C_{OUT13}$ for $f_{CPU}$=80MHz
- Changed min to typ value for $C_{IN5}$

Changes from V0.6 to V0.7

- Name of package is updated

Changes from V0.7 to V0.8

- Absolute maximum rating section for is updated for $V_{DDP}$, $V_{IN}$, $V_{AIN}$, $V_{AREF0}$, $V_{AINF}$
- A footnote is added to $t_{ERD}$
- A note is added, updated pad supply levels in Pin Reliability in Overload section
- Updated min limit for $t_{17}$ of MLI
- Added a footnote to $I_{DDP}$
- Included text to power sequencing sections for setting of P0.4 and P0.5.
- Added limits for $EF_{DNL}$ for Gain= 4, 8
- Changed STT to $t_{EVR}$, updated Power, Pad and Reset Timing figure
- Changed min limit of $t_L$ for PLL_Sysclk timing
- Removed $I_{PU\_VDPG}$ for $V_{DD5}$≥2.97V, $V_{DD5}$£3.63V
- Updated limit and test condition for $C_{OUT33}$, $C_{OUT13}$
- Updated limit for $C_{IN5}$
- Updated limit and test condition for $\Delta V_{LOREG33}$
- Removed $PSRR_{33}$, $PSRR_{13}$
- Updated test condition for $\Delta V_{LOREG13}$
- Updated limit and test condition for $\Delta V_{LIREG13}$
- Updated min limit for MSC t45, strong sharp setting, CMOS mode
- Added $\Delta V_{OUT33}$, $\Delta V_{OUT13}$ parameters
- Updated first sentence for Chapter 5.3
- Added text for MLI and SSC parameters for validity of strong driver medium edge only
- Updated description for $t_{52}$ and $t_{53}$
- Changed SSC parameters from CC to SR for $t_{56}$, $t_{57}$, $t_{58}$, and $t_{59}$
- Changed min to max limit for EVR Supply ramp-up parameter
- Updated min limit for $I_{PU\_VDPG}$

Changes from V0.8 to V1.0

- Added limits for $EF_{GRAD}$ for Gain= 4, 8
- Added limits for $EF_{REFI}$
- Updated $V_{FAGNDI}$, $V_{FAREFI}$, changed from SR to CC
- A footnote is added for $V_{FAREFI}$
- Updated limit for $C_{IN5}$
- Added min limit for $V_5$
- Updated limits for $f_{ADCI}$, $t_{BWG}$, $t_{BWR}$ , $t_{AWAF}$, $t_{AWAS}$, $t_{FWAF}$, , $t_{FWAS}$
- Updated limits for ADC table, $V_{DDM}$=3.3V, $f_{ADCI}$, $t_{BWG}$, $t_{BWR}$ , $t_{AWAF}$, $t_{AWAS}$, $t_{FWAF}$, , $t_{FWAS}$, $R_{AIN7T}$, $EA_{DNL}$, $EA_{GAIN}$, $EA_{INL}$, , $EA_{OFF}$, $TUE$ , $Q_{CONV}$
- Corrected typo in test condition for $R_{DSON}$
- Removed $R_{DSONW}$ parameter for class F pads
- Removed footnote 2 from $\Sigma I_{SC\_D}$

- Added footnote 3 to $V_{DDM}$
- Updated max limit for ADC parameter $t_S$
- Added footnote 2 for $t_9$ of JTAG parameter
- Changed $t_{26}$, $t_{27}$ from CC to SR
- Updated max limit for ADC parameter $V_{AIN}$
- Added footnote 5 to $t_{59}$
- Added $t_{POR\_APP}$ parameter of Reset Timing parameters

Changes from V1.0 to V1.1

- Updated description for $t_{CAL}$
- Added a footnote to $Q_{CONV}$
- Added marking option SAK-TC1728F-192F133HR to Table 1,Summary of Features section
- Updated Figure 2, Figure 3-1, Figure 3-2
- Added identification registers in Table 4
- Updated $f_{CPU}$, $f_{FPI}$, $f_{LMB}$, $f_{PCP}$, $f_{ADC}$, $f_{FADC}$, $I_{DD}$, $I_{DDSUM}$, $I_{V5}$, $PD$
- Added footnote 8 to $PD$

Changes from V1.1 to V1.2

- change $t_{48}$ from 100ns to 200ns in table 29
- change $t_{49}$ from 100ns to 200ns in table 29
- extend $K_{OVAN}$ conditon from $I_{OV} \leq$ 0 mA; $I_{OV} \geq$ -1 mA to $I_{OV} \leq$ 0 mA; $I_{OV} \geq$ -2 mA
- clearify leakage definition for A1 and I pads for 150°C $< T_J \leq$ 160°C
- change $V_{ILS}$ from 2.1V to 1.9V in table 25
- change $t_{56}$ from 1 / $f_{FPI}$ to 1 / $f_{FPI}$ + 1 in table 30
- change $R_{AIN}$ from 4500 Ohm to 9000 Ohm in table 15
- add the product options SAK-TC1728F-192F133HL
- shift the products SAK-TC1728F-192F133HR and SAK-TC1728N-192F80HR from step AB to AC
- Update max limit for pad class F parameter $R_{DSONM}$

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