250mA, 4V to 80V Low Dropout Micropower Linear Regulator with PWRGD

FEATURES

- **Wide Input Voltage Range: 4V to 80V**
- **Low Quiescent Current: 65µA**
- **Low Dropout Voltage: 400mV**
- **Output Current: 250mA**
- No Protection Diodes Needed
- Adjustable Output from 1.24V to 60V
- 1µA Quiescent Current in Shutdown
- Stable with 3.3µF Output Capacitor
- Stable with Aluminum, Tantalum or Ceramic Capacitors
- Reverse-Battery Protection
- No Reverse Current Flow from Output to Input
- Thermal Limiting
- Thermally Enhanced 16-Lead TSSOP and 12-Pin (4mm × 3mm) DFN Package

APPLICATIONS

- Low Current High Voltage Regulators
- Regulator for Battery-Powered Systems
- Telecom Applications
- Automotive Applications

DESCRIPTION

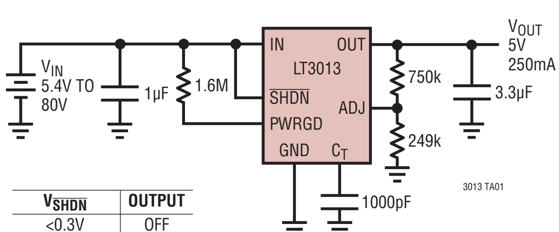
The LT®3013 is a high voltage, micropower low dropout linear regulator. The device is capable of supplying 250mA of output current with a dropout voltage of 400mV. Designed for use in battery-powered or high voltage systems, the low quiescent current (65µA operating and 1µA in shutdown) makes the LT3013 an ideal choice. Quiescent current is also well controlled in dropout.

Other features of the LT3013 include a PWRGD flag to indicate output regulation. The delay between regulated output level and flag indication is programmable with a single capacitor. The LT3013 also has the ability to operate with very small output capacitors. The regulator is stable with only 3.3µF on the output while most older devices require between 10µF and 100µF for stability. Small ceramic capacitors can be used without any need for series resistance (ESR) as is common with other regulators. Internal protection circuitry includes reverse-battery protection, current limiting, thermal limiting and reverse current protection.

The device is available with an adjustable output with a 1.24V reference voltage. The LT3013 regulator is available in the thermally enhanced 16-lead TSSOP and the low profile (0.75mm), 12-pin (4mm × 3mm) DFN package, both providing excellent thermal characteristics.

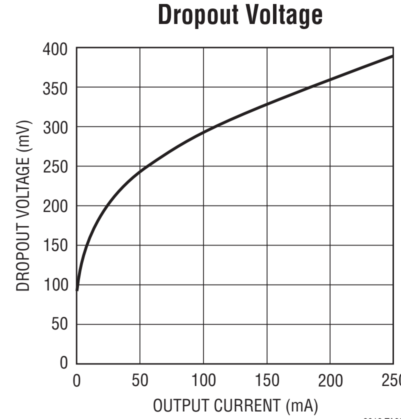
TYPICAL APPLICATION

5V Supply with Shutdown



$V_{\overline{SHDN}}$	OUTPUT
<0.3V	OFF
>2.0V	ON

Dropout Voltage



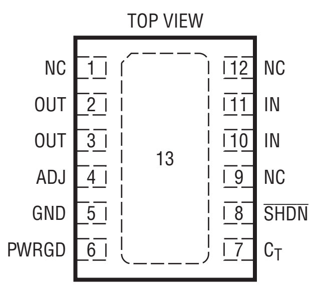
ABSOLUTE MAXIMUM RATINGS

(Note 1)

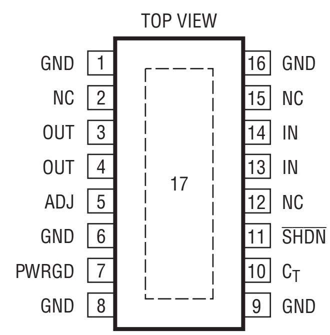
IN Pin Voltage .... ±80V
OUT Pin Voltage .... ±60V
IN to OUT Differential Voltage .... ±80V
ADJ Pin Voltage .... ±7V
$\overline{\text{SHDN}}$ Pin Input Voltage .... ±80V
CT Pin Voltage .... 7V, –0.5V
PWRGD Pin Voltage .... 80V, –0.5V
Output Short-Circuit Duration .... Indefinite

Storage Temperature Range
TSSOP Package .... –65°C to 150°C
DFN Package .... –65°C to 125°C
Operating Junction Temperature Range
(Notes 3, 10, 11)
LT3013E .... –40°C to 125°C
LT3013HFE .... –40°C to 140°C
LT3013MP .... –55°C to 125°C
Lead Temperature (FE16 Soldering, 10 sec) .... 300°C

PIN CONFIGURATION



DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 16°C/W
EXPOSED PAD (PIN 13) IS GND
MUST BE SOLDERED TO PCB



FE PACKAGE
16-LEAD PLASTIC TSSOP
T_{JMAX} = 140°C, θ_{JA} = 40°C/W, θ_{JC} = 16°C/W
EXPOSED PAD (PIN 17) IS GND
MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3013EDE#PBF	LT3013EDE#TRPBF	3013	12-Lead (4mm x 3mm) Plastic DFN	–40°C to 125°C
LT3013EFE#PBF	LT3013EFE#TRPBF	3013EFE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3013HFE#PBF	LT3013HFE#TRPBF	3013HFE	16-Lead Plastic TSSOP	–40°C to 140°C
LT3013MPFE#PBF	LT3013MPFE#TRPBF	3013MPFE	16-Lead Plastic TSSOP	–55°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3013EDE	LT3013EDE#TR	3013	12-Lead (4mm x 3mm) Plastic DFN	–40°C to 125°C
LT3013EFE	LT3013EFE#TR	3013EFE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3013HFE	LT3013HFE#TR	3013HFE	16-Lead Plastic TSSOP	–40°C to 140°C
LT3013MPFE	LT3013MPFE#TR	3013MPFE	16-Lead Plastic TSSOP	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS (LT3013E, LT3013MP)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage	I_{LOAD} = 250mA	●		4	4.75	V
ADJ Pin Voltage (Notes 2,3)	V_{IN} = 4V, I_{LOAD} = 1mA 4.75V < V_{IN} < 80V, 1mA < I_{LOAD} < 250mA	 ●	1.225 1.2	1.24 1.24	1.255 1.28	V V
Line Regulation	ΔV_{IN} = 4V to 80V, I_{LOAD} = 1mA (Note 2)	●		0.1	5	mV
Load Regulation (Note 2)	V_{IN} = 4.75V, ΔI_{LOAD} = 1mA to 250mA V_{IN} = 4.75V, ΔI_{LOAD} = 1mA to 250mA	 ●		7	12 25	mV mV
Dropout Voltage V_{IN} = $V_{OUT(NOMINAL)}$ (Notes 4, 5)	I_{LOAD} = 10mA I_{LOAD} = 10mA	 ●		160	230 300	mV mV
	I_{LOAD} = 50mA I_{LOAD} = 50mA	 ●		250	340 420	mV mV
	I_{LOAD} = 250mA I_{LOAD} = 250mA	 ●		400	490 620	mV mV
GND Pin Current V_{IN} = 4.75V (Notes 4, 6)	I_{LOAD} = 0mA I_{LOAD} = 100mA I_{LOAD} = 250mA	● ●		65 3 10	120 18	µA mA mA
Output Voltage Noise	C_{OUT} = 10µF, I_{LOAD} = 250mA, BW = 10Hz to 100kHz			100		μV_{RMS}
ADJ Pin Bias Current	(Note 7)			30	100	nA
Shutdown Threshold	V_{OUT} = Off to On V_{OUT} = On to Off	● ●	 0.3	1.3 0.8	2	V V
$\overline{SHDN}$ Pin Current (Note 8)	$V_{\overline{SHDN}}$ = 0V $V_{\overline{SHDN}}$ = 6V			0.3 0.1	2 1	µA µA
Quiescent Current in Shutdown	V_{IN} = 6V, $V_{\overline{SHDN}}$ = 0V			1	5	µA
PWRGD Trip Point	% of Nominal Output Voltage, Output Rising	●	85	90	94	%
PWRGD Trip Point Hysteresis	% of Nominal Output Voltage			1.1		%
PWRGD Output Low Voltage	I_{PWRGD} = 50µA	●		140	250	mV
C_T Pin Charging Current				3.0	6	µA
C_T Pin Voltage Differential	$V_{CT(PWRGD\ High)} - V_{CT(PWRGD\ Low)}$			1.6		V
Ripple Rejection	V_{IN} = 7V(Avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 250mA		65	75		dB
Current Limit	V_{IN} = 7V, V_{OUT} = 0V V_{IN} = 4.75V, ΔV_{OUT} = –0.1V (Note 2)	 ●	 250	400		mA mA
Reverse Output Current (Note 9)	V_{OUT} = 1.24V, V_{IN} < 1.24V (Note 2)			12	25	µA

ELECTRICAL CHARACTERISTICS (LT3013H)

The ● denotes the specifications which apply over the –40°C to 140°C operating temperature range, otherwise specifications are at T_J = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage	I_{LOAD} = 200mA	●		4	4.75	V
ADJ Pin Voltage (Notes 2,3)	V_{IN} = 4V, I_{LOAD} = 1mA 4.75V < V_{IN} < 80V, 1mA < I_{LOAD} < 200mA	 ●	1.225 1.2	1.24 1.24	1.255 1.28	V V
Line Regulation	ΔV_{IN} = 4V to 80V, I_{LOAD} = 1mA (Note 2)	●		0.1	5	mV
Load Regulation (Note 2)	V_{IN} = 4.75V, ΔI_{LOAD} = 1mA to 200mA V_{IN} = 4.75V, ΔI_{LOAD} = 1mA to 200mA	 ●		6	12 30	mV mV

ELECTRICAL CHARACTERISTICS (LT3013H)

The ● denotes the specifications which apply over the –40°C to 140°C operating temperature range, otherwise specifications are at T_J = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Dropout Voltage $V_{IN} = V_{OUT(NOMINAL)}$ (Notes 4, 5)	I_{LOAD} = 10mA I_{LOAD} = 10mA	 ●		160	230 320	mV mV
	I_{LOAD} = 50mA I_{LOAD} = 50mA	 ●		250	340 450	mV mV
	I_{LOAD} = 200mA I_{LOAD} = 200mA	 ●		360	490 630	mV mV
GND Pin Current V_{IN} = 4.75V (Notes 4, 6)	I_{LOAD} = 0mA I_{LOAD} = 100mA I_{LOAD} = 200mA	● ●		65 3 7	130 18	µA mA mA
Output Voltage Noise	C_{OUT} = 10µF, I_{LOAD} = 200mA, BW = 10Hz to 100kHz			100		$µV_{RMS}$
ADJ Pin Bias Current	(Note 7)			30	100	nA
Shutdown Threshold	V_{OUT} = Off to On V_{OUT} = On to Off	● ●	 0.3	1.3 0.8	2	V V
$\overline{SHDN}$ Pin Current (Note 8)	$V_{\overline{SHDN}}$ = 0V $V_{\overline{SHDN}}$ = 6V			0.3 0.1	2 1	µA µA
Quiescent Current in Shutdown	V_{IN} = 6V, $V_{\overline{SHDN}}$ = 0V			1	5	µA
PWRGD Trip Point	% of Nominal Output Voltage, Output Rising	●	85	90	95	%
PWRGD Trip Point Hysteresis	% of Nominal Output Voltage			1.1		%
PWRGD Output Low Voltage	I_{PWRGD} = 50µA	●		140	250	mV
C_T Pin Charging Current				3.0	6	µA
C_T Pin Voltage Differential	$V_{CT(PWRGD\ High)} – V_{CT(PWRGD\ Low)}$			1.6		V
Ripple Rejection	V_{IN} = 7V(Avg), $V_{RIPPLE} = 0.5V_{P-P}$, f_{RIPPLE} = 120Hz, I_{LOAD} = 200mA		65	75		dB
Current Limit	V_{IN} = 7V, V_{OUT} = 0V V_{IN} = 4.75V, ΔV_{OUT} = –0.1V (Note 2)	 ●	 200	400		mA mA
Reverse Output Current (Note 9)	V_{OUT} = 1.24V, V_{IN} < 1.24V (Note 2)			12	25	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3013 is tested and specified for these conditions with the ADJ pin connected to the OUT pin.

Note 3: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

Note 4: To satisfy requirements for minimum input voltage, the LT3013 is tested and specified for these conditions with an external resistor divider (249k bottom, 649k top) for an output voltage of 4.5V. The external resistor divider will add a 5µA DC load on the output.

Note 5: Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to ($V_{IN} – V_{DROPOUT}$).

Note 6: GND pin current is tested with V_{IN} = 4.75V and a current source load. This means the device is tested while operating close to its dropout region. This is the worst-case GND pin current. The GND pin current will decrease slightly at higher input voltages.

Note 7: ADJ pin bias current flows into the ADJ pin.

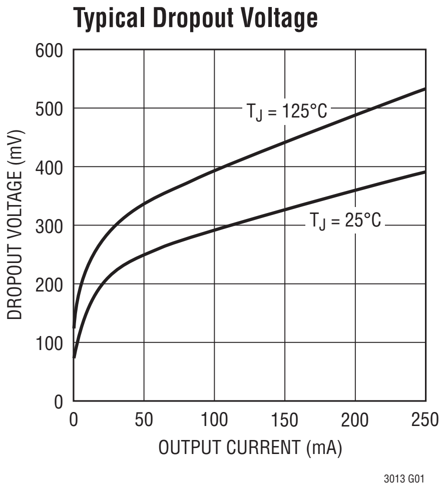
Note 8: $\overline{SHDN}$ pin current flows out of the $\overline{SHDN}$ pin.

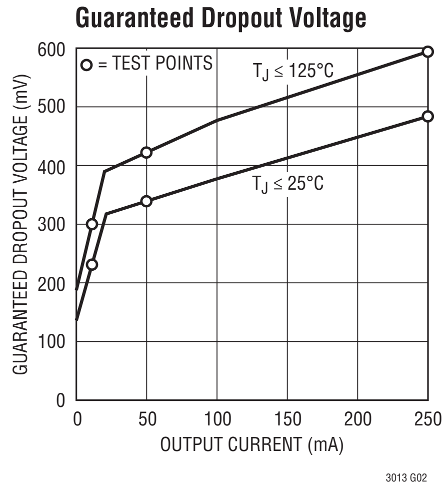
Note 9: Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

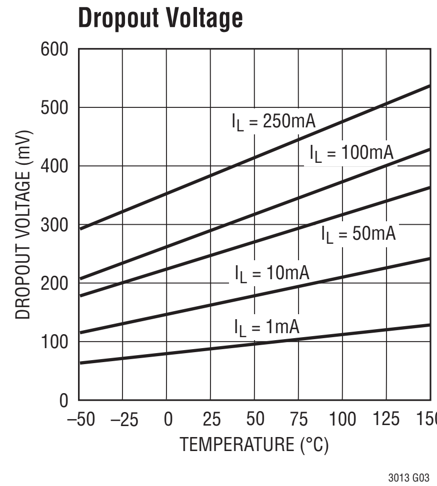
Note 10: The LT3013E is guaranteed to meet performance specifications from 0°C to 125°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3013H is tested to the LT3013H Electrical Characteristics table at 140°C operating junction temperature. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C. The LT3013MP is 100% tested and guaranteed over the –55°C to 125°C operating junction temperature range.

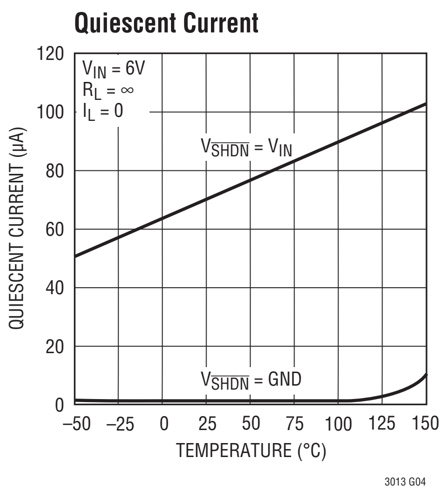
Note 11: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C (LT3013E, LT3013MP) or 140°C (LT3013H) when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

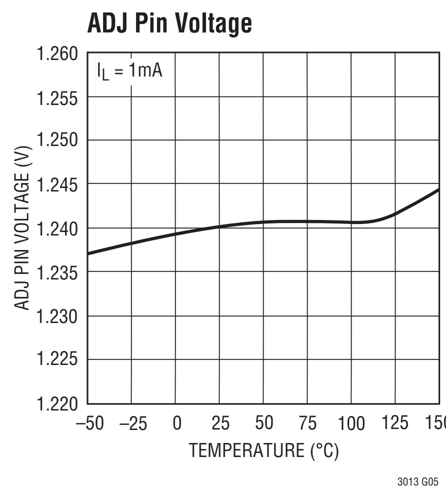
TYPICAL PERFORMANCE CHARACTERISTICS





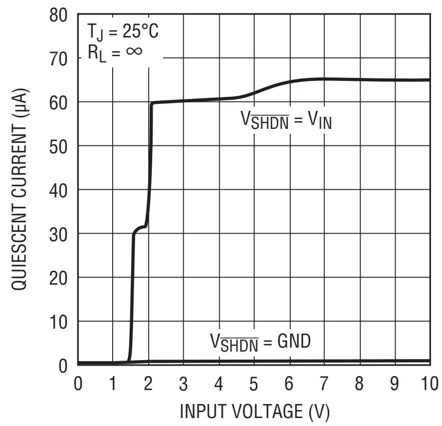






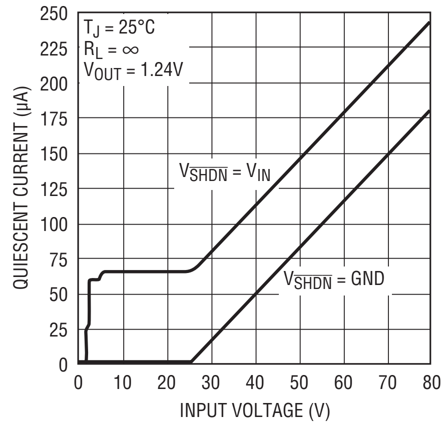
TYPICAL PERFORMANCE CHARACTERISTICS

Quiescent Current



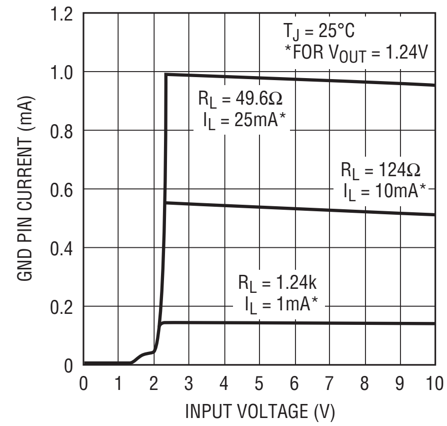
3013 G06

Quiescent Current



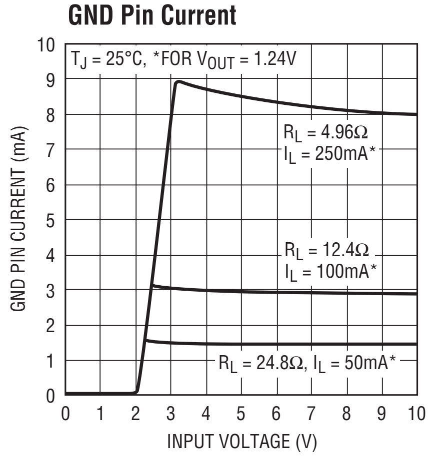
3013 G06b

GND Pin Current



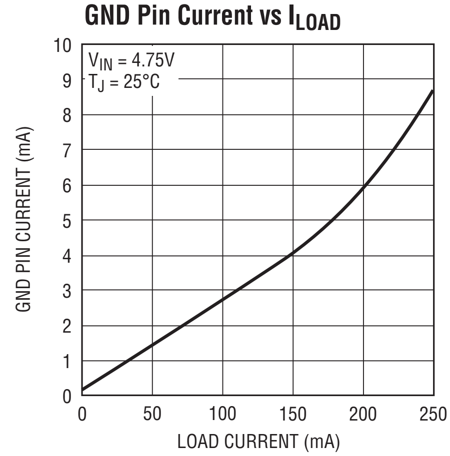
3013 G07

GND Pin Current



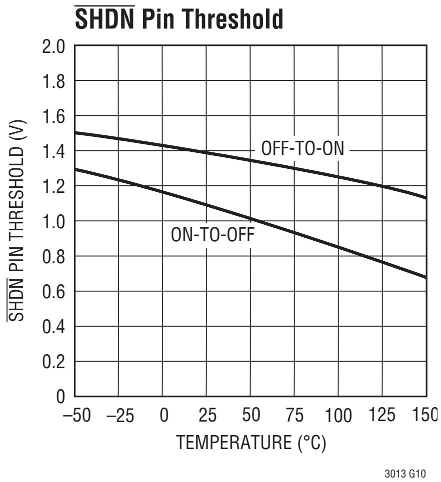
3013 G08

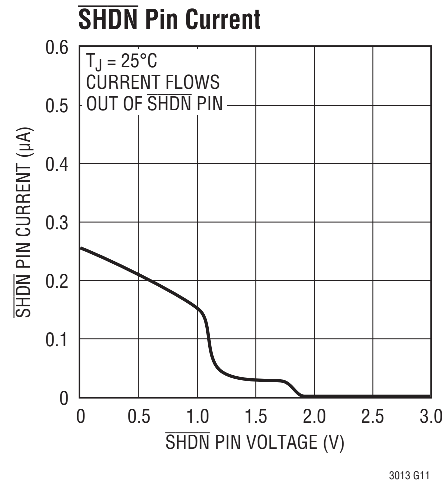
GND Pin Current vs I_{LOAD}

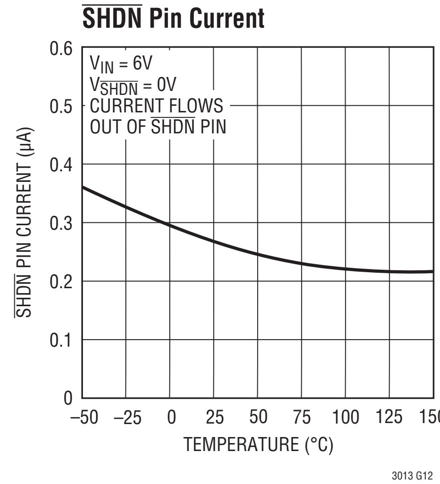


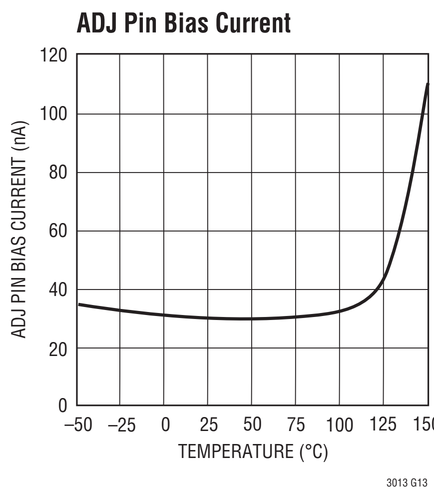
3013 G09

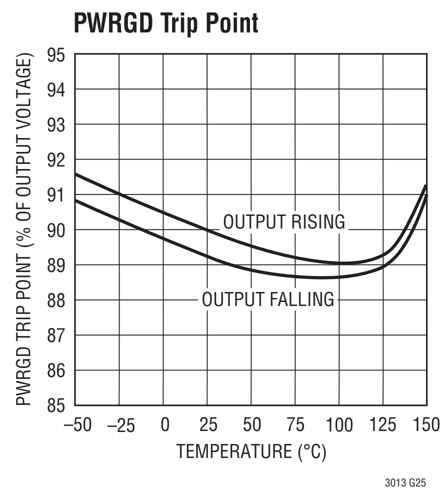
TYPICAL PERFORMANCE CHARACTERISTICS











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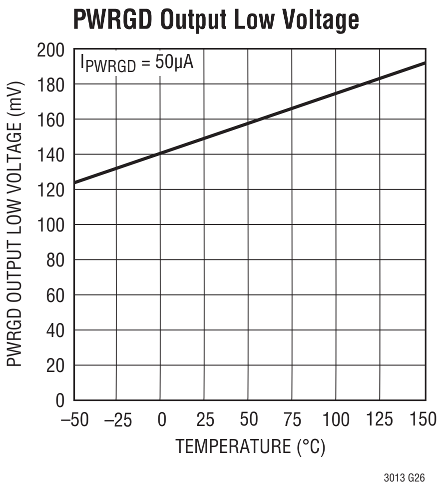

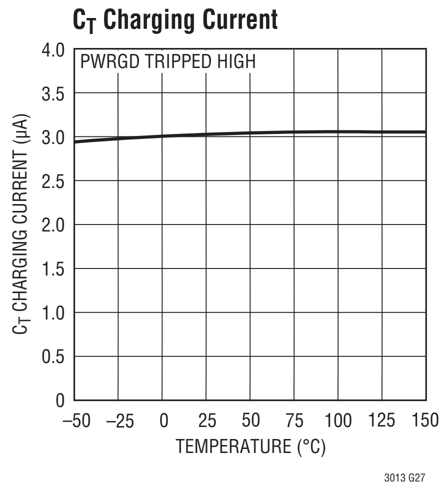

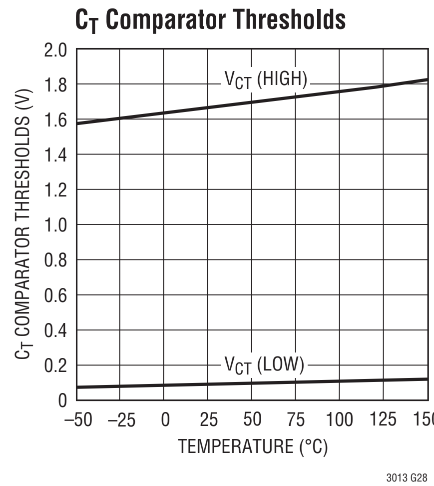

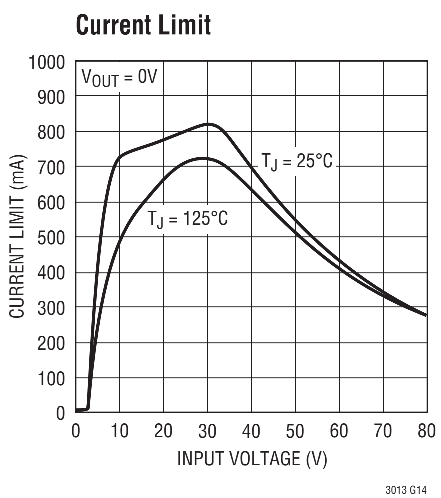

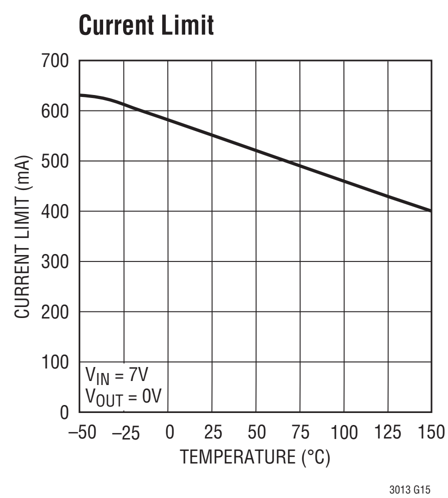

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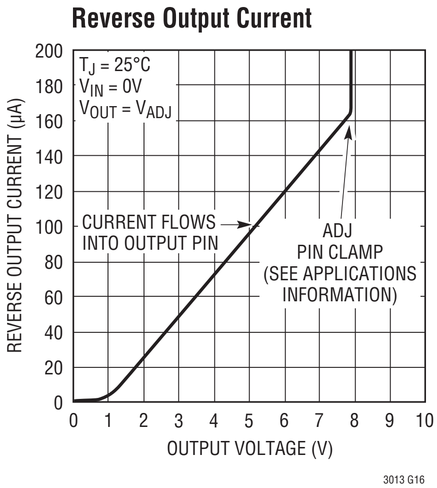
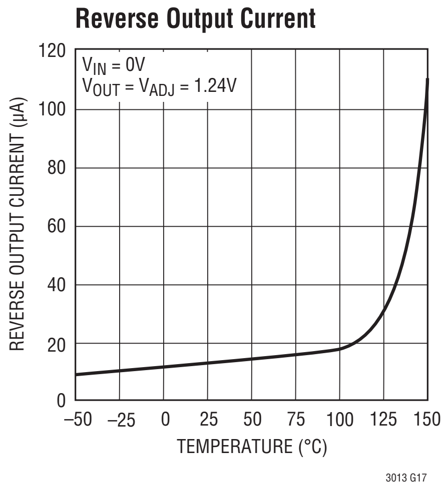
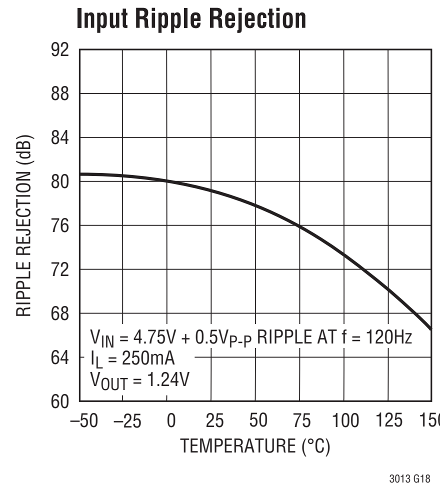
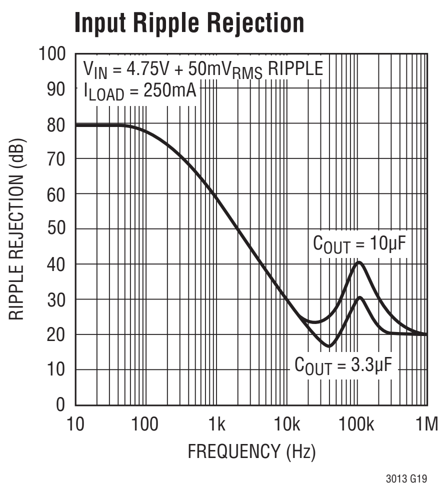
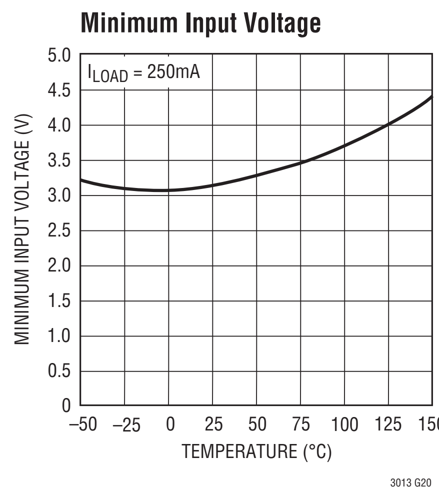


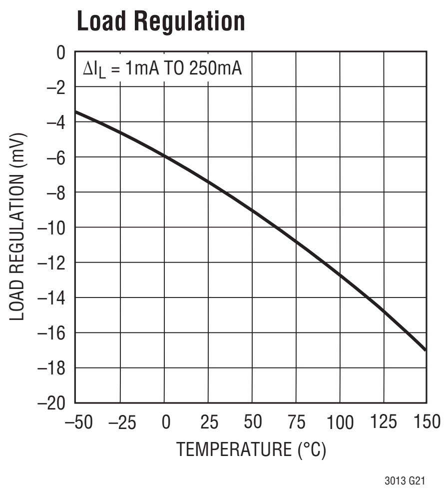


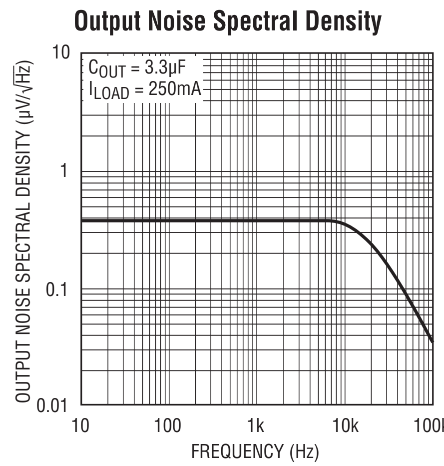


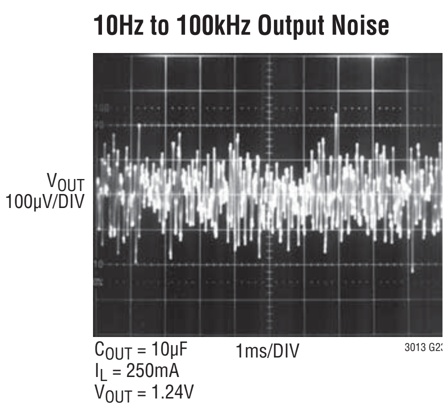


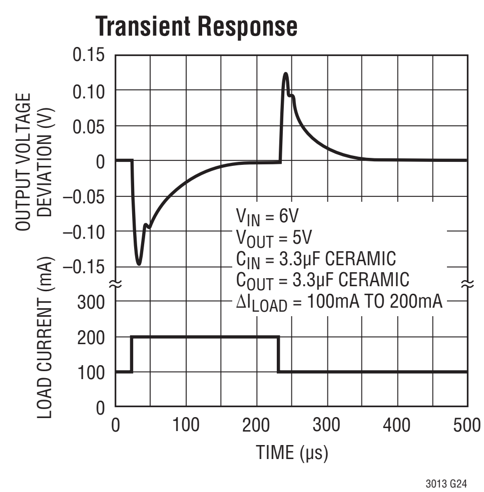


TYPICAL PERFORMANCE CHARACTERISTICS









PIN FUNCTIONS (DFN Package)/(TSSOP Package)

NC (Pins 1, 9, 12)/(Pins 2, 12, 15): No Connect. These pins have no internal connection; connecting NC pins to a copper area for heat dissipation provides a small improvement in thermal performance.

OUT (Pins 2, 3)/(Pins 3, 4): Output. The output supplies power to the load. A minimum output capacitor of 3.3µF is required to prevent oscillations. Larger output capacitors will be required for applications with large transient loads to limit peak voltage transients. See the Applications Information section for more information on output capacitance and reverse output characteristics.

ADJ (Pin 4)/(Pin 5): Adjust. This is the input to the error amplifier. This pin is internally clamped to ±7V. It has a bias current of 30nA which flows into the pin (see curve of ADJ Pin Bias Current vs Temperature in the Typical Performance Characteristics). The ADJ pin voltage is 1.24V referenced to ground, and the output voltage range is 1.24V to 60V.

GND (Pins 5, 13)/(Pins 1, 6, 8, 9, 16, 17): Ground. The exposed backside of the package is an electrical connection for GND. As such, to ensure optimum device operation and thermal performance, the exposed pad must be connected directly to Pin 5/Pin 6 on the PC board.

PWRGD (Pin 6)/(Pin 7): Power Good. The PWRGD flag is an open collector flag to indicate that the output voltage has come up to above 90% of the nominal output voltage. There is no internal pull-up on this pin; a pull-up resistor must be used. The PWRGD pin will change state from an open-collector to high impedance after both the output is above 90% of the nominal voltage and the capacitor on the CT pin has charged through a 1.6V differential. The maximum pull-down current of the PWRGD pin in the low state is 50µA.

$\overline{\text{SHDN}}$ (Pin 8)/(Pin 11): Shutdown. The $\overline{\text{SHDN}}$ pin is used to put the LT3013 into a low power shutdown state. The output will be off when the $\overline{\text{SHDN}}$ pin is pulled low. The $\overline{\text{SHDN}}$ pin can be driven either by 5V logic or open-collector logic with a pull-up resistor. The pull-up resistor is only required to supply the pull-up current of the open-collector gate, normally several microamperes. If unused, the $\overline{\text{SHDN}}$ pin must be tied to a logic high or V_{IN}.

C_T (Pin 7)/(Pin 10): Timing Capacitor. The C_T pin allows the use of a small capacitor to delay the timing between the point where the output crosses the PWRGD threshold and the PWRGD flag changes to a high impedance state. Current out of this pin during the charging phase is 3µA. The voltage difference between the PWRGD low and PWRGD high states is 1.6V (see the Applications Information Section).

IN (Pins 10, 11)/(Pins 13,14): Input. Power is supplied to the device through the IN pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1µF to 10µF is sufficient. The LT3013 is designed to withstand reverse voltages on the IN pin with respect to ground and the OUT pin. In the case of a reversed input, which can happen if a battery is plugged in backwards, the LT3013 will act as if there is a diode in series with its input. There will be no reverse current flow into the LT3013 and no reverse voltage will appear at the load. The device will protect both itself and the load.

APPLICATIONS INFORMATION

The LT3013 is a 250mA high voltage low dropout regulator with micropower quiescent current and shutdown. The device is capable of supplying 250mA at a dropout voltage of 400mV. The low operating quiescent current (65μA) drops to 1μA in shutdown. In addition to the low quiescent current, the LT3013 incorporates several protection features which make it ideal for use in battery-powered systems. The device is protected against both reverse input and reverse output voltages. In battery backup applications where the output can be held up by a backup battery when the input is pulled to ground, the LT3013 acts like it has a diode in series with its output and prevents reverse current flow.

Adjustable Operation

The LT3013 has an output voltage range of 1.24V to 60V. The output voltage is set by the ratio of two external resistors as shown in Figure 1. The device servos the output to maintain the voltage at the adjust pin at 1.24V referenced to ground. The current in R1 is then equal to 1.24V/R1 and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 30nA at 25°C, flows through R2 into the ADJ pin. The output voltage can be calculated using the formula in Figure 1. The value of R1 should be less than 250k to minimize errors in the output voltage caused by the ADJ pin bias current.

Note that in shutdown the output is turned off and the divider current will be zero.

The adjustable device is tested and specified with the ADJ pin tied to the OUT pin and a 5μA DC load (unless otherwise specified) for an output voltage of 1.24V. Specifications for output voltages greater than 1.24V will be proportional to the ratio of the desired output voltage to 1.24V; (V_{OUT}/1.24V). For example, load regulation for an output current change of 1mA to 250mA is –7mV typical at V_{OUT} = 1.24V. At V_{OUT} = 12V, load regulation is:

$$(12V/1.24V) \bullet (–7mV) = –68mV$$

Output Capacitance and Transient Response

The LT3013 is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 3.3μF with an ESR of 3Ω or less is recommended to prevent oscillations. The LT3013 is a micropower device and output transient response will be a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3013, will increase the effective output capacitor value.

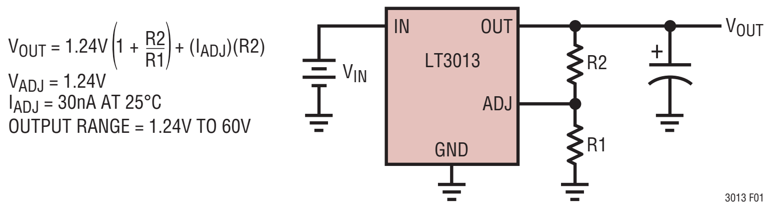


Figure 1. Adjustable Operation

APPLICATIONS INFORMATION

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients as shown in Figures 2 and 3. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor the stress can be induced by vibrations in the system or thermal transients.

PWRGD Flag and Timing Capacitor Delay

The PWRGD flag is used to indicate that the ADJ pin voltage is within 10% of the regulated voltage. The PWRGD pin is an open-collector output, capable of sinking 50µA of current when the ADJ pin voltage is low. There is no internal pull-up on the PWRGD pin; an external pull-up resistor must be used. When the ADJ pin rises to within 10% of its final reference value, a delay timer is started. At the end of this delay, programmed by the value of the capacitor on the C_T pin, the PWRGD pin switches to a high impedance and is pulled up to a logic level by an external pull-up resistor.

To calculate the capacitor value on the C_T pin, use the following formula:

$$C_{TIME} = \frac{I_{CT} \bullet t_{DELAY}}{V_{CT(HIGH)} - V_{CT(LOW)}}$$

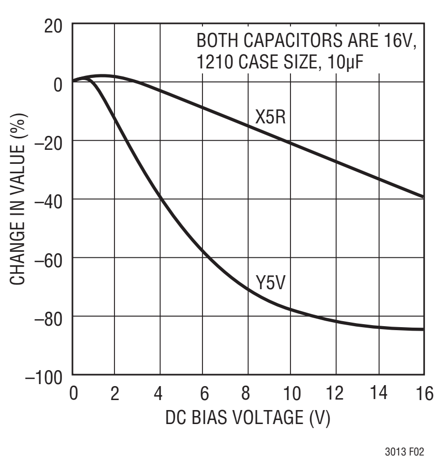


Figure 2. Ceramic Capacitor DC Bias Characteristics

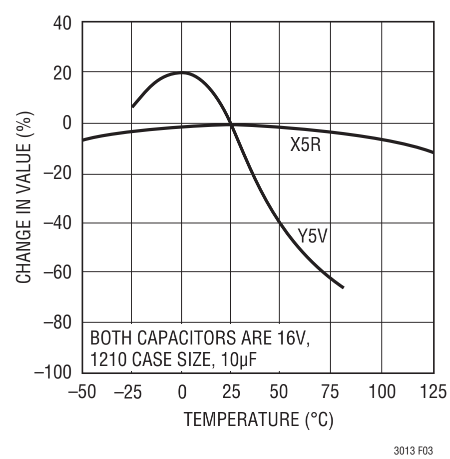


Figure 3. Ceramic Capacitor Temperature Characteristics

APPLICATIONS INFORMATION

Figure 4 shows a block diagram of the PWRGD circuit. At startup, the timing capacitor is discharged and the PWRGD pin will be held low. As the output voltage increases and the ADJ pin crosses the 90% threshold, the JK flip-flop is reset, and the 3µA current source begins to charge the timing capacitor. Once the voltage on the C_T pin reaches the $V_{CT(HIGH)}$ threshold (approximately 1.7V at 25°C), the capacitor voltage is clamped and the PWRGD pin is set to a high impedance state.

During normal operation, an internal glitch filter will ignore short transients (<15µs). Longer transients below the 90% threshold will reset the JK flip-flop. This flip-flop ensures that the capacitor on the C_T pin is quickly discharged all the way to the $V_{CT(LOW)}$ threshold before re-starting the time delay. This provides a consistent time delay after the ADJ pin is within 10% of the regulated voltage before the PWRGD pin switches to high impedance.

Thermal Considerations

The power handling capability of the device will be limited by the maximum rated junction temperature (125°C for LT3013E, LT3013MP or 140°C for LT3013HFE). The power dissipated by the device will be made up of two components:

1. Output current multiplied by the input/output voltage differential: $I_{OUT} \bullet (V_{IN} - V_{OUT})$ and,
2. GND pin current multiplied by the input voltage: $I_{GND} \bullet V_{IN}$.

The GND pin current can be found by examining the GND Pin Current curves in the Typical Performance Characteristics. Power dissipation will be equal to the sum of the two components listed above.

The LT3013 has internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions the maximum junction temperature rating of 125°C (E-grade, MP-grade) or 140°C (H-grade)must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

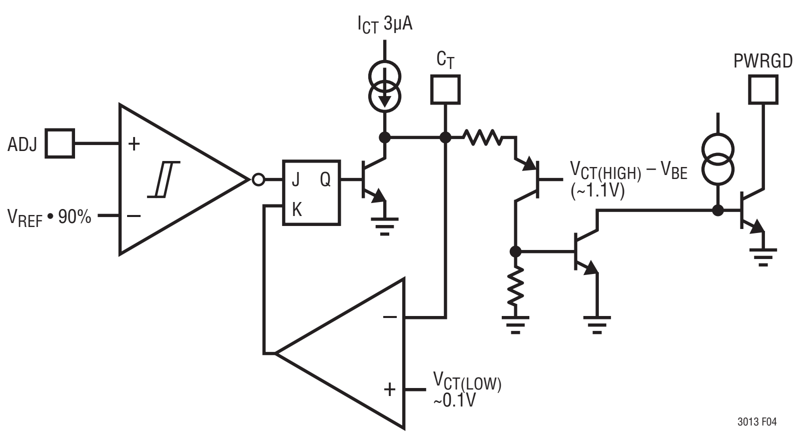


Figure 4. PWRGD Circuit Block Diagram

APPLICATIONS INFORMATION

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

The following tables list thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 3/32" FR-4 board with one ounce copper.

Table 1. TSSOP Measured Thermal Resistance

COPPER AREA TOPSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500 sq mm	2500 sq mm	40°C/W
1000 sq mm	2500 sq mm	45°C/W
225 sq mm	2500 sq mm	50°C/W
100 sq mm	2500 sq mm	62°C/W

Table 2. DFN Measured Thermal Resistance

COPPER AREA TOPSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500 sq mm	2500 sq mm	40°C/W
1000 sq mm	2500 sq mm	45°C/W
225 sq mm	2500 sq mm	50°C/W
100 sq mm	2500 sq mm	62°C/W

The thermal resistance junction-to-case (θ_{JC}), measured at the exposed pad on the back of the die, is 16°C/W.

Continuous operation at large input/output voltage differentials and maximum load current is not practical due to thermal limitations. Transient operation at high input/output differentials is possible. The approximate thermal time constant for a 2500sq mm 3/32" FR-4 board with maximum topside and backside area for one ounce copper is three seconds. This time constant will increase as more thermal mass is added (i.e., vias, larger board, and other components).

For an application with transient high power peaks, average power dissipation can be used for junction temperature calculations if the pulse period is significantly less than the thermal time constant of the device and board.

Calculating Junction Temperature

Example 1: Given an output voltage of 5V, an input voltage range of 8V to 12V, an output current range of 0mA to 250mA, and a maximum ambient temperature of 30°C, what will the maximum junction temperature be?

The power dissipated by the device will be equal to:

$$I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + (I_{GND} \bullet V_{IN(MAX)})$$

where:

$I_{OUT(MAX)} = 250mA$

$V_{IN(MAX)} = 12V$

I_{GND} at ($I_{OUT} = 250mA$, $V_{IN} = 12V$) = 8mA

So:

$$P = 250mA \bullet (12V - 5V) + (8mA \bullet 12V) = 1.85W$$

The thermal resistance will be in the range of 40°C/W to 62°C/W depending on the copper area. So the junction temperature rise above ambient will be approximately equal to:

$$1.85W \bullet 50°C/W = 92.3°C$$

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_{JMAX} = 30°C + 92.3°C = 122.3°C$$

Example 2: Given an output voltage of 5V, an input voltage of 48V that rises to 72V for 5ms(max) out of every 100ms, and a 5mA load that steps to 200mA for 50ms out of every 250ms, what is the junction temperature rise above ambient? Using a 500ms period (well under the time constant of the board), power dissipation is as follows:

$$P1(48V\ in,\ 5mA\ load) = 5mA \bullet (48V - 5V) + (200\mu A \bullet 48V) = 0.23W$$

$$P2(48V\ in,\ 50mA\ load) = 200mA \bullet (48V - 5V) + (8mA \bullet 48V) = 8.98W$$

$$P3(72V\ in,\ 5mA\ load) = 5mA \bullet (72V - 5V) + (200\mu A \bullet 72V) = 0.35W$$

$$P4(72V\ in,\ 50mA\ load) = 200mA \bullet (72V - 5V) + (8mA \bullet 72V) = 13.98W$$

APPLICATIONS INFORMATION

Operation at the different power levels is as follows:

76% operation at P1, 19% for P2, 4% for P3, and 1% for P4.

P_{EFF} = 76%(0.23W) + 19%(8.98W) + 4%(0.35W) + 1%(13.98W) = 2.03W

With a thermal resistance in the range of 40°C/W to 62°C/W, this translates to a junction temperature rise above ambient of 81°C to 125°C.

High Temperature Operation

Care must be taken when designing LT3013 applications to operate at high ambient temperatures. The LT3013 works at elevated temperatures but erratic operation can occur due to unforeseen variations in external components. Some tantalum capacitors are available for high temperature operation, but ESR is often several ohms; capacitor ESR above 3Ω is unsuitable for use with the LT3013. Ceramic capacitor manufacturers (Murata, AVX, TDK, and Vishay Vitramon at this writing) now offer ceramic capacitors that are rated to 150°C using an X8R dielectric. Device instability will occur if output capacitor value and ESR are outside design limits at elevated temperature and operating DC voltage bias (see information on capacitor characteristics under Output Capacitance and Transient Response). Check each passive component for absolute value and voltage ratings over the operating temperature range.

Leakages in capacitors or from solder flux left after insufficient board cleaning adversely affects low quiescent current operation. The output voltage resistor divider should use a maximum bottom resistor value of 124k to compensate for high temperature leakage, setting divider current to 10μA. Consider junction temperature increase due to power dissipation in both the junction and nearby components to ensure maximum specifications are not violated for the device or external components.

Protection Features

The LT3013 incorporates several protection features which make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse-input voltages, and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C (LT3013E, LT3013MP) or 140°C (LT3013HFE).

Like many IC power regulators, the LT3013 has safe operating area protection. The safe area protection decreases the current limit as input voltage increases and keeps the power transistor inside a safe operating region for all values of input voltage. The protection is designed to provide some output current at all values of input voltage up to the device breakdown. The SOA protection circuitry for the LT3013 uses a current generated when the input voltage exceeds 25V to decrease current limit. This current shows up as additional quiescent current for input voltages above 25V. This increase in quiescent current occurs both in normal operation and in shutdown (see curve of Quiescent Current in the Typical Performance Characteristics).

The input of the device will withstand reverse voltages of 80V. No negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries which can be plugged in backward.

The ADJ pin of the device can be pulled above or below ground by as much as 7V without damaging the device. If the input is left open-circuit or grounded, the ADJ pin will act like an open-circuit when pulled below ground, and like a large resistor (typically 100k) in series with a diode when pulled above ground. If the input is powered by a voltage source, pulling the ADJ pin below the reference voltage will cause the device to current limit. This will cause the output to go to a unregulated high voltage. Pulling the ADJ pin above the reference voltage will turn off all output current.

APPLICATIONS INFORMATION

In situations where the ADJ pin is connected to a resistor divider that would pull the ADJ pin above its 7V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5mA. For example, a resistor divider is used to provide a regulated 1.5V output from the 1.24V reference when the output is forced to 60V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5mA when the ADJ pin is at 7V. The 53V difference between the OUT and ADJ pins divided by the 5mA maximum current into the ADJ pin yields a minimum top resistor value of 10.6k.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open-circuit. Current flow back into the output will follow the curve shown in Figure 5. The rise in reverse output current above 7V occurs from the breakdown of the 7V clamp on the ADJ pin. With a resistor divider on the regulator output, this current will be reduced depending on the size of the resistor divider.

When the IN pin of the LT3013 is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current will typically drop to less than 2μA. This can happen if the input of the LT3013 is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the $\overline{\text{SHDN}}$ pin will have no effect on the reverse output current when the output is pulled above the input.

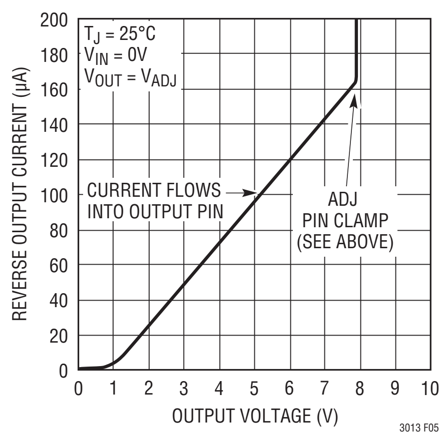
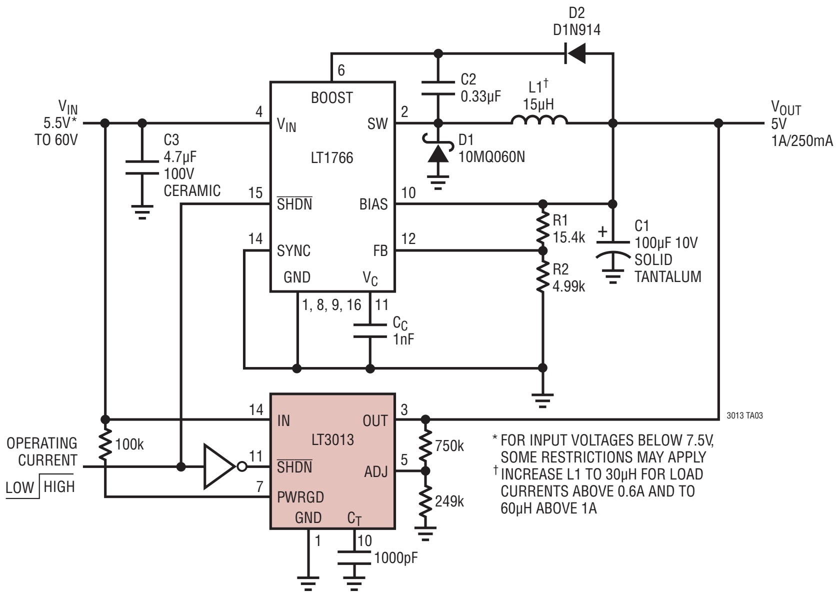


Figure 5. Reverse Output Current

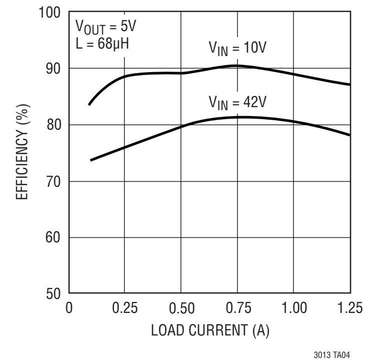
TYPICAL APPLICATIONS

5V Buck Converter with Low Current Keep Alive Backup

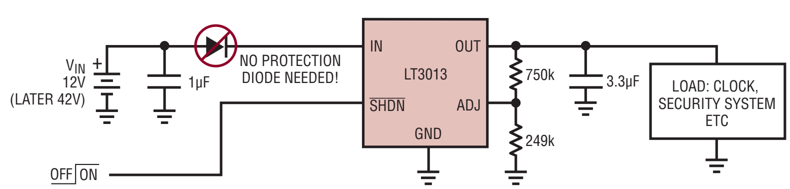


* FOR INPUT VOLTAGES BELOW 7.5V, SOME RESTRICTIONS MAY APPLY
† INCREASE L1 TO 30µH FOR LOAD CURRENTS ABOVE 0.6A AND TO 60µH ABOVE 1A

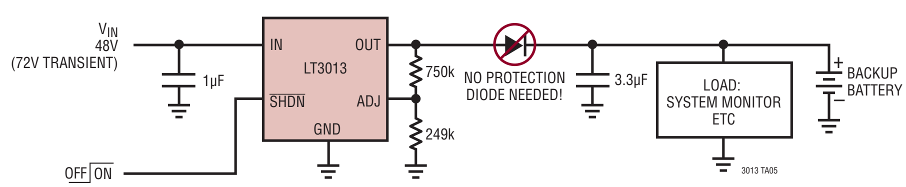
Buck Converter Efficiency vs Load Current



LT3013 Automotive Application

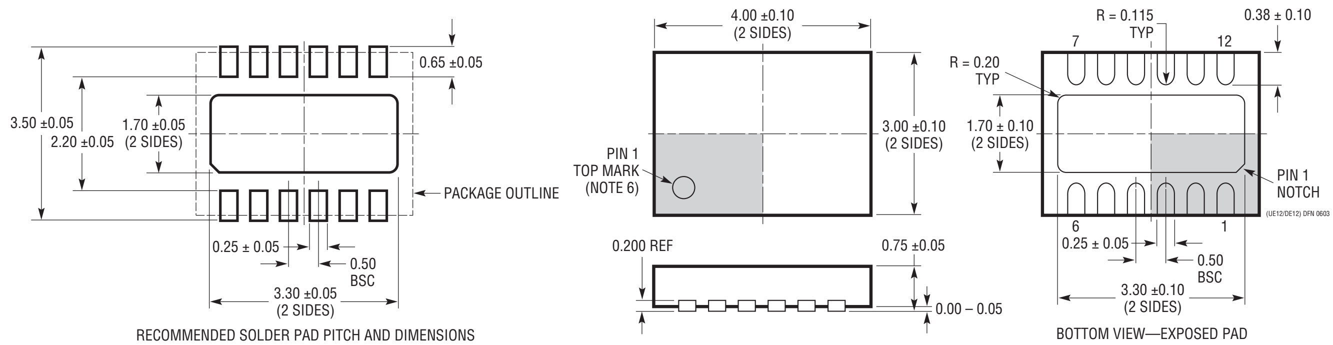


LT3013 Telecom Application



PACKAGE DESCRIPTION

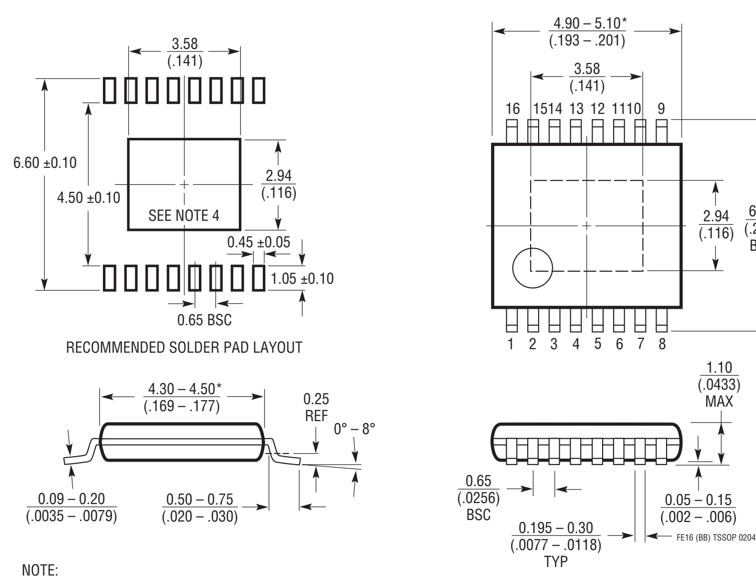
DE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695)



NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)

Exposed Pad Variation BB

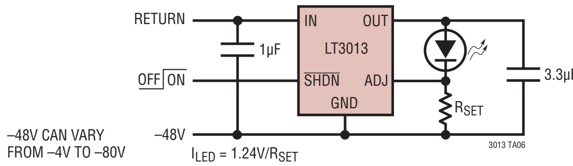


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

Constant Brightness for Indicator LED over Wide Input Voltage Range



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1020	125mA, Micropower Regulator and Comparator	V_{IN}: 4.5V to 36V, $V_{OUT(MIN)}$ = 2.5V, V_{DO} = 0.4V, I_Q = 40µA, I_{SD} = 40µA, Comparator and Reference, Class B Outputs, S16, PDIP14 Packages
LT1120/LT1120A	125mA, Micropower Regulator and Comparator	V_{IN}: 4.5V to 36V, $V_{OUT(MIN)}$ = 2.5V, V_{DO} = 0.4V, I_Q = 40µA, I_{SD} = 10µA, Comparator and Reference, Logic Shutdown, Ref Sources and Sinks 2/4mA, S8, N8 Packages
LT1121/LT1121HV	150mA, Micropower, LDO	V_{IN}: 4.2V to 30/36V, $V_{OUT(MIN)}$ = 3.75V, V_{DO} = 0.42V, I_Q = 30µA, I_{SD} = 16µA, Reverse Battery Protection, SOT-223, S8, Z Packages
LT1129	700mA, Micropower, LDO	V_{IN}: 4.2V to 30V, $V_{OUT(MIN)}$ = 3.75V, V_{DO} = 0.4V, I_Q = 50µA, I_{SD} = 16µA, DD, SOT-223, S8,TO220-5, TSSOP20 Packages
LT1676	60V, 440mA (I_{OUT}), 100kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.4V to 60V, $V_{OUT(MIN)}$ = 1.24V, I_Q = 3.2mA, I_{SD} = 2.5µA, S8 Package
LT1761	100mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.3V, I_Q = 20µA, I_{SD} = <1µA, Low Noise < 20µV_{RMS}, Stable with 1µF Ceramic Capacitors, ThinSOT™ Package
LT1762	150mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.3V, I_Q = 25µA, I_{SD} = <1µA, Low Noise < 20µV_{RMS}, MS8 Package
LT1763	500mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.3V, I_Q = 30µA, I_{SD} = <1µA, Low Noise < 20µV_{RMS}, S8 Package
LT1764/LT1764A	3A, Low Noise, Fast Transient Response, LDO	V_{IN}: 2.7V to 20V, $V_{OUT(MIN)}$ = 1.21V, V_{DO} = 0.34V, I_Q = 1mA, I_{SD} = <1µA, Low Noise < 40µV_{RMS}, "A" Version Stable with Ceramic Capacitors, DD, TO220-5 Packages
LT1766	60V, 1.2A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.5mA, I_{SD} = 25µA, TSSOP16/E Package
LT1776	40V, 550mA (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.4V to 40V, $V_{OUT(MIN)}$ = 1.24V, I_Q = 3.2mA, I_{SD} = 30µA, N8, S8 Packages
LT1934/LT1934-1	300mA/60mA, (I_{OUT}), Constant Off-Time, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN}: 3.2V to 34V, $V_{OUT(MIN)}$ = 1.25V, I_Q = 14µA, I_{SD} = <1µA, ThinSOT Package
LT1956	60V, 1.2A (I_{OUT}), 500kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.5mA, I_{SD} = 25µA, TSSOP16/E Package
LT1962	300mA, Low Noise Micropower, LDO	V_{IN}: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, V_{DO} = 0.27V, I_Q = 30µA, I_{SD} = <1µA, Low Noise < 20µV_{RMS}, MS8 Package
LT1963/LT1963A	1.5A, Low Noise, Fast Transient Response, LDO	V_{IN}: 2.1V to 20V, $V_{OUT(MIN)}$ = 1.21V, V_{DO} = 0.34V, I_Q = 1mA, I_{SD} = <1µA, Low Noise < 40µV_{RMS}, "A" Version Stable with Ceramic Capacitors, DD, TO220-5, SOT-223, S8 Packages
LT1964	200mA, Low Noise Micropower, Negative LDO	V_{IN}: –1.9V to –20V, $V_{OUT(MIN)}$ = –1.21V, V_{DO} = 0.34V, I_Q = 30µA, I_{SD} = 3µA, Low Noise < 30µVRMS, Stable with Ceramic Capacitors, ThinSOT Package
LT3010/LT3010H	50mA, 3V to 80V, Low Noise Micropower LDO	V_{IN}: 3V to 8V, $V_{OUT(MIN)}$ = 1.275V, V_{DO} = 0.3V, I_Q = 30µA, I_{SD} = 1µA, Low Noise < 100µV_{RMS}, MS8E Package, H Grade = +140°C T_{JMAX}
LT3012/LT3012H	250mA, 4V to 80V, Low Dropout Micropower Linear Regulator	V_{IN}: 4V to 80V, V_{OUT}: 1.24V to 60V, V_{DO} = 0.4V, I_Q = 40µA, I_{SD} = <1µA, TSSOP-16E and 4mm × 3mm DFN-12 Packages, H Grade = +140°C T_{JMAX}
LT3014/HV	20mA, 3V to 80V, Low Dropout Micropower Linear Regulator	V_{IN}: 3V to 80V (100V for 2ms, HV version), V_{OUT}: 1.22V to 60V, V_{DO} = 0.35V, I_Q = 7µA, I_{SD} = <1µA, ThinSOT and 3mm × 3mm DFN-8 Packages

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