Tsi572
Serial RapidIO Switch

Features

Serial RapidIO Interfaces

- 30 Gbits/s full-duplex Serial RapidIO switch
- Standard Compliant
  - *RapidIO Interconnect Specification (Revision 1.3)*
  - IEEE 1149.6 AC-JTAG
- Socket compatible with the Tsi576

Configurable

- Two 4x links or up to eight 1x links
  - Each 4x link can be separated into two, 1x links
- Supports 1.25, 2.5 and 3.125 Gbaud rates
- Hot Swap
  - Live insertion and extraction of field replaceable units
- I^{2}C Master/Slave
- Multicast event control symbol
- Lane swap

The Tsi572 enhances system scalability through device configuration and provides architects and designers with a solution for both throughput intensive and power sensitive applications.

Performance

- Low latency 110 ns packet cut-through
- Full duplex, line rate termination, non-blocking fabric
- Prevention of head-of-line blocking
- Error management extensions
- Multicast
- Performance monitoring and statistic registers
- Programmable buffer management
- Additional scheduling algorithms

Low Power

- Programmable SerDes
- Configurable on port width and speed
- Configurable port power down
- Low power
 - 120-200mW per port

Cost

- Integrated SerDes
- Small, 399 HSBGA, 21mm package

The Tsi572^{TM} is a fourth generation RapidIO switch which supports 30 Gbits/s aggregate bandwidth and is optimized for multiprocessor, peer-to-peer embedded networking on line cards using the *RapidIO Interconnect Specification (Revision 1.3)*. The Tsi572 offers lower power and cost per gigabit switched than equivalent PCIe and Gigabit Ethernet solutions, making it optimal for cost sensitive, power-limited embedded systems. For cost sensitive designs, the socket compatibility between the Tsi572 and Tsi576 enables customers to cost-reduce certain Tsi576 applications.

The Tsi572 provides designers and architects with maximum design scalability, enabling them to design theTsi572 into a wide range of applications. As is the case with IDT's other Tsi57x parts, flexible port configurations can be selected through multiple port width and frequency options. The Tsi572 also supports multicast, traffic management through scheduling algorithms, programmable buffer depth, and fabric performance monitoring to supervise and manage traffic flow.

The Tsi572 leverages the industry's best plug and play interoperability with Texas Instruments, Freescale, Xiliinx, and Altera's RapidIO-enabled products.

Block Diagram
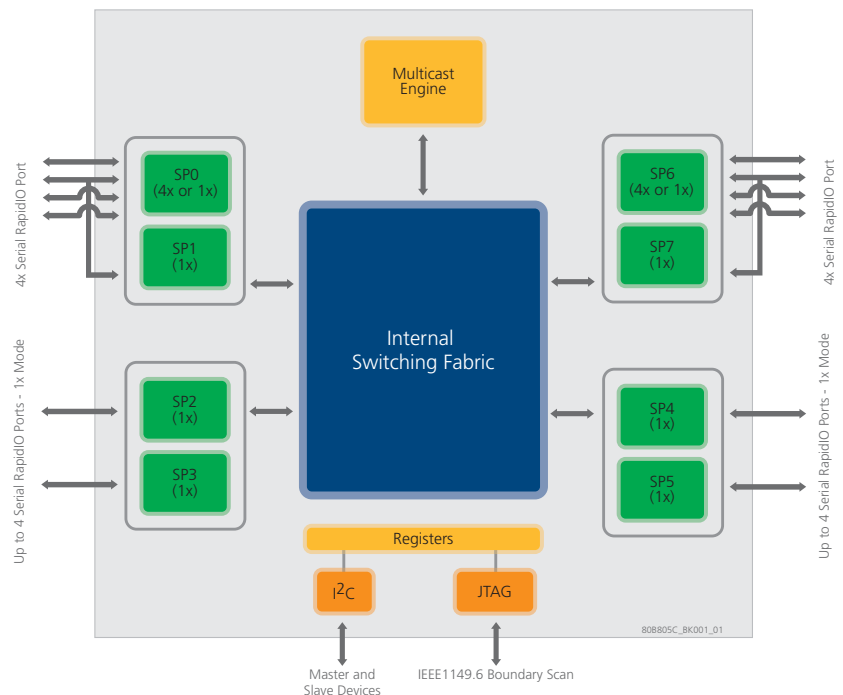
Embedded applications further benefit from the ability to route packets to multiple endpoints through hierarchical lookup tables, independent unicast and multicast routing mechanisms, and error management extensions that provide proactive issue notification to the fabric controller. In addition, the Tsi572 supports both in-band RapidIO access and out-of-band access to the full fabric register set through the I^{2}C interface.

Benefits

- Scalability: Tsi576 footprint compatibility allows system scaling depending on systems cost and performance requirements
- Performance: Improved system and distributed processing performance
- Cost; Designed for more cost-sensitive applications
- Power: Lowest power product in Tsi57x portfolio

Specifications

- Technology: 0.13um
- Voltage: 1.2V and 3.3V
- Low power consumption
- Package: 399 ball, 21mm x 21mm, 1mm ball pitch HSBGA
- Rated for commercial and industrial temperatures
- Pin compatible with the Tsi576

Socket compatibility with Tsi576 eases migration and increases design scalability for existing cost sensitive designs.

Target Markets

Wireless Infrastructure
- WiMax
- 3G LTE
- eWCDMA
- Node B, Radio Network Controller, Media Gateway

Communications Wireline Infrastructure
- Multiservice WAN Switches, 1 to 10 Gbit Ethernet Switches, 1 to >10Gbit Routers, DSLAMs

Video Infrastructure
- Broadcast, imaging, and encoding
- Video conference systems
- Video head-end infrastructure
- Video telepresence

Architecture Standards
- ATCA, MicroTCA, VXS, VPX

Typical Applications

The Tsi572 is ideal for many embedded applications because it provides chip-to-chip interconnect between I/O devices and 4x links to backplanes. The Tsi572 supports multiple backplanes, inlcuding those compliant with PICMG AMC 4, which has a data rate of up to 10 Gbps.

The Tsi572 enables high performance peer-to-peer communication through its non-blocking switch fabric for systems with multiple RapidIO-enabled processors. With the Tsi572, system OEMs can design multiple software applications on the same base hardware by leveraging the RapidIO-enabled architecture.
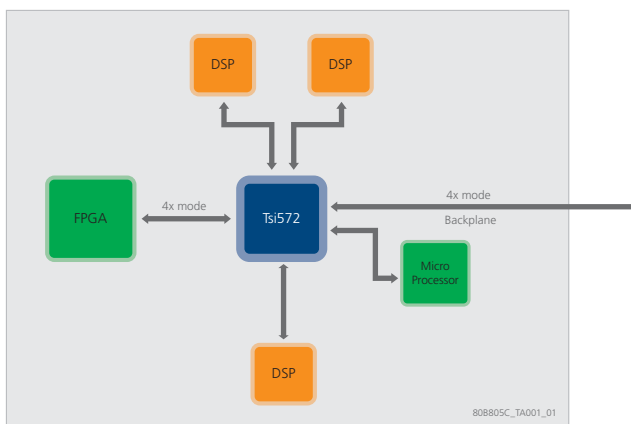
For video applications, which have critical high frame size and rate performance requirements, the Tsi572 offers DSP aggregation with low latency

Video Card DSP Application
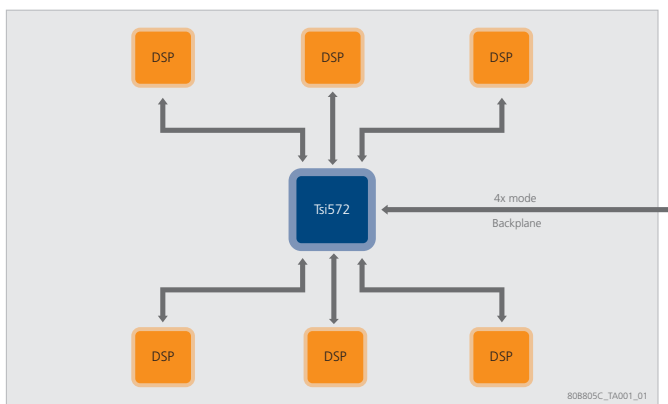
The Tsi572 brings many advantages to wireless applications. It provides a unified platform for WiMAX, eWCDMA, or 3G LTE, and aggregates the key hardware components with three layer hardware termination. It also frees the FPGA, ASIC, DSP and microprocessor resources for application tasks such as OFDMA PHY processing, MAC layer processing, symbol and chip rate processing tasks.

Wireless Baseband Processor Application