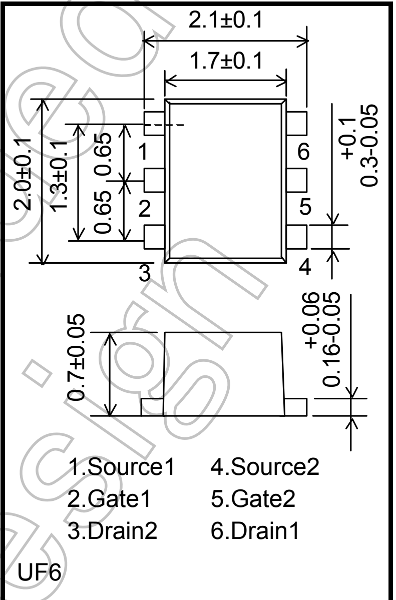
TOSHIBA Field Effect Transistor Silicon P/N Channel MOS Type

SSM6L11TU

High Speed Switching Applications

- Optimum for high-density mounting in small packages
- Low ON-resistance Q1: $R_{DS(ON)}$ = 395mΩ (max) (@V_{GS} = 1.8 V)
  Q2: $R_{DS(ON)}$ = 430mΩ (max) (@V_{GS} = -2.5 V)

Unit: mm



JEDEC	―
JEITA	―
TOSHIBA	2-2T1B

Weight: 7.0 mg (typ.)

Q1 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	20	V
Gate-source voltage		V_{GSS}	± 12	V
Drain current	DC	I_D	0.5	A
	Pulse	I_{DP}	1.5	

Q2 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	-20	V
Gate-source voltage		V_{GSS}	± 12	V
Drain current	DC	I_D	-0.5	A
	Pulse	I_{DP}	-1.5	

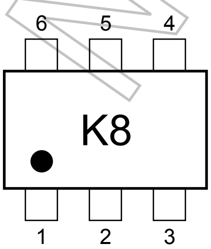
Absolute Maximum Ratings (Q1,Q2 Common) (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Drain power dissipation	P_D (Note 1)	500	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C

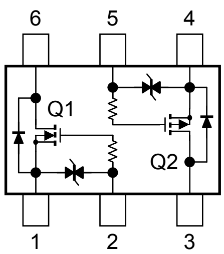
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board. (total dissipation)
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm^2)

Marking



Equivalent Circuit (top view)



Start of commercial production
2004-03

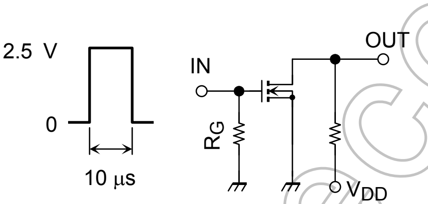
Q1 Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±12V, V_{DS} = 0	—	—	±1	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 1 mA, V_{GS} = 0	20	—	—	V
		$V_{(BR)\ DSX}$	I_D = 1 mA, V_{GS} = −12 V	10	—	—	
Drain cut-off current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.5	—	1.1	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 0.25 A (Note2)	1.2	2.4	—	S
Drain-source on-resistance		$R_{DS\ (ON)}$	I_D = 0.25 A, V_{GS} = 4.0 V (Note2)	—	125	145	mΩ
			I_D = 0.25 A, V_{GS} = 2.5 V (Note2)	—	150	190	
			I_D = 0.25 A, V_{GS} = 1.8 V (Note2)	—	200	395	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	268	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	34	—	pF
Output capacitance		C_{oss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	44	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 10 V, I_D = 0.25 A,	—	11	—	ns
	Turn-off time	t_{off}	V_{GS} = 0 to 2.5 V, R_G = 4.7 Ω	—	15	—	

Note2: Pulse test

Switching Time Test Circuit

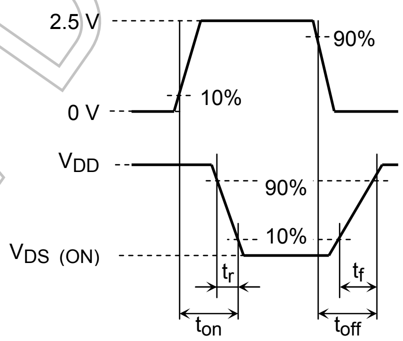
(a) Test Circuit



V_{DD} = 10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}



Precaution

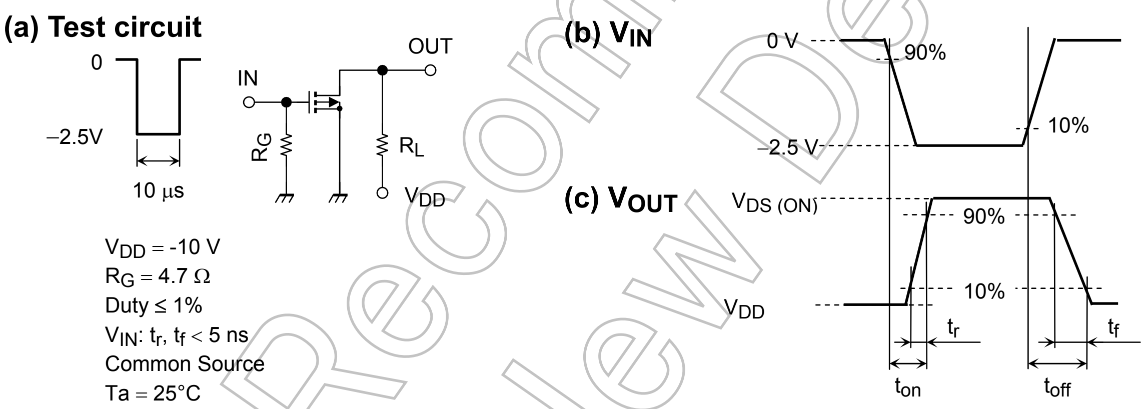
V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D=100 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}.
(The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$)
Please take this into consideration when using the device.

Q2 Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ± 12V, V_{DS} = 0	—	—	±1	μA
Drain-source breakdown voltage		$V_{(BR)\,DSS}$	I_D = -1 mA, V_{GS} = 0	-20	—	—	V
		$V_{(BR)\,DSX}$	I_D = -1 mA, V_{GS} = +12 V	-8	—	—	
Drain cut-off current		I_{DSS}	V_{DS} = -20 V, V_{GS} = 0	—	—	-1	μA
Gate threshold voltage		V_{th}	V_{DS} = -3 V, I_D = -0.1 mA	-0.5	—	-1.1	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -0.25 A (Note3)	0.65	1.3	—	S
Drain-source on-resistance		$R_{DS\,(ON)}$	I_D = -0.25 A, V_{GS} = -4 V (Note3)	—	210	260	mΩ
			I_D = -0.25 A, V_{GS} = -2.5 V (Note3)	—	310	430	
Input capacitance		C_{iss}	V_{DS} = -10 V, V_{GS} = 0, f = 1 MHz	—	218	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = -10 V, V_{GS} = 0, f = 1 MHz	—	42	—	pF
Output capacitance		C_{oss}	V_{DS} = -10 V, V_{GS} = 0, f = 1 MHz	—	52	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = -10 V, I_D = -0.25 A,	—	16	—	ns
	Turn-off time	t_{off}	V_{GS} = 0 to -2.5 V, R_G = 4.7 Ω	—	15	—	

Note3: Pulse test

Switching Time Test Circuit



Precaution

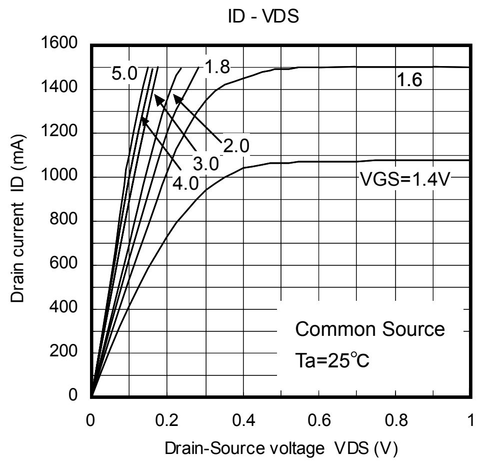
V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D=-100 μA for this product. For normal switching operation, $V_{GS\,(on)}$ requires a higher voltage than V_{th} and $V_{GS\,(off)}$ requires a lower voltage than V_{th}.
(The relationship can be established as follows: $V_{GS\,(off)} < V_{th} < V_{GS\,(on)}$)
Please take this into consideration when using the device.

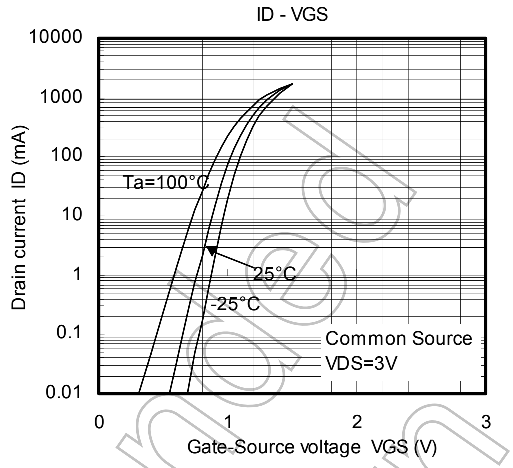
Handling Precaution

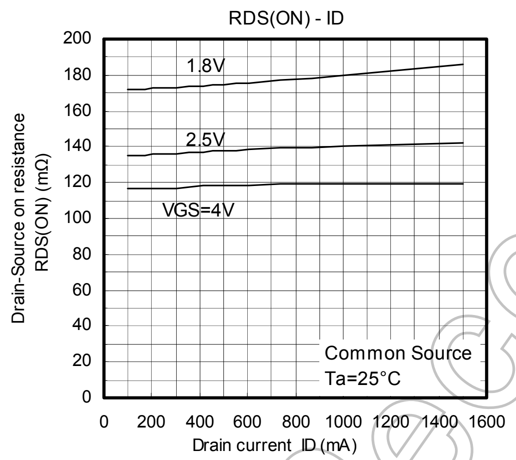
When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

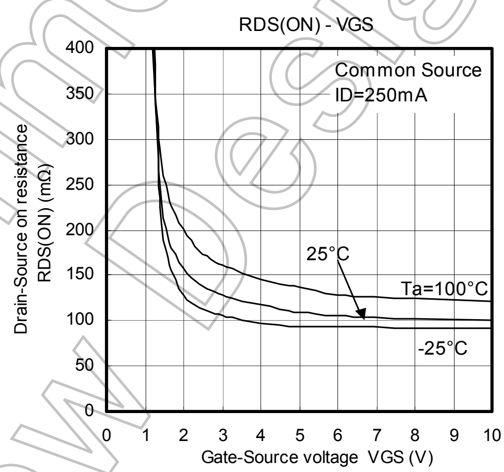
Thermal resistance $R_{th(j-a)}$ and drain power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration.

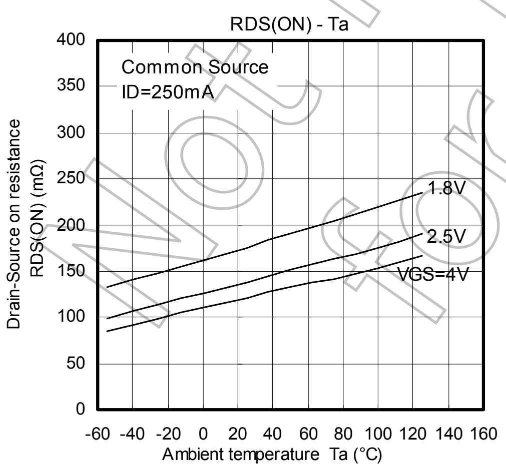
Q1(Nch MOS FET)

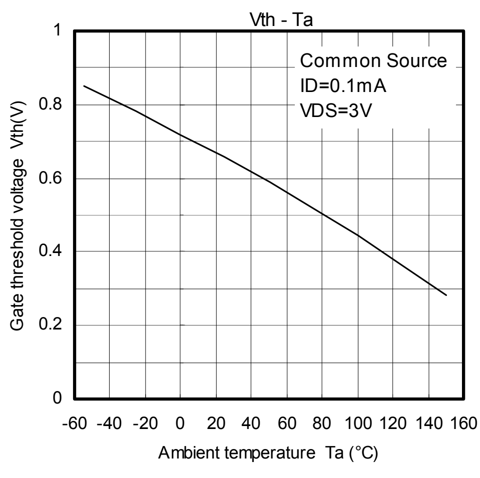




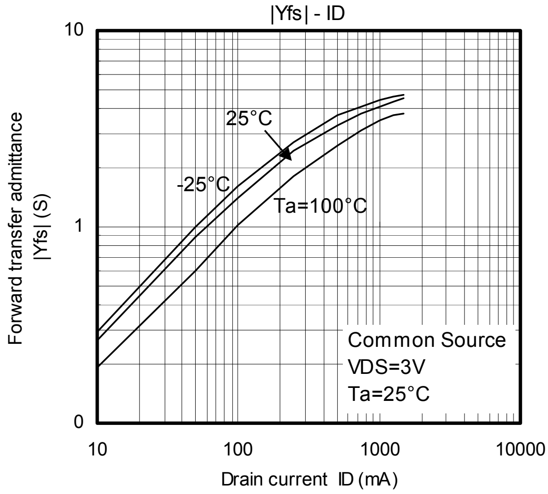


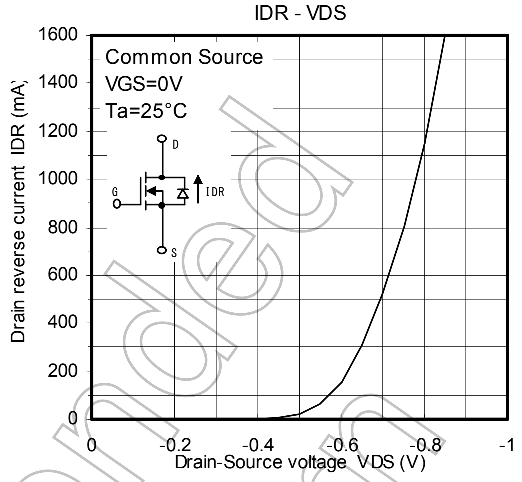


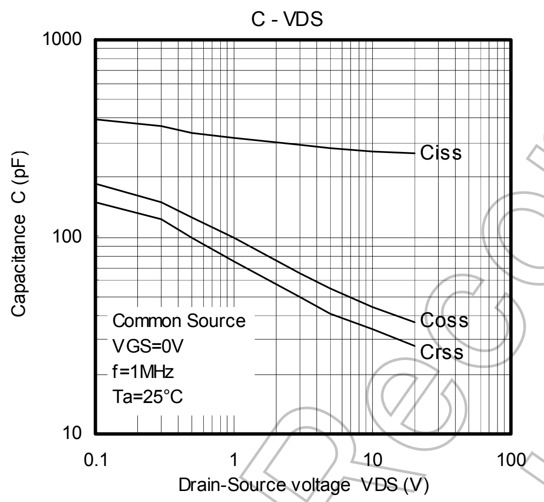


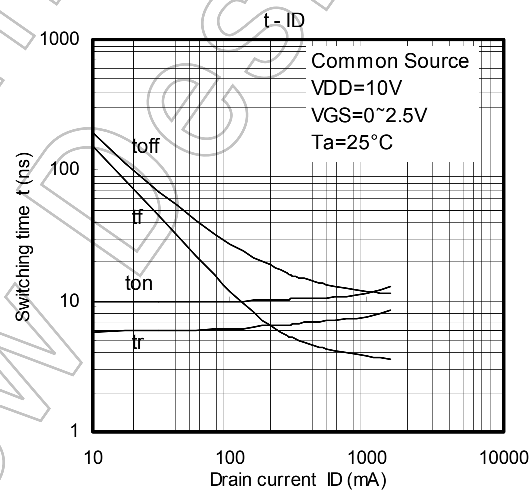


Q1(Nch MOS FET)

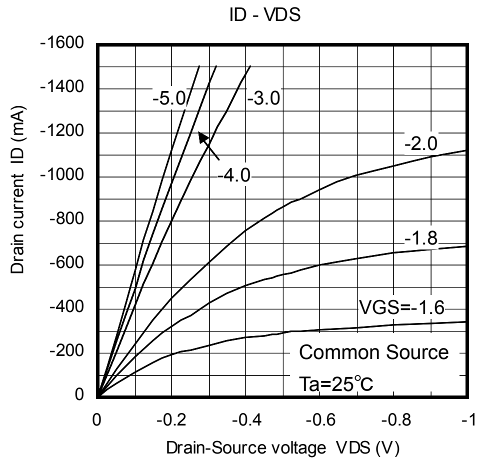


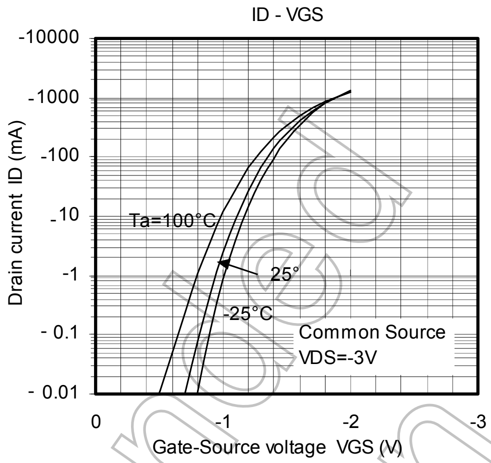


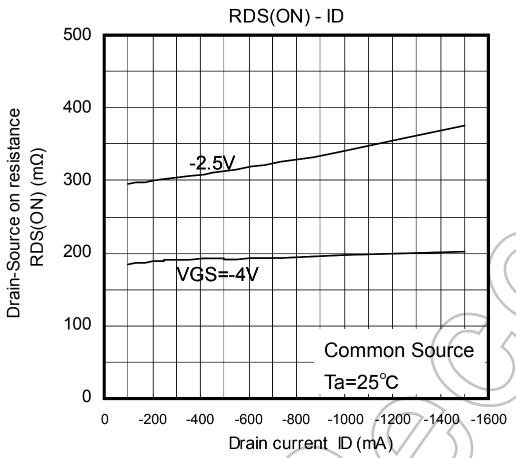


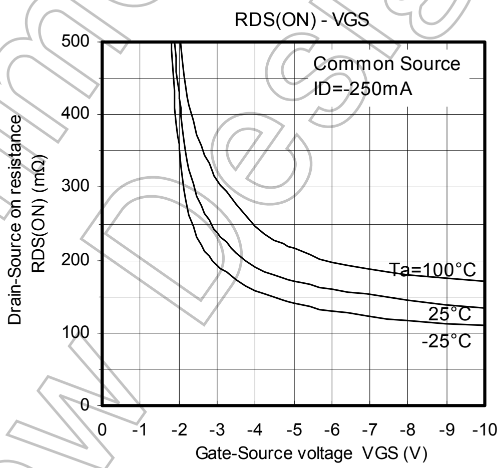


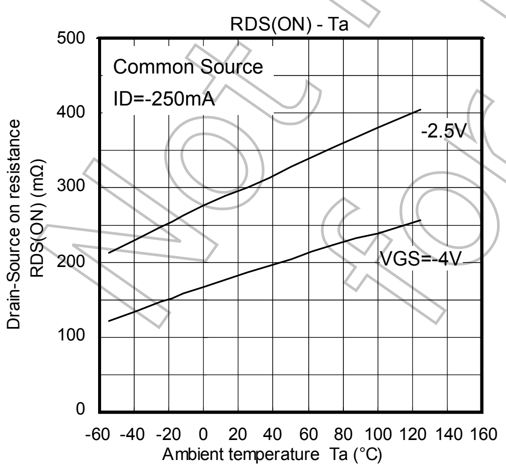
Q2(Pch MOS FET)

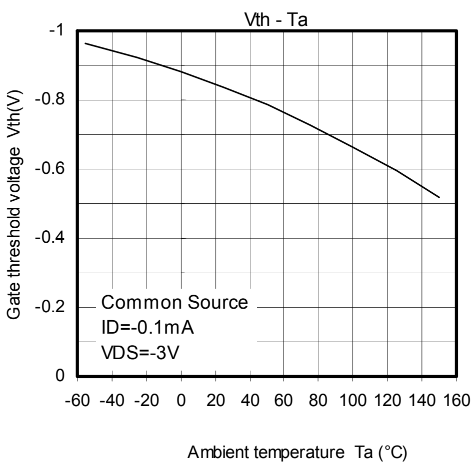




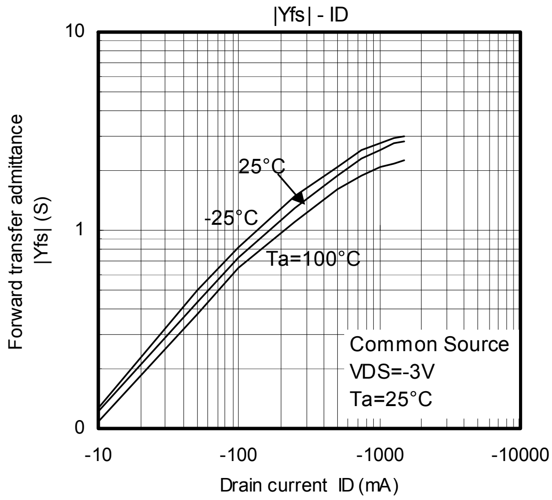


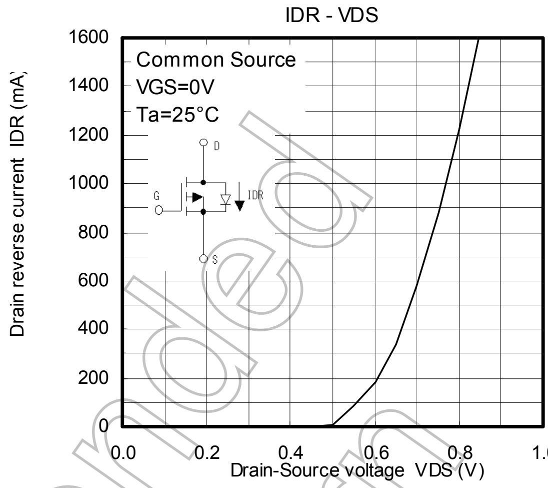


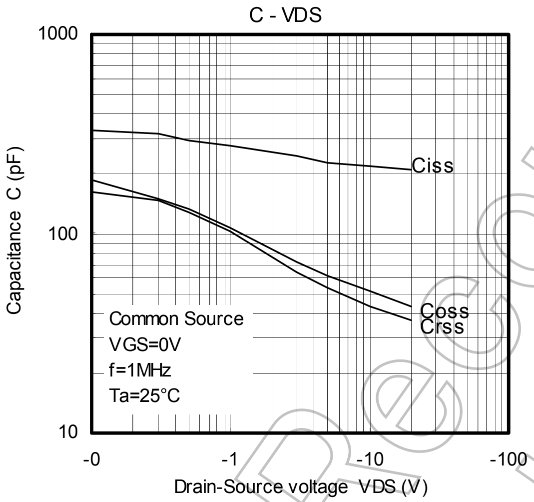


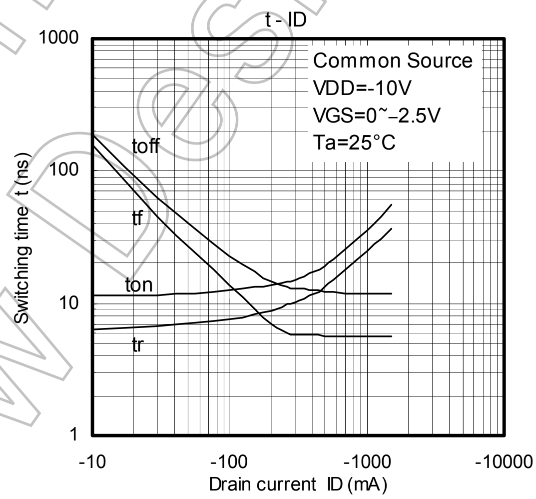


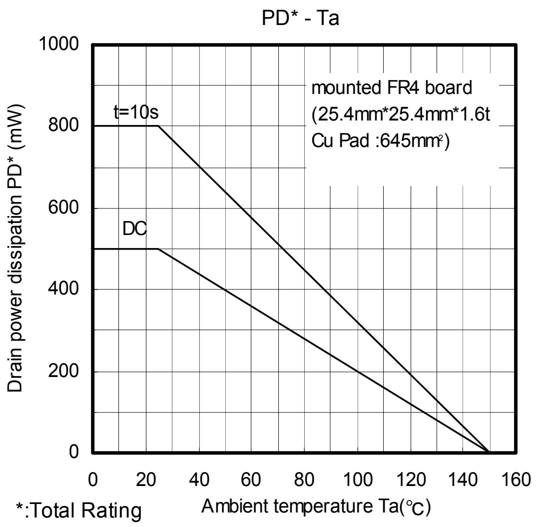
Q2(Pch MOS FET)



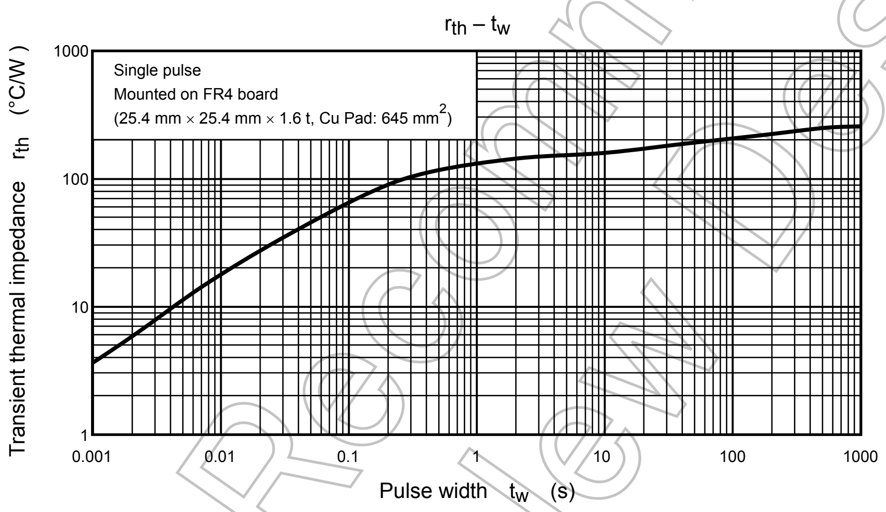








*:Total Rating



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