LDO Regulators with Voltage Detector

200mA / 300mA Output LDO Regulator with 2ch RESET

BD4269FJ-C BD4269EFJ-C

General Description

BD4269FJ-C BD4269EFJ-C are a low quiescent voltage regulator with 45V absolute maximum voltage allowing usage in battery direct-connected systems. IC integrates Power on and under-voltage reset and Input voltage reset for VCC or other voltages. Quiescent current is minimized to optimize the system current consumption. Offers selection of the output current between 200 mA or 300 mA depending on the application.
Power on and under-voltage reset and Input voltage reset threshold voltage can be adjusted by external resistance. Power on and under-voltage reset delay time can programmed set by external capacitor.

Features

- AEC-Q100 Qualifies (Note 1)
- Low ESR ceramic capacitors applicable for output.
- Low drop voltage: PDMOS output transistor
- Power on and under-voltage reset
- Sense input comparator for VCC or other voltage
- Adjustable power on and under-voltage reset and Sense input comparator by external resistance
- Programmable reset delay time by external capacitor.

(Note 1: Grade 1)

Applications

- Onboard vehicle device (body-control, car stereos, satellite navigation system, etc.)

Key Specifications

- Qualified for Automotive Applications
- Input voltage range: -0.3 to +45 V
- Low quiescent current: 70 µA (Typ)
- Output load (BD4269FJ-C): 200 mA
  (BD4269EFJ-C) 300 mA
- Output voltage: 5.0 V ±2 %
- Power on and under-voltage reset detect voltage: 4.62 V ±2.6 %
  (Adjusting detect voltage accuracy:±3 %)
- Over Current Protection (OCP)
- Thermal Shut Down (TSD)

Packages

W (Typ) x D (Typ) x H (Max)

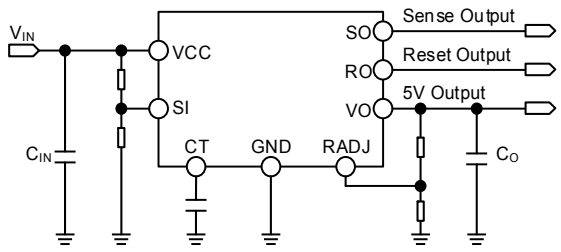
- FJ: SOP-J8 4.90 mm x 6.00 mm x 1.65 mm

- EFJ : HTSOP-J8 4.90 mm x 6.00 mm x 1.00 mm

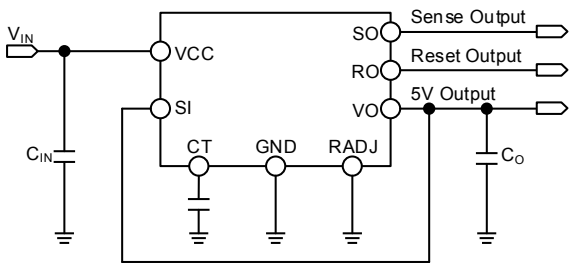
Typical Application Circuits

- VCC and VO pin capacitors: 0.1 µF ≤ C_{IN} (Typ), 6 µF ≤ C_O (Min)
  Please refer to the "Selection of Components Externally Connected".

< Using SI and RADJ >

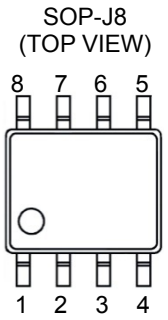


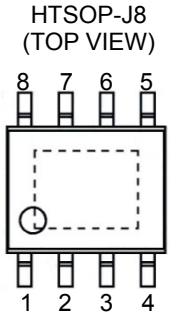
< Not Using SI and RADJ >



○Product structure : Silicon monolithic integrated circuit ○This product is not designed for protection against radioactive rays

Pin Configurations

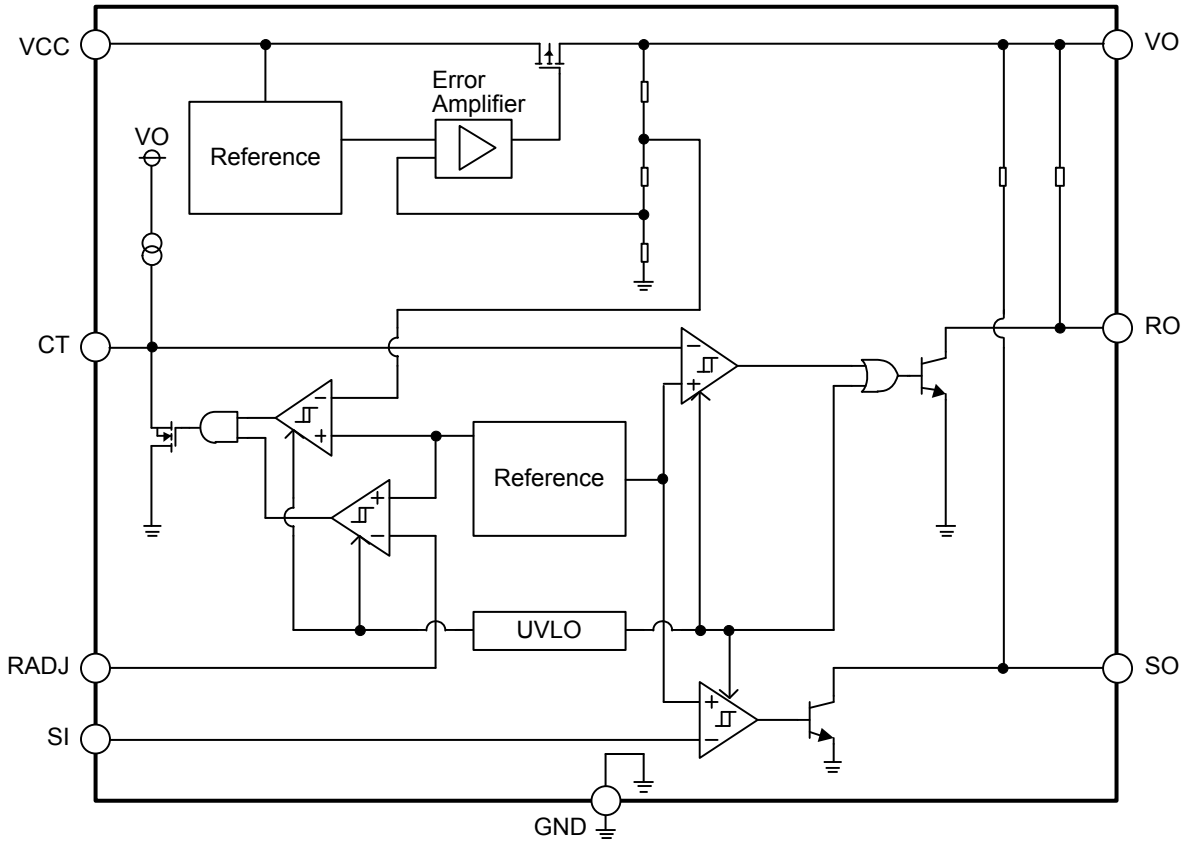




Pin Description

Pin No.	Symbol	Function
1	VCC	Supply voltage input
2	SI	Sense input ; if not needed, connect to VO.
3	RADJ	Power on and under-voltage reset Threshold adjust ; if not needed, connect to GND.
4	CT	Power on and under-voltage reset Delay; connect capacitor to GND for setting delay time.
5	GND	Ground
6	RO	Power on and under-voltage reset output ; the open-collector output is internally linked to VO via a 24 kΩ pull-up resistor. Keep open, if not needed.
7	SO	Input voltage reset output ; the open-collector output is internally linked to VO via a 24 kΩ pull-up resistor. Keep open, if not needed.
8	VO	5 V Output

Block Diagram



Description of Blocks

Block Name	Function	Description of Blocks
Reference	Reference Voltage	The Reference generates the Reference Voltage
Error Amplifier	Error Amplifier	The Error Amplifier amplifies the difference between the feedback voltage of the output voltage and the reference voltage
TSD	Thermal Shutdown Protection	The TSD protect the device from overheating. If the chip temperature (Tj) reaches ca. 175 °C (Typ), the output is turned off.
OCP	Over Current Protection	The OCP protect the device from damage caused by over current.
UVLO	Under Voltage Lock Out	The UVLO prevents malfunction of the reset block in case of very low output voltage.

Absolute Maximum Ratings

Parameter		Symbol	Ratings	Unit
VCC Input Voltage (Note 1)		V_{CC}	-0.3 to + 45.0	V
RADJ Input Voltage		V_{RADJ}	-0.3 to +7.0 (≤ V_O +0.3)	V
RO Input Voltage		R_O	-0.3 to +7.0 (≤ V_O +0.3)	V
VO Input Voltage		V_O	-0.3 to +7.0 (≤ V_O +0.3)	V
SO Input Voltage		S_O	-0.3 to +7.0 (≤ V_O +0.3)	V
SI Input Voltage		V_{SI}	-0.3 to +45.0 (≤ V_{CC} +0.3)	V
Power Dissipation	(SOP-J8) (Note 2)	Pd	0.80	W
	(HTSOP-J8) (Note 3)		0.96	W
Junction Temperature Range		Tj	-40 to + 150	°C
Storage Temperature Range		Tstg	-55 to + 150	°C

(Note 1) Not to exceed Pd.

(Note 2) Reduced by 6.45 mW / °C over Ta = 25 °C, when mounted on glass epoxy board: 114.3 mm x 76.2 mm x 1.6 mm.

(Note 3) Reduced by 7.69 mW / °C over Ta = 25 °C, when mounted on glass epoxy board: 114.3 mm x 76.2 mm x 1.6 mm.

Caution: Exceeding the absolute maximum rating for supply voltage, operating temperature or other parameters can result in damages to or destruction of the chip. In this event it also becomes impossible to determine the cause of the damage (e.g. short circuit, open circuit, etc.). Therefore, if any special mode is being considered with values expected to exceed the absolute maximum ratings, implementing physical safety measures, such as adding fuses, should be considered.

Recommended Operating Conditions (-40 °C ≤ Tj ≤ +150 °C)

Parameter		Symbol	Min	Max	Unit
Supply Voltage (I_O ≤ 100mA) (Note 1)		V_{CC}	5.5	45.0	V
Supply Voltage (I_O ≤ 200mA) (Note 1)		V_{CC}	6.0	45.0	V
Start Up Voltage		V_{CC}	3.0	-	V
VO Operating Voltage for RO		V_{OPR}	1.0	-	V
VO Operating Voltage for SO		V_{OPS}	3.5	-	V
Power on and Under-Voltage Reset Switching Threshold Adjustable Range		V_{RTADJ}	3.5	4.5	V
SI Input Voltage		V_{SI}	0	V_{CC}	V
RADJ Input Voltage		V_{RADJ}	0	V_O	V
Output Current	(SOP-J8)	I_O	0	200	mA
	(HTSOP-J8)		0	300	mA
Operating Temperature Range		Ta	-40	+125	°C

(Note 1) Not to exceed Pd.

Thermal Characteristics (Note 1)

Parameter	Symbol	Typ.	Unit	Conditions
SOP-J8				
Junction to Ambient	θ_{JA}	155	°C / W	1s (Note 2)
		87	°C / W	2s2p (Note 3)
Junction to Top Center of Case (Note 4)	Ψ_{JT}	15	°C / W	1s (Note 2)
		13	°C / W	2s2p (Note 3)
HTSOP-J8				
Junction to Ambient	θ_{JA}	130	°C / W	1s (Note 2)
		34	°C / W	2s2p (Note 3)
Junction to Top Center of Case (Note 4)	Ψ_{JT}	15	°C / W	1s (Note 2)
		7	°C / W	2s2p (Note 3)

(Note 1) The thermal impedance is based on JESD51 - 2A (Still - Air) standard.
(Note 2) JESD51 - 3 standard FR4 114.3 mm x 76.2 mm x 1.57 mm 1 - layer (1s)
(Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.)
(Note 3) JESD51 - 5 / - 7 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 4 - layer (2s2p)
(Top copper foil: ROHM recommended footprint + wiring to measure /
2 inner layers and copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm,
copper (top & reverse side / inner layers) 2oz. / 1oz.)
(Note 4) T_T : Top center of case's (mold) temperature

Electrical Characteristics

(Unless otherwise specified, Tj = -40 °C to +150 °C, V_{CC} = 13.5 V)

Parameter		Symbol	Limits			Unit	Conditions
			Min	Typ	Max		
Circuit current		I_{CC}	-	70	150	μA	I_O = 0 mA to 200 mA
Output voltage		V_Q	4.90	5.00	5.10	V	1 mA ≤ I_O ≤ 100 mA 6 V ≤ V_{CC} ≤ 16 V
Dropout voltage		ΔVd	-	0.25	0.50	V	V_{CC} = 4.75 V, I_O = 100 mA
Load regulation		Reg.L	-	10	30	mV	I_O = 10 mA to 100 mA
Line regulation		Reg.I	-	10	30	mV	V_{CC} = 8 V to 16 V, I_O = 1 mA
Current limit	BD4269FJ-C	I_{OCP}	200	-	-	mA	-
	BD4269EFJ-C		300	-	-	mA	-
Thermal Shut Down Temperature		T_{TSD}	-	175	-	°C	-

Electrical Characteristics (Power on and under-voltage reset)

(Unless otherwise specified, Tj = -40 °C to +150 °C, V_{CC} = 13.5 V)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Power on and under-voltage reset Switching threshold	V_{RT}	4.50	4.62	4.74	V	-
Power on and under-voltage reset Switching Hysteresis	V_{RHY}	20	60	100	mV	-
RADJ switching threshold	$V_{RADJ,TH}$	0.776	0.800	0.824	V	3.5 V ≤ Vo ≤ 4.5 V
RADJ input current	I_{RADJ}	-1	0	+1	μA	V_{RADJ} = 2 V
RO pull-up resistance	R_{RO}	10	24	40	kΩ	-
CT threshold high	V_{CTH}	-	1.20	-	V	-
CT threshold low	V_{CTL}	-	0.25	-	V	-
CT Charge current	I_{CT}	5	12	20	μA	V_{CT} = 0.5 V
Delay time L→H (Power On Reset Time)	T_{DLH}	17	22	28	ms	C_{CT} = 0.22 μF (Note 1)

(Note 1) T_{DLH} can be varied by changing the CT capacitance value. (0.001μF to 10 μF available)

T_{DLH} (ms) ≈ T_{DLH0} (Delay time L→H at C_{CT} = 0.22 μF) × C_{CT} (μF) / 0.22 C_{CT} : 0.1μF ≤ C_{CT} ≤ 10 μF
example: When C_{CT}= 2.2μF, 170ms ≤ T_{POR} ≤ 280 ms

T_{DLH} (ms) ≈ T_{DLH0} (Delay time L→H at C_{CT} = 0.22 μF) × C_{CT} (μF) / 0.22 ±0.1 C_{CT}: 0.001μF ≤ C_{CT} < 0.1 μF
example: When C_{CT}= 0.022μF, 1.6ms ≤ T_{DLH} ≤ 2.9 ms

Electrical Characteristics (Input voltage reset)

(Unless otherwise specified, Tj = -40 °C to 150 °C, V_{CC} = 13.5 V)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
SI threshold high	V_{SIH}	0.80	0.87	0.94	V	-
SI threshold low	V_{SIL}	0.75	0.80	0.85	V	-
SO pull-up resistance	R_{so}	10	24	40	kΩ	-
SI input current	I_{SI}	-1	0	+1	μA	V_{SI} = 2 V

Typical Performance Curves (Unless otherwise specified, Tj = 25 °C, V_{CC} = 13.5 V)

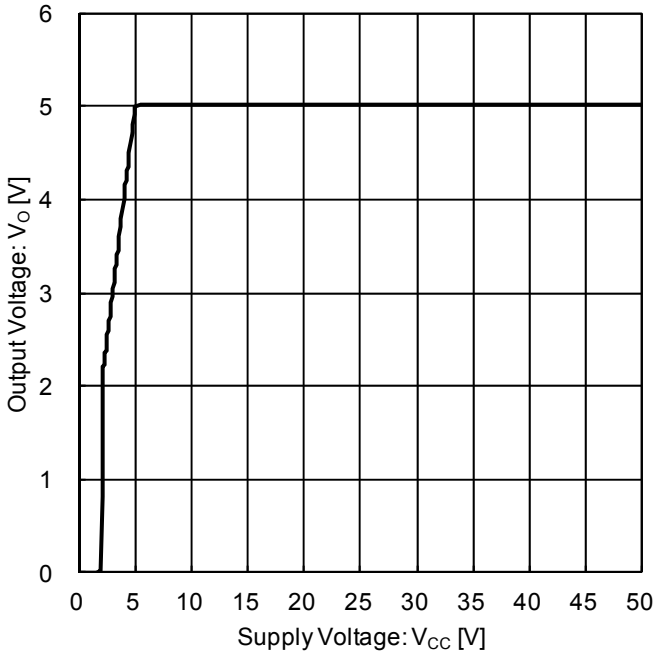


Figure 1. Output Voltage vs. Supply Voltage
(R_L = open)

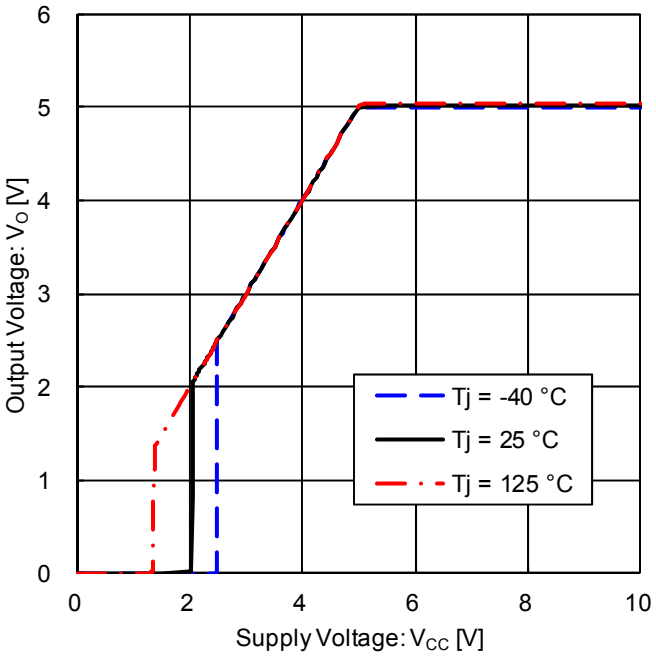


Figure 2. Output Voltage vs. Supply Voltage
(at low Supply Voltage: R_L = open)

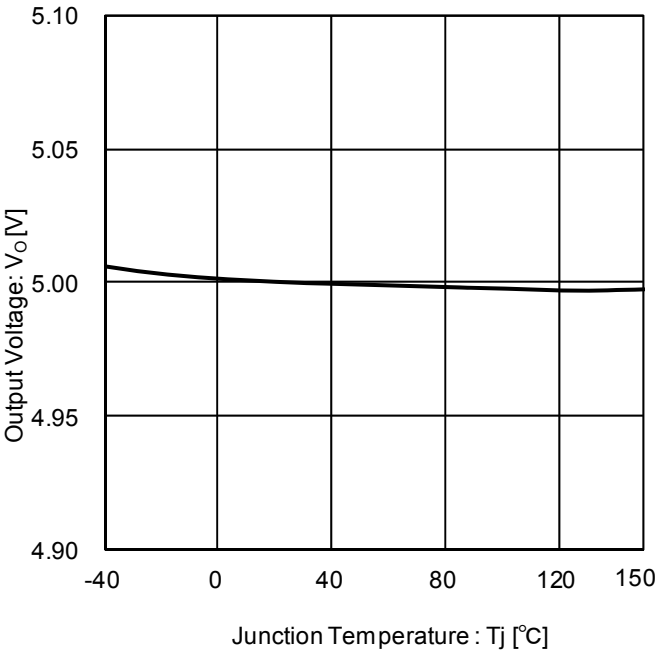


Figure 3. Output Voltage vs. Junction Temperature
(R_L = 1 kΩ)

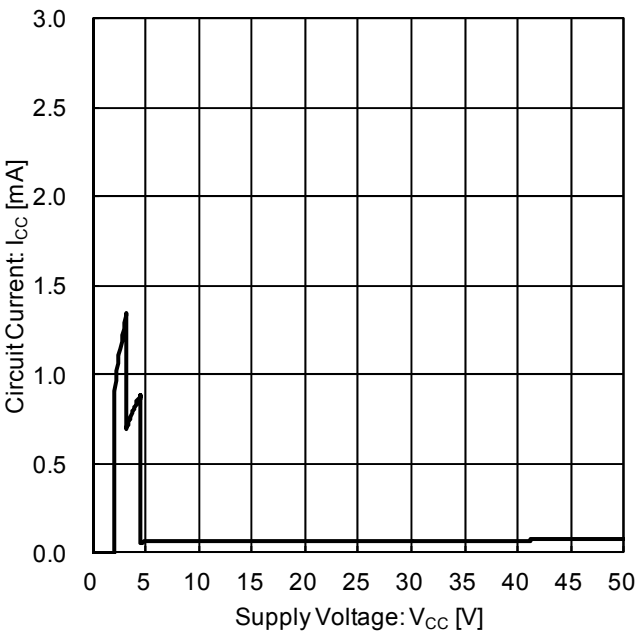


Figure 4. Circuit Current vs. Supply Voltage

Typical Performance Curves (Unless otherwise specified, Tj = 25 °C, V_{CC} = 13.5 V) -Continued

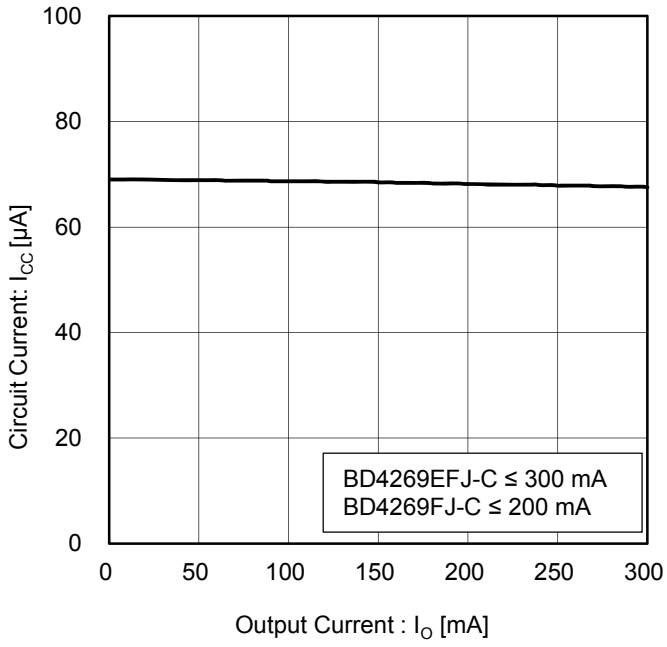


Figure 5. Circuit Current vs. Output Current

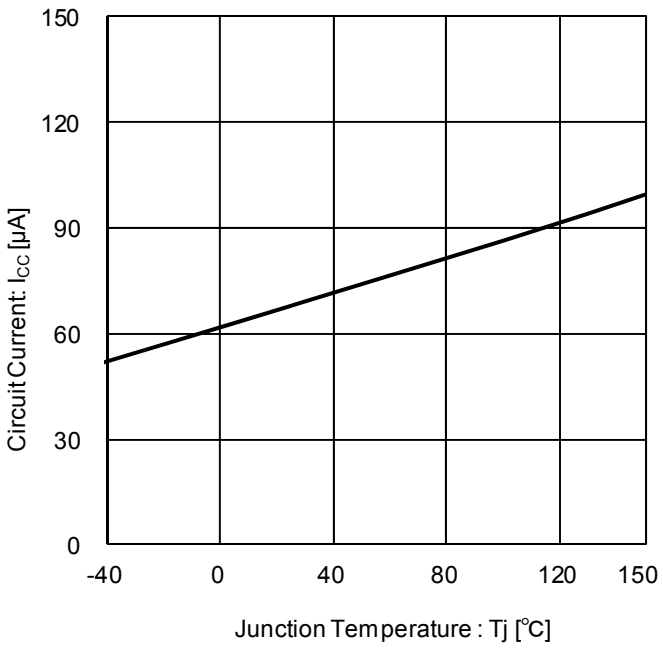


Figure 6. Circuit Current vs. Junction Temperature

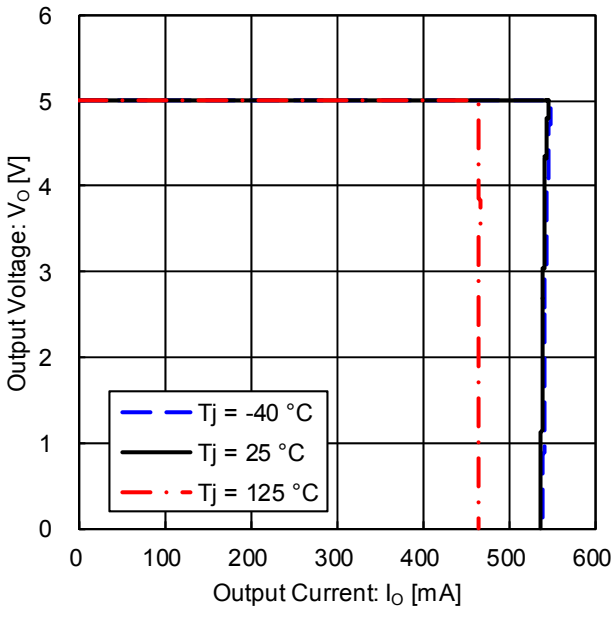


Figure 7. Output Voltage vs. Output Current (Over Current Protection)

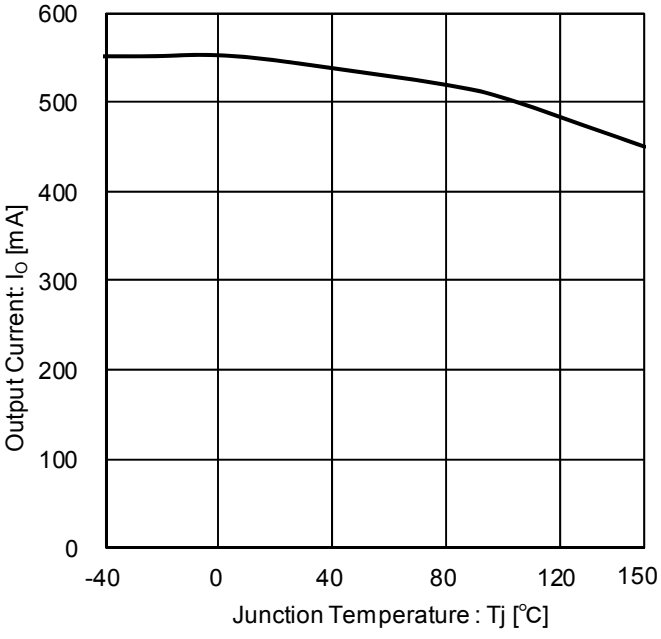


Figure 8. Output Current vs. Junction Temperature

Typical Performance Curves (Unless otherwise specified, Tj = 25 °C, V_{CC} = 13.5 V) -Continued

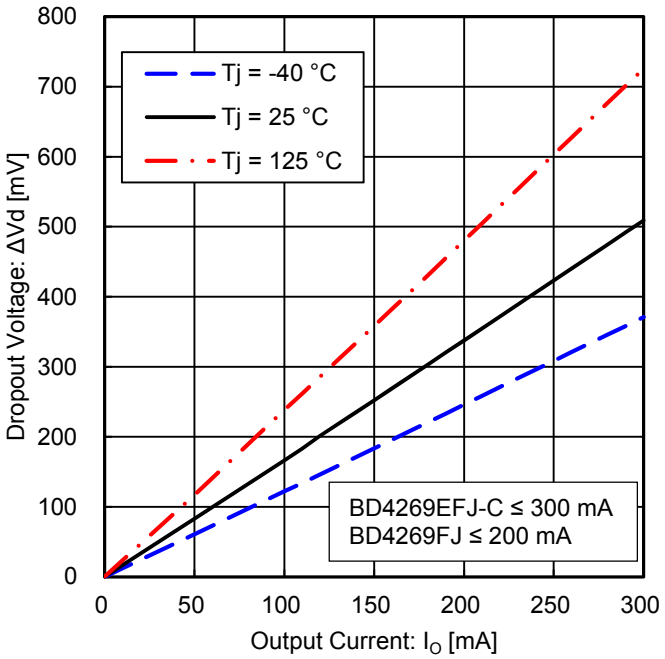


Figure 9. Dropout Voltage vs. Output Current (V_{CC} = 4.75 V)

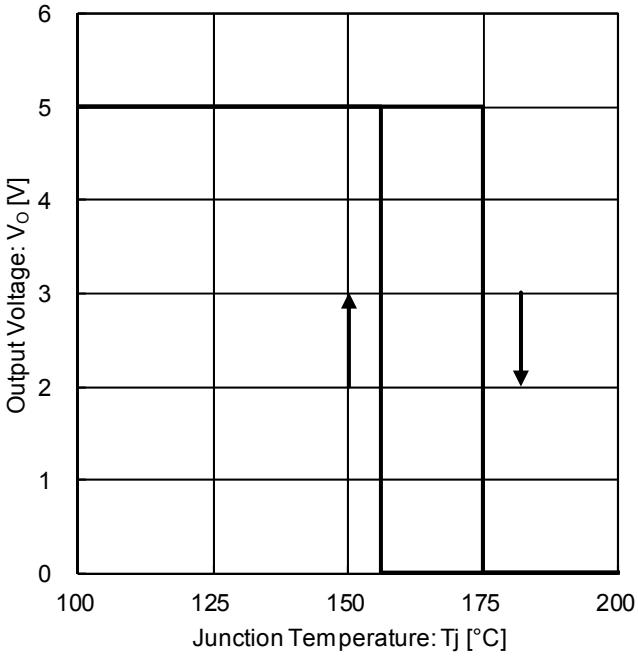


Figure 10. Output Voltage vs. Junction Temperature (Thermal Shut Down)

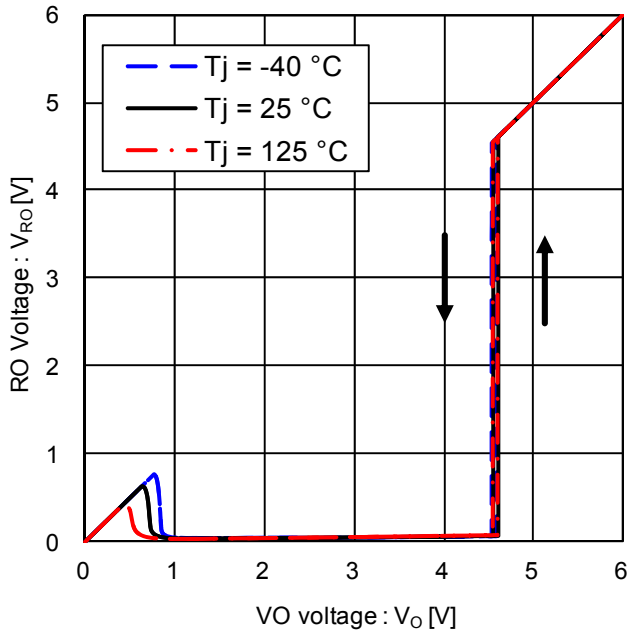


Figure 11. RO Voltage vs. VO Voltage

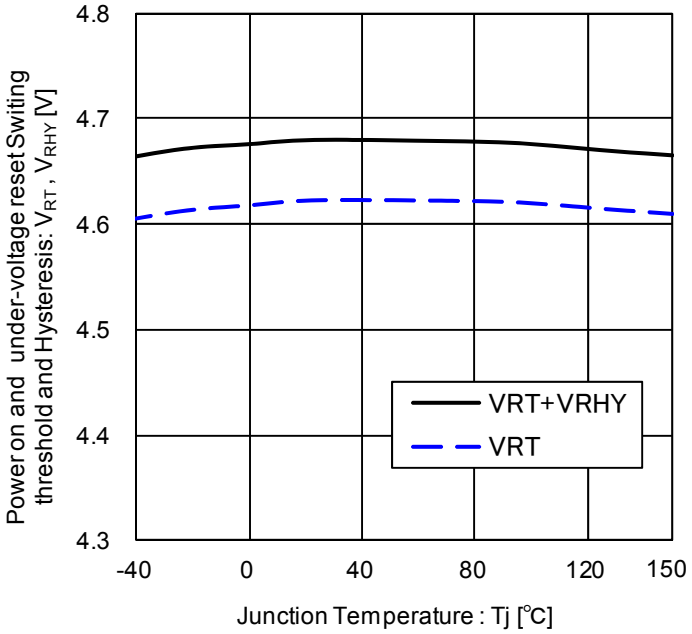


Figure 12. Power on and under-voltage reset Switing threshold and Hysteresis vs. Junction Temperature

Typical Performance Curves (Unless otherwise specified, Tj = -40 °C to 150 °C, V_{CC} = 13.5 V) -Continued

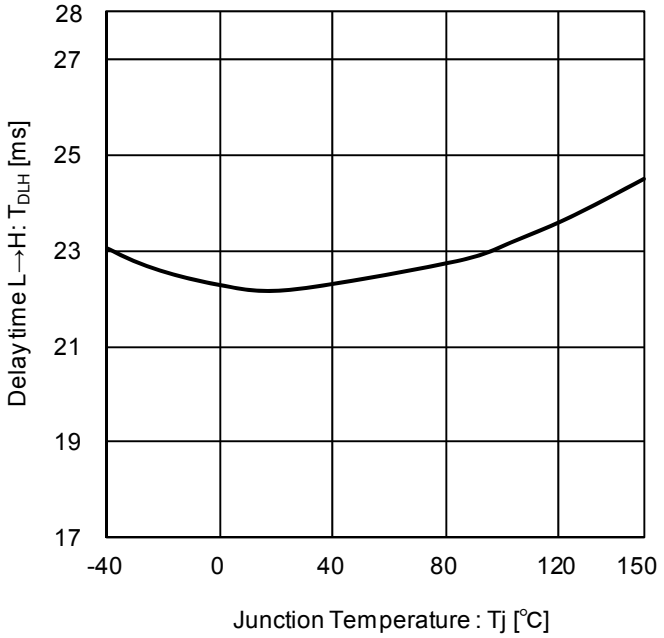


Figure 13. Delay Time L→H vs. Junction Temperature (C_{CT} = 0.22 µF)

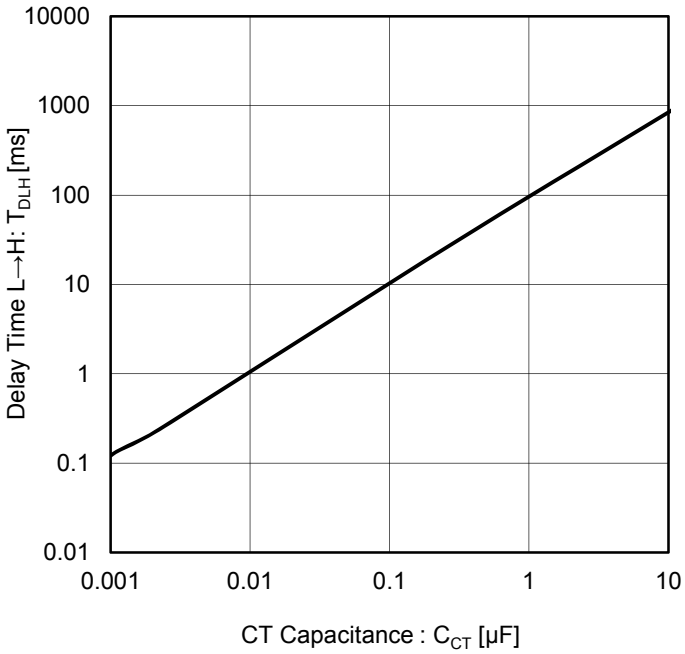


Figure 14. Delay Time L→H vs. CT Capacitance

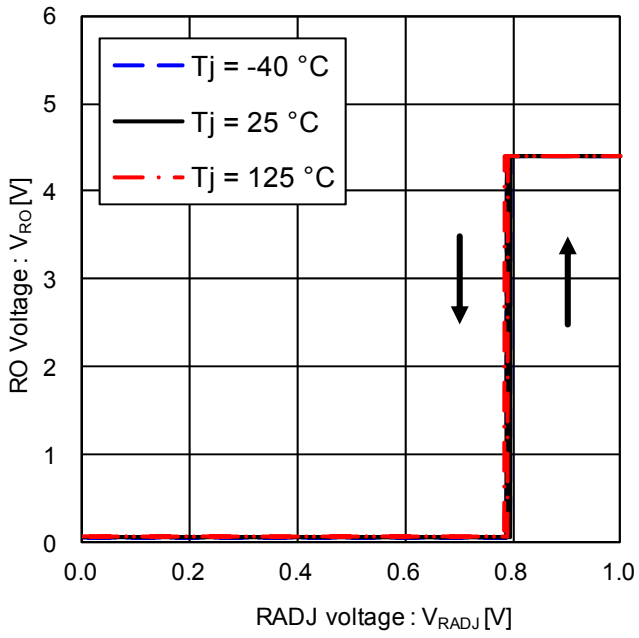


Figure 15. RO Voltage vs. RADJ Voltage

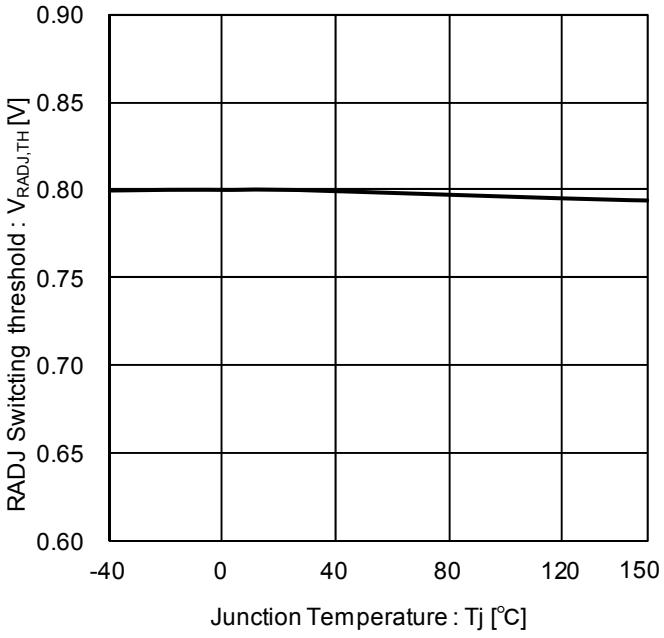


Figure 16. RADJ switching threshold vs. Junction Temperature

Typical Performance Curves (Unless otherwise specified, Tj = -40 °C to 150 °C, V_{CC} = 13.5 V) -Continued

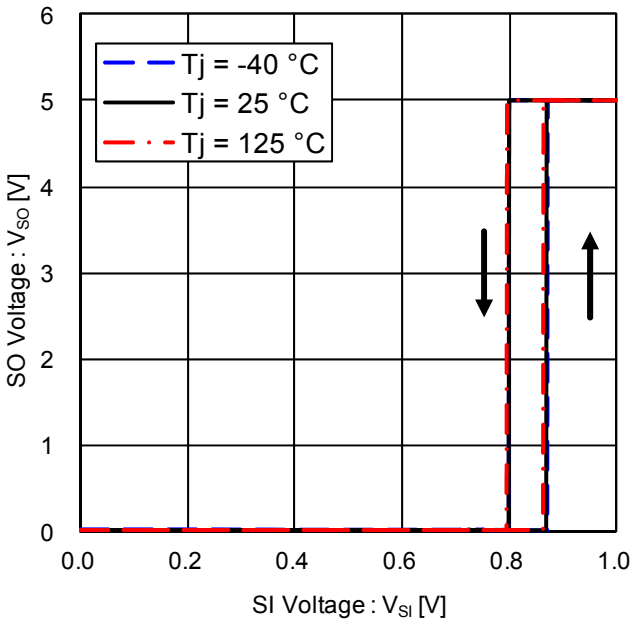


Figure 17. SO Voltage vs. SI Voltage

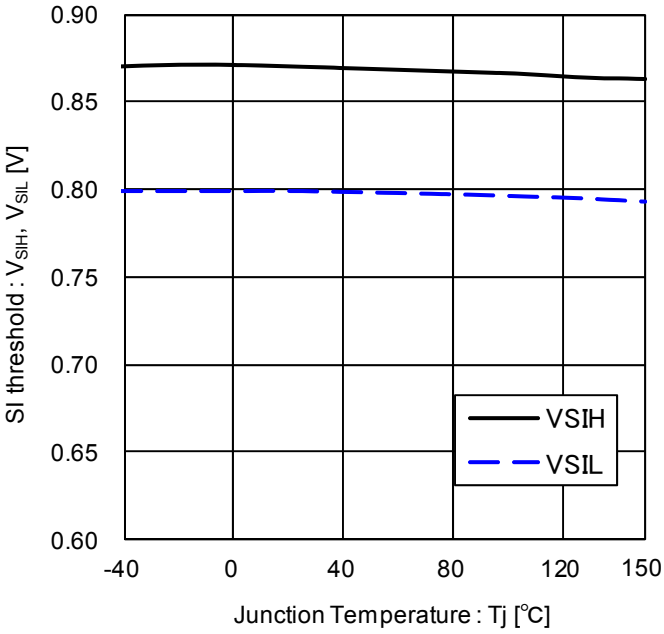
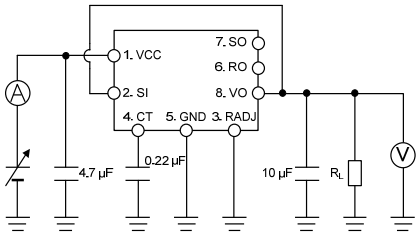
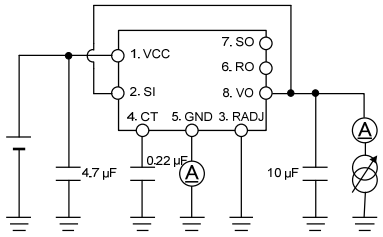


Figure 18. SI threshold vs. Junction Temperature

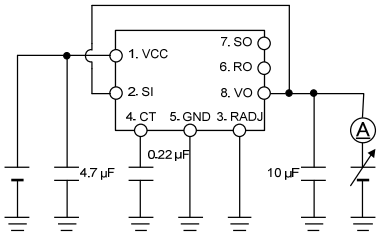
Measurement circuit for Typical Performance Curves



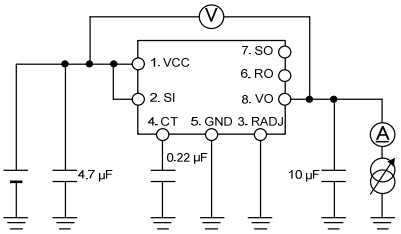
Measurement Circuit for
Figure 1, 2, 3, 4, 6, 10



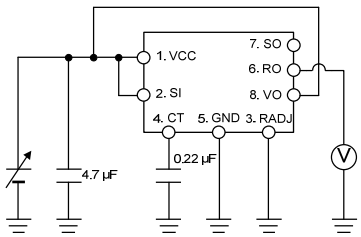
Measurement Circuit for
Figure 5



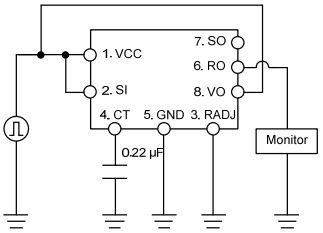
Measurement Circuit for
Figure 7, 8



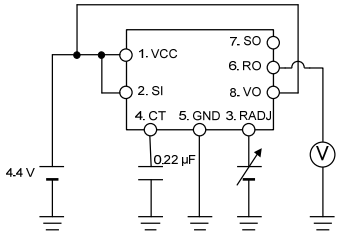
Measurement Circuit for
Figure 9



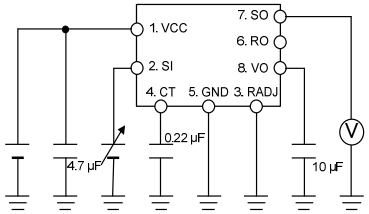
Measurement Circuit for
Figure 11, 12



Measurement Circuit for
Figure 13, 14



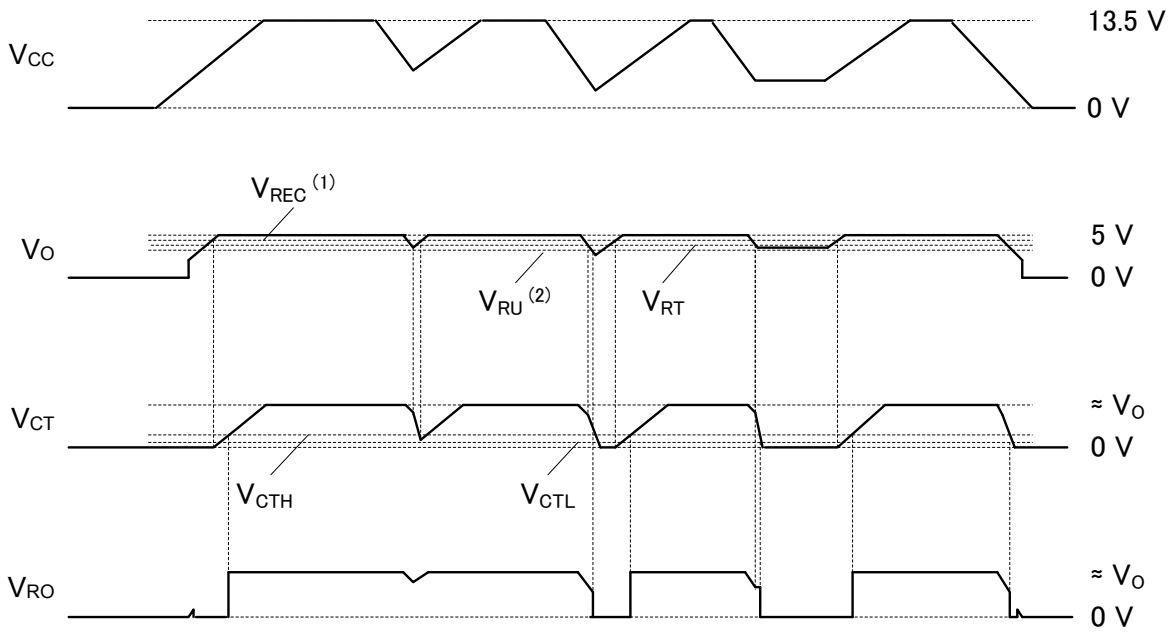
Measurement Circuit for
Figure 15, 16



Measurement Circuit for
Figure 17, 18

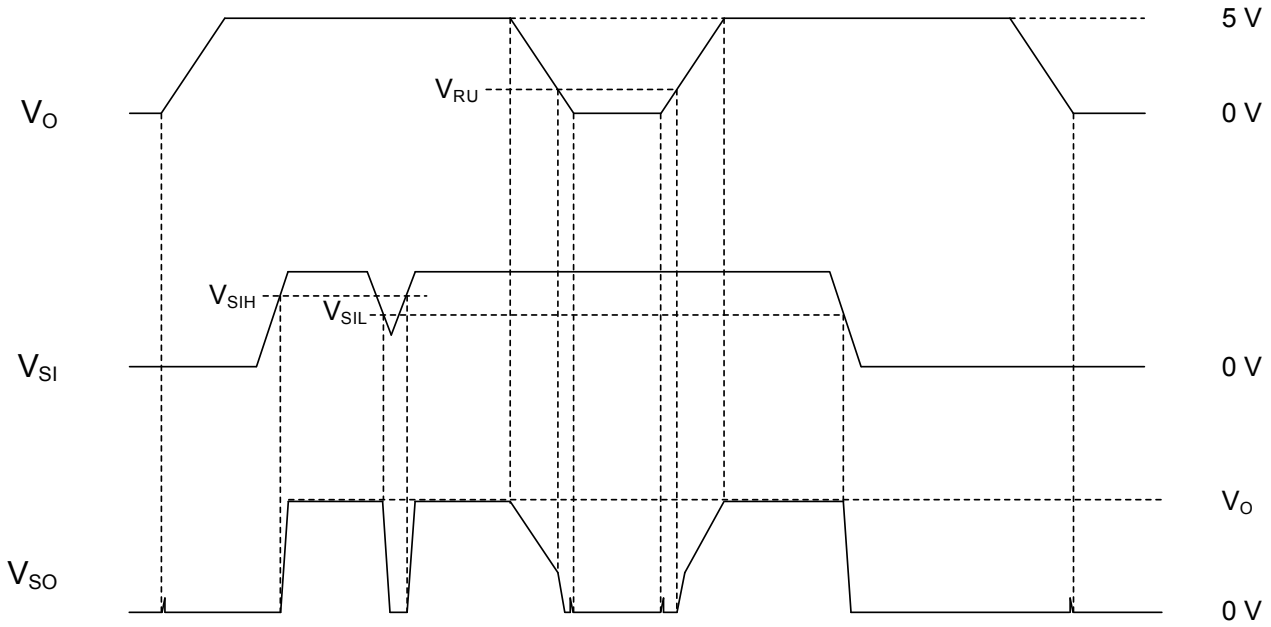
Timing Chart

1. Power on and under-voltage reset (RADJ is connected to GND)



(1) $V_{REC} = V_{RT} + V_{RHY}$
(2) V_{RU} = 2 to 3.5 V
(3) When RADJ is used, $V_{RT} = V_{RTADJ}$, $V_{REC} = V_{RTADJ} + V_{RHY}$

2. Input voltage reset



Selection of Components Externally Connected

・VCC pin capacitor

Insert capacitors with a capacitance of 0.1 μF or higher between the VCC and GND pin. We recommend using ceramic capacitor generally featuring good high frequency characteristic. When selecting a ceramic capacitor, please be consider about temperature and DC - biasing characteristics. Place capacitors closest possible to VCC - GND pin. When input impedance is high, e.g. in case there is distance from battery, line voltage drop needs to be prevented by large capacitor. Choose the capacitance according to the line impedance between the power smoothing circuit and the VCC pin. Selection of the capacitance also depends on the applications. Verify the application and allow sufficient margins in the design. We recommend using a capacitor with excellent voltage and temperature characteristics.

・Output pin capacitor

In order to prevent oscillation, a capacitor needs to be placed between the output pin and GND pin. We recommend using a ceramic capacitor with a capacitance of 6 μF or higher. In selecting the capacitor, ensure that the capacitance of 6 μF or higher is maintained at the intended applied voltage and temperature range. Due to changes in temperature the capacitor's capacitance can fluctuate possibly resulting in oscillation.

In actual applications the stable operating range is influenced by the PCB impedance, input supply impedance and load impedance. Therefore verification of the final operating environment is needed. When selecting a ceramic capacitor, we recommend using X7R or better components with excellent temperature and DC - biasing characteristics and high voltage tolerance.

In case of the transient input voltage and the load current fluctuation, output voltage may fluctuate. In case this fluctuation can be problematic for the application, connect low ESR capacitor (capacitance > 6 μF, ESR < 1 Ω) in paralleled to large capacitor with a capacitance of 13 μF or higher and ESR of 5 Ω or lower. Electrolytic and tantalum capacitors can be used as large capacitor. When selecting an electrolytic capacitor, please consider about increasing ESR and decreasing capacitance at cold temperature.

Place the capacitor closest possible to output pin.

・RADJ pin

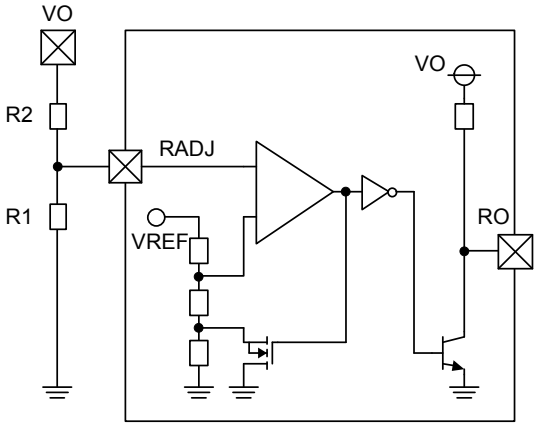


Figure 19. RADJ pin configuration method

Power on and under-voltage reset threshold is changed by connecting external resister R1 and R2 in Figure 19.The available resister range is from

$$V_O = V_{RADJ,TH} \times \frac{R1 + R2}{R1}$$

(R1 and R2 recommended resistance values are 100 kΩ or lower.)

Power on and under-voltage reset is adjusted in from 3.5V to 4.5V. In case that it is needless to RADJ pin, it must be short GND. If it is open, the reset function can be unstable.

・SI pin

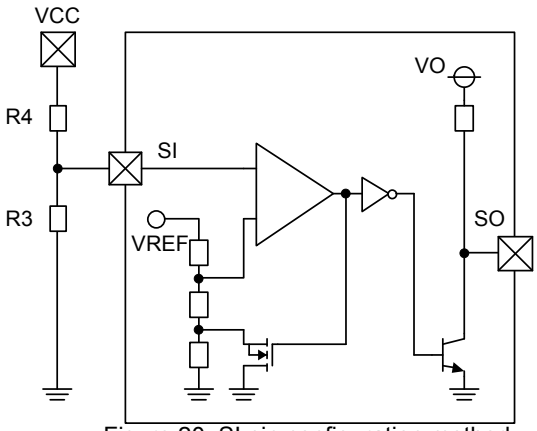


Figure 20. SI pin configuration method

Input voltage reset threshold is changed by connecting external resister R3 and R4 in Figure 20. The adjusted reset threshold V_{SIADJL} and V_{SIADJH} can be calculated by following equation.

$$V_{CC} = V_{SIL} \times \frac{R3 + R4}{R3}$$

(R3 and R4 recommended resistance values are 100 kΩ or lower.)

This IC incorporates UVLO circuit to prevent malfunction of the reset block in case of very low output voltage. When UVLO is activated, SO is L regardless of SI voltage. When SI is used, set $V_O \geq 3.5$ V.

In case that it is needless to SI pin, it must be short VO. If it is open, the reset function can be unstable.

Power Dissipation

■SOP-J8

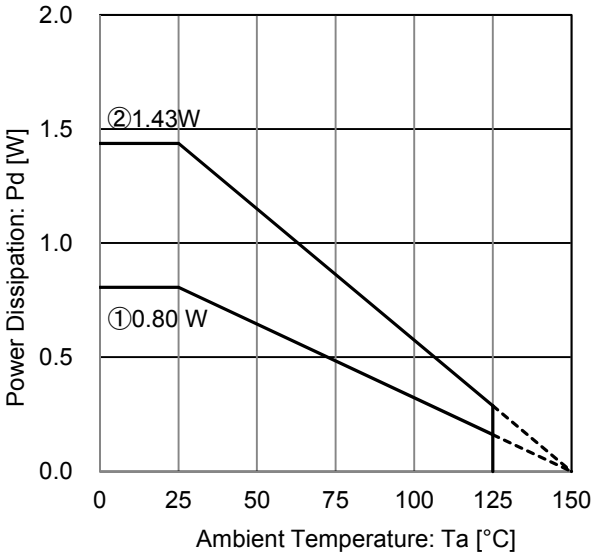


Figure 21. SOP-J8 Package Data
(Reference Data)

IC mounted on ROHM standard board based on JEDEC.
① : 1 - layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.57 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.

② : 4 - layer PCB
(2 inner layers and Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.60 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB
: 74.2 mm x 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB
: 74.2 mm x 74.2 mm, 2 oz. copper.

Condition①: θ_{JA} = 155 °C / W, Ψ_{JT} (top center) = 15 °C / W
Condition②: θ_{JA} = 87 °C / W, Ψ_{JT} (top center) = 13 °C / W

■HTSOP-J8

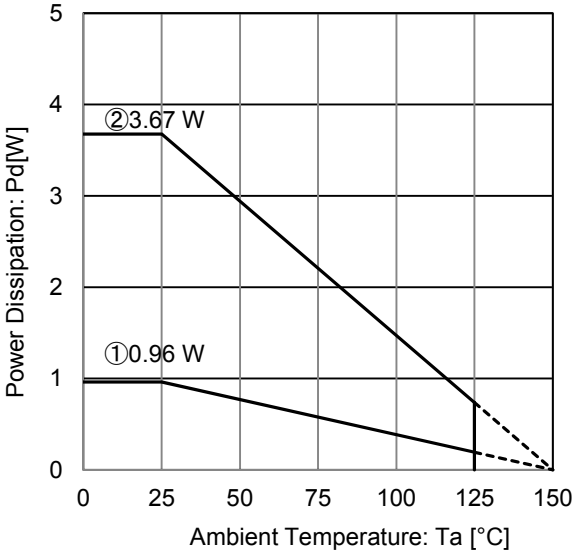


Figure 22. HTSOP-J8 Package Data
(Reference Data)

IC mounted on ROHM standard board based on JEDEC.
① : 1 - layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.57 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.

② : 4 - layer PCB
(2 inner layers and Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm)
Board material: FR4
Board size: 114.3 mm x 76.2 mm x 1.60 mmt
Mount condition: PCB and exposed pad are soldered.
Top copper foil: ROHM recommended
footprint + wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB
: 74.2 mm x 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB
: 74.2 mm x 74.2 mm, 2 oz. copper.

Condition①: θ_{JA} = 130 °C / W, Ψ_{JT} (top center) = 15 °C / W
Condition②: θ_{JA} = 34 °C / W, Ψ_{JT} (top center) = 7 °C / W

Thermal Design

Within this product, the power consumption is decided by the dropout voltage condition, the load current and the circuit current. Refer to Package Data illustrated in Figure 21, 22 when using the IC in an environment of Ta ≥ 25 °C. Even if the ambient temperature Ta is at 25 °C, depending on the input voltage and the load current, chip junction temperature can be very high. Consider the design to be Tj ≤ Tjmax = 150 °C in all possible operating temperature range. On the reverse side of the package BD4269EFJ-C has an exposed heat pad for improving the heat dissipation.
Should by any condition the maximum junction temperature Tjmax = 150 °C rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature Tj.
Tj can be calculated by either of the two following methods.

1. The following method is used to calculate the junction temperature Tj.

$$Tj = Ta + P_C \times \theta_{JA}$$

Where:
Tj : Junction Temperature
Ta : Ambient Temperature
P_C : Power Consumption
θ_{JA} : Thermal Impedance (Junction to Ambient)

2. The following method is also used to calculate the junction temperature Tj.

$$Tj = T_T + P_C \times \Psi_{JT}$$

Where:
Tj : Junction Temperature
T_T : Top Center of Case's (mold) Temperature
P_C : Power consumption
Ψ_{JT} : Thermal Impedance (Junction to Top Center of Case)

The following method is used to calculate the power consumption Pc (W).

$$Pc = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{CC}$$

Where:
P_C : Power Consumption
V_{CC} : Input Voltage
V_O : Output Voltage
I_O : Load Current
I_{CC} : Circuit Current

・Calculation Example (SOP-J8)

If V_{CC} = 13.5 V, V_O = 5.0 V, I_O = 50 mA, I_{CC} = 70 μA, the power consumption Pc can be calculated as follows:

$$P_C = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{CC}$$
$$= (13.5\ V - 5.0\ V) \times 50\ mA + 13.5\ V \times 70\ \mu A$$
$$= 0.43\ W$$

At the ambient temperature Tamax = 85°C, the thermal Impedance (Junction to Ambient)θ_{JA} = 87 °C / W (4-layer PCB),

$$Tj = Tamax + P_C \times \theta_{JA}$$
$$= 85\ ℃ + 0.43\ W \times 87\ ℃ / W$$
$$= 122.5\ ℃$$

When operating the IC, the top center of case's (mold) temperature T_T = 100 °C、Ψ_{JT} = 15 °C / W (1-layer PCB),

$$Tj = T_T + P_C \times \Psi_{JT}$$
$$= 100\ ℃ + 0.43\ W \times 15\ ℃ / W$$
$$= 106.5\ ℃$$

For optimum thermal performance, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad.

・Calculation Example (HTSOP-J8)

If V_{CC} = 13.5 V, V_O = 5.0 V, I_O = 50 mA, I_{CC} = 70 μA, the power consumption Pc can be calculated as follows:

$$P_C = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{CC}$$
$$= (13.5\ V - 5.0\ V) \times 50\ mA + 13.5\ V \times 70\ \mu A$$
$$= 0.43\ W$$

At the ambient temperature Tamax = 85°C, the thermal impedance (Junction to Ambient) θ_{JA} = 34 °C / W (4-layer PCB),

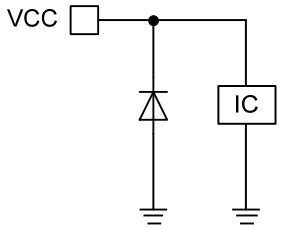
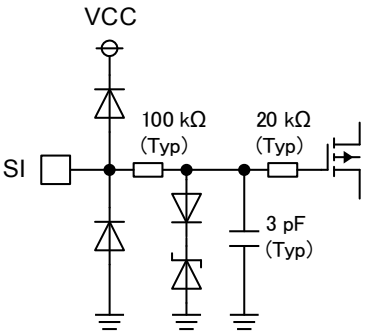
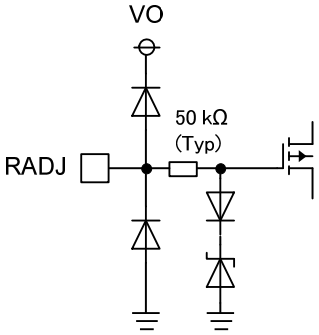
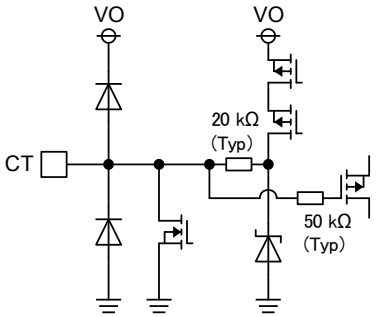
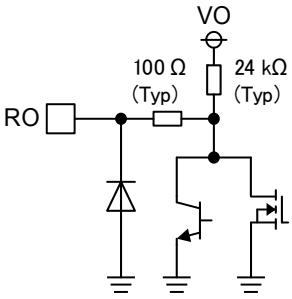
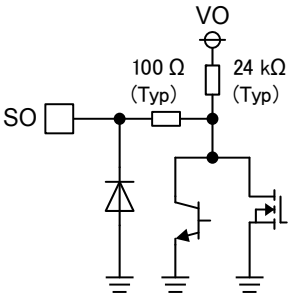
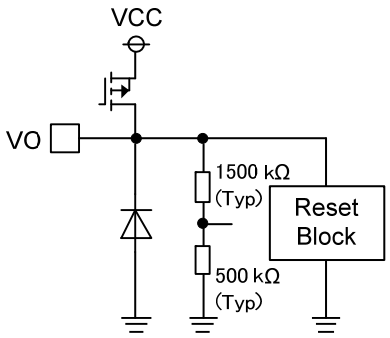
$$Tj = Tamax + P_C \times \theta_{JA}$$
$$= 85\ ℃ + 0.43\ W \times 34\ ℃ / W$$
$$= 99.7\ ℃$$

When operating the IC, the top center of case's (mold) temperature T_T = 100 °C, Ψ_{JT} = 15 °C / W (1-layer PCB),

$$Tj = T_T + P_C \times \Psi_{JT}$$
$$= 100\ ℃ + 0.43\ W \times 15\ ℃ / W$$
$$= 106.5\ ℃$$

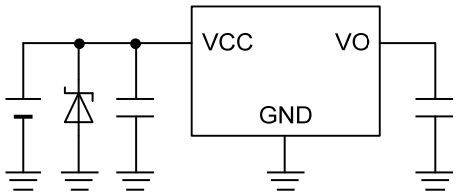
For optimum thermal performance, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad.

I/O equivalence circuits

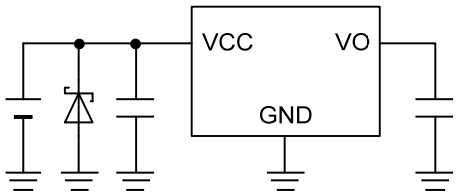
1 VCC	2 SI	3 RADJ
		
4 CT	**6 RO**	**7 SO**
		
8 VO		
		

Application Examples

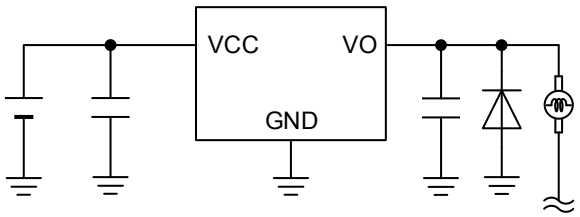
・Applying positive surge to the VCC
If the possibility exists that surges higher than 45 V will be applied to the VCC, a Zener Diode should be placed between the VCC and GND as shown in the figure below.



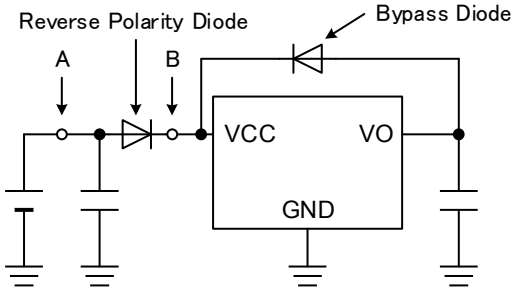
・Applying negative surge to the VCC
If the possibility exists that negative surges lower than the GND are applied to the VCC, a Shottky Diode should be place between the VCC and GND as shown in the figure below.



・Implementing a Protection Diode
If the possibility exists that a large inductive load is connected to the output pin resulting in back-EMF at time of startup and shutdown, a protection diode should be placed as shown in the figure below.



・Reverse Polarity Diode
In some applications, the VCC and the VO potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, the accumulated charge in the output pin capacitor flowing backward from the VO to the VCC when the VCC shorts to the GND. In order to minimize the damage in such case, use a capacitor with a capacitance less than 1000 µF. Also by inserting a reverse polarity diode in series to the VCC, it can prevent reverse current from reverse battery connection or the case. When the point A is short-circuited GND, if there may be any possible case point B is short-circuited to GND, we also recommend using a bypass diode between the VCC and the VO.



Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed for in the thermal design. On the reverse side of the package BD4269EFJ-C has an exposed heat pad for improving the heat dissipation. Use both the front and reverse side of the PCB to increase the heat dissipation pattern as far as possible. The amount of heat generated depends on the voltage difference across the input and output, load current, and bias current. Therefore, when actually using the chip, ensure that the generated heat does not exceed the Pd rating.
   Should by any condition the maximum junction temperature Tjmax = 150 °C rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Terminals**
    Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

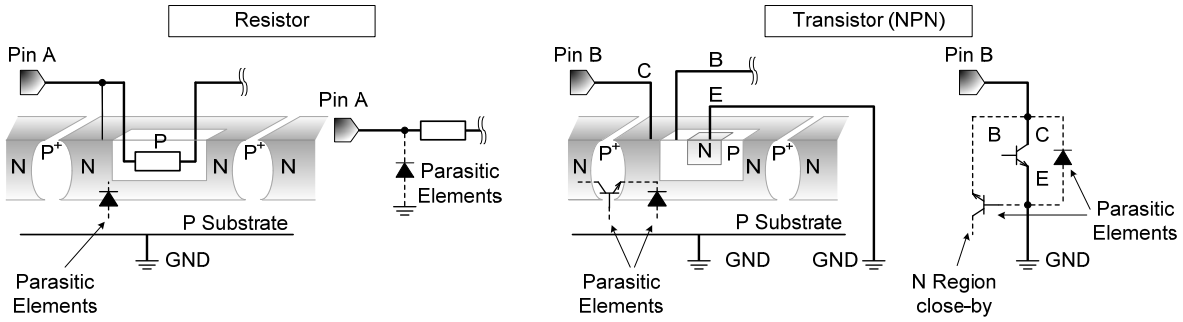
Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



12. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Thermal Shutdown Circuit (TSD)

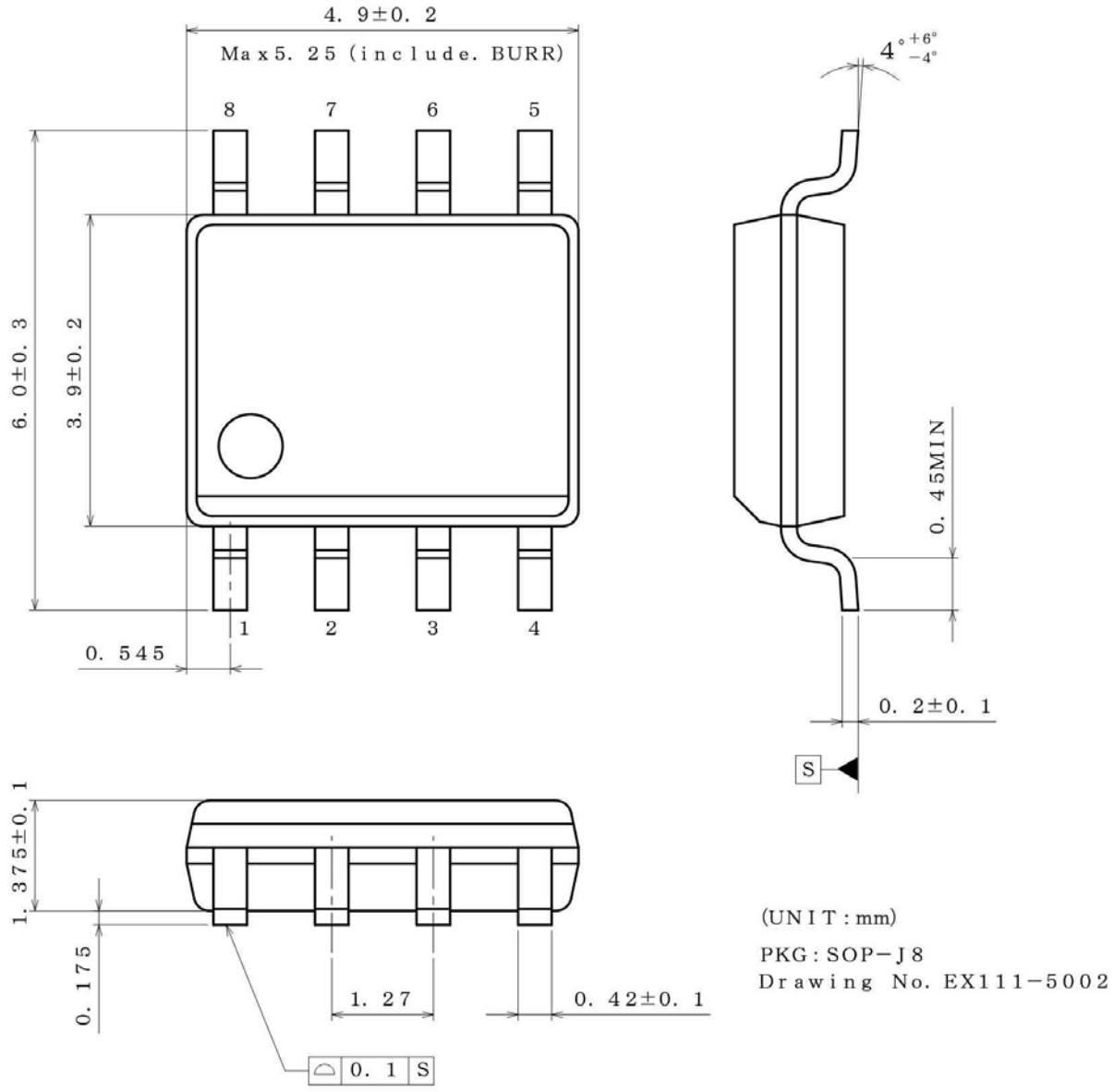
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

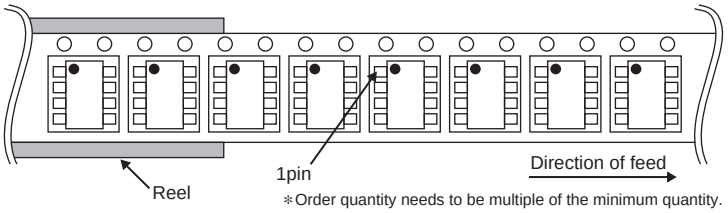
Physical Dimension, Tape and Reel Information

Package Name	SOP-J8



<Tape and Reel information>

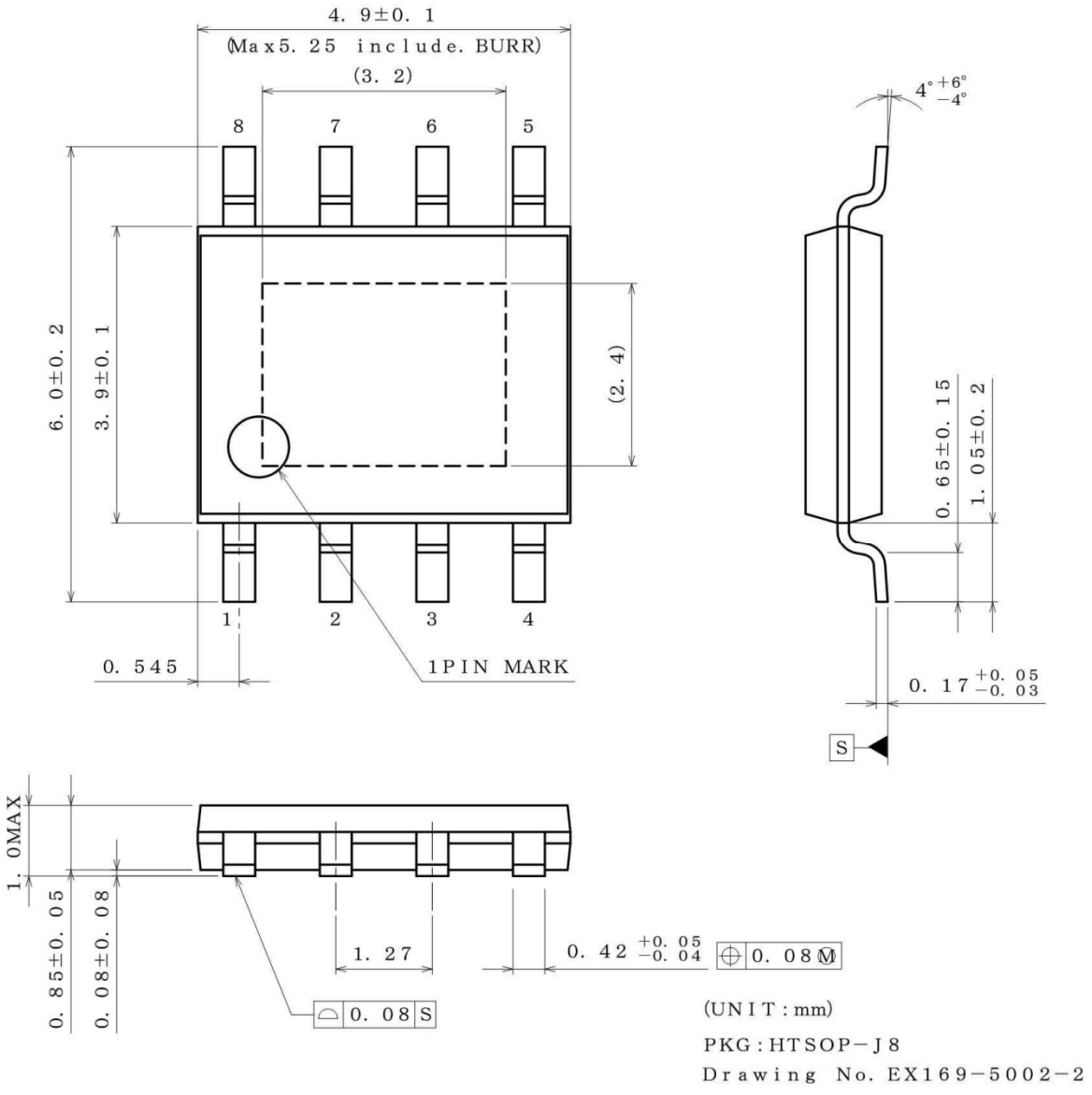
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



＊Order quantity needs to be multiple of the minimum quantity.

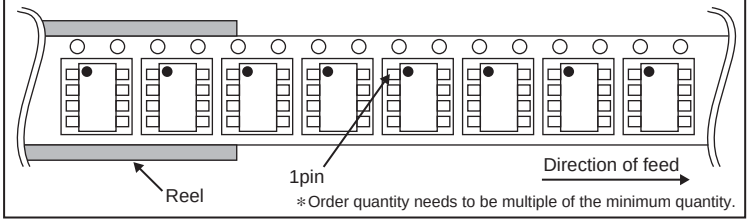
Physical Dimension, Tape and Reel Information -Continued

Package Name	HTSOP-J8



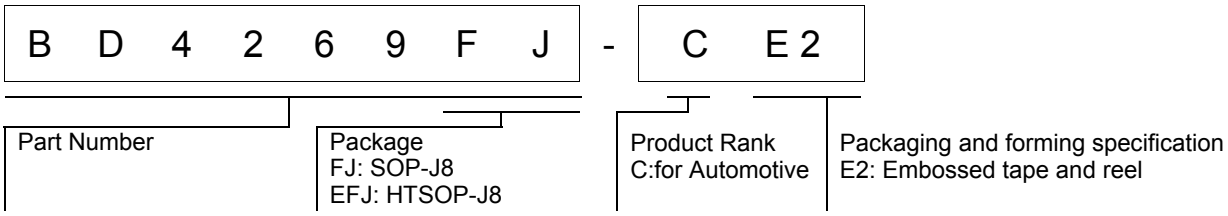
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

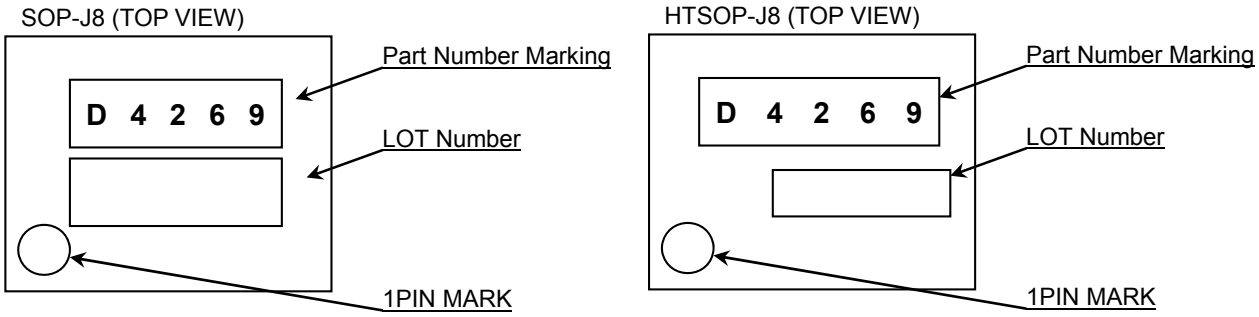


∗Order quantity needs to be multiple of the minimum quantity.

Ordering Information



Marking Diagram



Revision History

Date	Revision	Changes
31.Jul.2014	001	New Release
27.Feb.2015	002	BD4269EFJ-C was added. P1 Revised expression on the tittle P1 AEC-Q100 grade was added. P4, P5, P15, P16 and P17 Revised expression on the information of Thermal Characteristics of SOP-J8. P14 Revised expression on the information of VCC pin and Output pin capacitors. P19 Added description on Reverse Polarity Diode. P20 Revised expression on the information of Thermal Consideration.
20.Mar.2015	003	P5 A writing error of paragraph of Thermal Characteristics was corrected. P15 A writing error of paragraph of Power Dissipation was corrected.
5.Jun.2015	004	P1 The Figure of “Not Using SI and RADJ” was corrected. P16 Description of Thermal Design was corrected.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

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2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

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General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

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