19-4644; Rev 1; 8/10

EVALUATION KIT AVAILABLE

Internal-Switch Boost Regulator with Integrated Scan Driver, VCOM Calibrator, and Op Amp for TFT LCDs

General Description

The MAX17100 includes a high-voltage step-up regulator, three high-performance operational amplifiers, two linear regulators, two high-voltage switch control blocks for gate-driver supply modulation, a digital VCOM calibrator, and six independent scan drivers.

The DC-DC converter is a 1.2MHz current-mode step-up regulator with a built-in power MOSFET and provides the regulated supply voltage for the panel source driver ICs. The built-in power MOSFET allows output voltages to be as high as 18V from inputs of 2.5V to 6V. A built-in 7-bit digital soft-start function limits inrush currents during startup. The step-up regulator provides fast transient response to pulsed loads while producing efficiencies over 87%.

Three operational amplifiers, typically used as the gamma correction divider string, are configured as unity-gain buffers and feature high output short-circuit current (200mA), fast slew rate (45V/µs), and wide bandwidth (20MHz). Their rail-to-rail inputs and outputs maximize application flexibility.

Two linear regulators provide regulated gate-on and gate-off supplies for TFT panel. The two high-voltage switch control blocks modulate the shape of the gate-on supply with adjustable startup delay.

One operational amplifier is designed to drive the LCD backplane (VCOM). It features high short-circuit current of 200mA. The programmable VCOM calibrator adjusts the VCOM output-voltage level through serial interface by sinking a programmable current from the VCOM resistor-divider. The calibrator includes nonvolatile memory cells that store the desired VCOM voltage level.

The six independent high-voltage level-shifting scan drivers are designed to drive the TFT panel gate lines. The outputs swing from +35V (maximum) to -15V (minimum) and can swiftly drive capacitive loads.

The MAX17100 is available in a lead-free, 48-pin, thin QFN package with 0.4mm lead spacing. The package is a 6mm x 6mm square with a maximum thickness of 0.8mm for ultra-thin LCD panel design.

Applications

LCD Monitors

LCD TVs

Features

- **2.5V to 6V Input Supply Range**
- **1.2MHz Current-Mode Step-Up Converter**
  - **Fast Transient Response to Pulsed Load**
  - **High-Accuracy Output Voltage (1%)**
  - **Built-In 20V, 3A, 0.16Ω n-Channel Power MOSFET**
  - **Cycle-by-Cycle Current Limit**
  - **High Efficiency (87%)**
- **Three High-Performance Operational Amplifiers**
  - **200mA Output Short-Circuit Current**
  - **45V/µs Slew Rate**
  - **20MHz, -3dB Bandwidth**
  - **Rail-to-Rail Inputs and Outputs**
- **Linear Regulator for Gate-On and Gate-Off Supply**
- **Two Logic-Controlled High-Voltage Switches with Adjustable Delay**
- **Programmable VCOM Calibrator**
  - **7-Bit Adjustable Current-Sink Output**
  - **Serial Interface**
  - **Nonvolatile Setting Memory**
- **Six Independent Level-Shifting Scan Drivers**
- **Built-In Sequencing**
- **Soft-Start and Timer-Delayed Fault Latch for All Regulator Outputs**
- **Thermal-Overload Protection**
- **Gate Driver for External Input-Side Series MOSFET**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17100ETM+	-40°C to +85°C	48 Thin QFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Pin Configuration and Minimal Operating Circuit appear at end of data sheet.

Internal-Switch Boost Regulator with Integrated Scan Driver, VCOM Calibrator, and Op Amp for TFT LCDs

ABSOLUTE MAXIMUM RATINGS

IN, YV1C_, GATE to AGND .....-0.3V to +7.5V
SCL, SDA, $\overline{WR}$, $\overline{RST}$, RSET, ST_, CK_, CKB_ to AGND .....-0.3V to +7.5V
TGS, REF, COMP, FB, FBN, FBP, to AGND .....-0.3V to (V_{IN} + 0.3V)
PGND, OGND to AGND .....-0.3V to +0.3V
LX to PGND .....-0.3V to +20V
SUP to OGND .....-0.3V to +20V
DRVN to AGND .....(V_{IN} - 30V) to (V_{IN} + 0.3V)
DRVP to AGND .....-0.3V to +40V
GHON to AGND .....-0.3V to +40V
GOFF to AGND .....-20V to +0.3V
GHON to GOFF .....-0.3V to +50V
GHD_ to AGND .....-0.3V to (V_{GHON} + 0.3V)
STH_, CKH_, CKBH_ .....(-0.3V + V_{GOFF}) to (V_{GHON} + 0.3V)
POS_, OUT_, COMFB, COMADJ, VCOM to OGND .....-0.3V to (V_{SUP} + 0.3V)
COMADJ to COMFB .....-6V to +6V
OUT_ Maximum Continuous Output Current .....±75mA
GHON, GOFF RMS Current Rating 130mA
LX, PGND RMS Current Rating 2.4A
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFN (derate 27mW/°C above +70°C) 2150mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3V, Circuit of Figure 2, V_{MAIN} = V_{SUP} = +14V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input Supply Range	(Note 1)	2.5		6	V
IN Undervoltage Lockout Threshold	V_{IN} rising, hysteresis = 140mV	2.05	2.25	2.45	V
IN Quiescent Current	V_{FB} = V_{FBP} = 1.3V, V_{FBN} = 0V, LX not switching		1	3	mA
	V_{FB} = 1.2V, V_{FBP} = 1.4V, V_{FBN} = 0V, LX switching		3	5	
Duration to Trigger Fault Condition	FB or FBP below threshold or FBN above threshold; V_{FB} = 1.14V, V_{FBP} = 1V, V_{FBN} = 420mV		218		ms
Thermal Shutdown	Temperature rising		160		°C
	Hysteresis		15		
REFERENCE					
REF Output Voltage	No external load	1.238	1.250	1.262	V
REF Load Regulation	0V < I_{LOAD} < 50µA			10	mV
REF Undervoltage Lockout Threshold	Rising edge, hysteresis = 120mV		1.0	1.15	V
STEP-UP REGULATOR					
Output-Voltage Range		V_S		18	V
Frequency		1000	1200	1400	kHz
Oscillator Maximum Duty Cycle		90	91.5	93	%
FB Regulation Voltage	No load, T_A = 0°C to +85°C	1.221	1.233	1.245	V
FB Fault Trip Level	Falling edge	1.10	1.14	1.17	V
FB Load Regulation	0V < I_{LOAD} < 500mA, transient only		-0.2		%
FB Line Regulation	V_{IN} = 2.5V to 6V		0.1	0.4	%/V
FB Input Bias Current	V_{FB} = 1.233V, T_A = +25°C		100	200	nA
FB Transconductance	ΔI = ±2.5µA, FB = COMP	80	190	300	µS
FB Voltage Gain	FB to COMP		2500		V/V
LX Current Limit	V_{FB} = 1.2V, duty cycle = 75%	2.5	3	3.5	A

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 2, V_{MAIN} = V_{SUP} = +14V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LX On-Resistance	I_{LX} = 200mA		0.12	0.25	Ω
LX Bias Current	V_{LX} = 19V, T_A = +25°C		10	20	µA
Current-Sense Transresistance		0.10	0.20	0.30	V/A
GATE-ON LINEAR REGULATOR CONTROLLER					
FBP Fault Trip Level	V_{FBP} falling	0.96	1.00	1.04	V
FBP Regulation Voltage	I_{DRVP} = 100µA	1.231	1.250	1.269	V
FBP Line Regulation Error	V_{IN} = 2.5V to 6V, I_{DRVP} = 100µA	-10		+10	mV
FBP Input Bias Current	V_{FBP} = 1.25V, T_A = +25°C	-50		+50	nA
FBP Effective Load Regulation Error (Transconductance)	V_{DRVP} = 10V, I_{DRVP} = 50µA to 1mA		-1	-1.5	%
DRVP Sink Current	V_{FBP} = 1.1V, V_{DRVP} = 10V	1	5		mA
DRVP Off-Leakage Current	V_{FBP} = 1.4V, V_{DRVP} = 34V, T_A = +25°C		0.01	10	µA
Soft-Start Period			14		ms
Soft-Start Step Size			V_{REF}/ 128		V
GATE-OFF LINEAR REGULATOR CONTROLLER					
FBN Fault Trip Level	V_{FBN} rising	370	420	470	mV
FBN Regulation Voltage	I_{DRVN} = 100µA, V_{REF} - V_{FBN}	0.985	1	1.015	V
FBN Line Regulation Error	V_{IN} = 2.5V to 6V, I_{DRVN} = 100µA	-5		+5	mV
FBN Input Bias Current	V_{FBN} = 0.25V, T_A = +25°C	-50		+50	nA
FBN Effective Load Regulation Error (Transconductance)	V_{DRVN} = -10V, I_{DRVN} = 50µA to 1mA		11	25	mV
DRVN Source Current	V_{FBN} = 300mV, V_{DRVN} = -10V	1	5		mA
DRVN Off-Leakage Current	V_{FBN} = 0V, V_{DRVN} = -25V, T_A = +25°C		0.01	10	µA
Soft-Start Period			14		ms
Soft-Start Step Size			(V_{REF} - V_{FBN}) /128		V
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES					
TGS Capacitor Charge Current	During startup, V_{TGS} = 1V	4	5	6	µA
TGS Turn-On Threshold		1.19	1.25	1.31	V
TGS Discharge Switch On-Resistance	During UVLO, V_{IN} = 2V		14		Ω
YV1C_ Input Low Voltage				0.6	V
YV1C_ Input High Voltage	V_{IN} < 4.5V	1.75			V
	V_{IN} > 4.5V	2.1			
YV1C_ Input Leakage Current	YV1C_ = AGND or IN, T_A = +25°C	-1		+1	µA
YV1C_-to-GHON Propagation Delay	Rising		100		ns
	Falling		300		
GHON Input-Voltage Range				35	V

Internal-Switch Boost Regulator with Integrated Scan Driver, VCOM Calibrator, and Op Amp for TFT LCDs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 2, V_{MAIN} = V_{SUP} = +14V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GHON Input Current	YV1C_ is high, CK_, CKB_, ST_ are low, (V_{GHON} = 32.5V, V_{GOFF} = -12.5V)		820	1550	µA
GHON to GHC_ Switch On-Resistance	V_{TGS} = 1.5V, YV1C_ = IN		6	12	Ω
GHD_ to GHC_ Switch On-Resistance	V_{TGS} = 1.5V, YV1C_ = AGND		30	60	Ω
INPUT SERIES SWITCH CONTROL					
GATE Output Sink Current	GATE = IN	45	50	55	µA
GATE Done Voltage Threshold	V_{IN} - V_{GATE}		1.5	2.2	V
GATE-On Voltage	V_{IN} = 5V			0.5	V
BUFFER AMPLIFIERS					
SUP Supply Range		6		18	V
SUP Overvoltage Fault Threshold		18.1	19.0	19.9	V
SUP Supply Current	All op amps are no load with V_{POS} = V_{SUP}/2		13	16	mA
Input Offset Voltage	$V_{POS\_}$ = V_{SUP}/2, T_A = +25°C	-8	+4	+16	mV
Input Bias Current	$V_{POS\_}$ = V_{SUP}/2, T_A = +25°C	-50		+50	nA
Input Common-Mode Voltage Range		0		V_{SUP}	V
Output-Voltage Swing High	$I_{OUT\_}$ = 5mA	V_{SUP} - 100			mV
Output-Voltage Swing Low	$I_{OUT\_}$ = -5mA			100	mV
Slew Rate			100		V/µs
-3dB Bandwidth	R_L = 10kΩ, C_L = 10pF, buffer configuration		20		MHz
Short-Circuit Current	Source: $V_{POS\_}$ = V_{SUP} - 3V, $V_{OUT\_}$ = V_{SUP} - 4V	115	200		mA
	Sink: $V_{POS\_}$ = 3V, $V_{OUT\_}$ = 4V	115	200		
Power-Supply Rejection Ratio (Note 4)	DC, 10V ≤ V_{SUP} ≤ 18V, $V_{POS\_}$ = 7V		100		dB
VCOM OPERATIONAL AMPLIFIER					
Input Bias Current	V_{COMFB} = V_{COMADJ} = V_{SUP}/2, T_A = +25°C	-50		+50	nA
SUP Supply Current	Buffer configuration, V_{COMADJ} = V_{SUP}/2, no load		3	4	mA
Input Offset Voltage		-8	+4	+16	mV
Output-Voltage Swing High	I_{VCOM} = 75mA	V_{SUP} - 1.5	V_{SUP} - 0.6		V
Output-Voltage Swing Low	I_{VCOM} = -75mA		0.4	1.5	V
Slew Rate			100		V/µs
-3dB Bandwidth	R_L = 10kΩ, C_L = 10pF, buffer configuration		20		MHz
Short-Circuit Current	Buffer configuration, Source: V_{COMADJ} = V_{SUP} - 3V, V_{VCOM} = V_{SUP} - 4V	115	200		mA
	Buffer configuration, Sink: V_{COMADJ} = 3V, V_{VCOM} = 4V				

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 2, V_{MAIN} = V_{SUP} = +14V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PROGRAMMABLE VCOM CALIBRATOR					
SUP Input Range	For MEMORY writing	8		18	V
RSET Voltage Resolution		7			Bits
RSET Differential Nonlinearity	Monotonic overtemperature	-1		+1	LSB
RSET Zero-Scale Error		-1	+1	+2	LSB
RSET Full-Scale Error		-4		+4	LSB
RSET Current	V_{COMADJ} = 4V, VCOM DAC code = 7FH			120	µA
RSET External Resistance (Note 2)	To AGND, V_{SUP} = 18V	8.5		170	kΩ
	To AGND, V_{SUP} = 6V	3.3		50	
V_{RSET}/V_{SUP} Voltage Ratio	DAC full scale		0.05		V/V
COMADJ Settling Time	To ±0.5 LSB error band		20		µs
Memory Write Cycles		30			Cycles
$\overline{WR}$ Input Low Voltage				1	V
$\overline{WR}$ Input High Voltage		2			V
$\overline{WR}$ Leakage Current	$\overline{WR}$ = AGND or IN, T_A = +25°C	-1		+1	µA
MTP Write Time		160	218	250	ms
SERIAL INTERFACE					
Logic-Input Low Voltage	SDA, SCL			0.3 x V_{IN}	V
Logic-Input High Voltage	SDA, SCL	0.7 x V_{IN}			V
Logic-Output Low Sink Current (SDA)	SDA sink 3mA	0		0.4	V
Logic-Input Current	SDA, SCL, T_A = +25°C	-1		+1	µA
SDA and SCL Input Capacitance	SDA, SCL		5		pF
SCL Frequency (f_{CLK})		DC		400	kHz
SCL High Time (t_{CLH})		600			ns
SCL Low Time (t_{CLL})		1300			ns
SDA and SCL Rise Time (t_R)	C_b = total capacitance of bus line in pF	20 + 0.1 x Cb		300	ns
SDA and SCL Fall Time (t_F)	C_b = total capacitance of bus line in pF	20 + 0.1 x Cb		300	ns
START Condition Hold Time (t_{HDSTT})	10% of SDA to 90% of SCL	600			ns
START Condition Setup Time (t_{SUSTT})		600			ns
Data Input Hold Time (t_{HDDAT})		200		900	ns
Data Input Setup Time (t_{SUDAT})		100			ns
STOP Condition Setup Time (t_{SUST})		600			ns
Bus Free Time (t_{BF})		1300			ns
Input Filter Spike Suppression	SDA, SCL, not tested			50	ns

Internal-Switch Boost Regulator with Integrated Scan Driver, VCOM Calibrator, and Op Amp for TFT LCDs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 2, V_{MAIN} = V_{SUP} = +14V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RESET FUNCTION					
$\overline{RST}$ Delay Threshold Voltage	V_{REF} = 1.25V	1.225	1.250	1.275	V
$\overline{RST}$ Sink Current	$V_{\overline{RST}}$ = 0.4V	10	40		mA
LEVEL SHIFTERS					
GHON to GOFF Voltage Range	V_{GHON} - V_{GOFF}			45	V
GHON Input-Voltage Range				35	V
GOFF Input-Voltage Range		-15			V
GHON Supply Current	YV1C_ is low, CK_, CKB_, ST_ are low, (V_{GHON} = 32.5V, V_{GOFF} = -12.5V)		450	830	µA
GOFF Supply Current	YV1C_ is high, CK_, CKB_, ST_ are low, (V_{GHON} = 32.5V, V_{GOFF} = -12.5V)		150	310	µA
	YV1C_ is high, CK_, CKB_, ST_ are high, (V_{GHON} = 32.5V, V_{GOFF} = -12.5V)		60	150	
ST_,CK_,CKB_ Input Current	T_A = +25°C	-1		+1	µA
CKH_,CKBH_,STH_ Output-Voltage Low	I_{OUT} = 10mA		V_{GOFF} + 0.3	V_{GOFF} + 1.0	V
CKH_,CKBH_,STH_ Output-Voltage High	I_{OUT} = 10mA	V_{GHON} - 1.0	V_{GHON} - 0.3		V
ST_,CK_,CKB_ Input High Level	V_{IN} < 4.5V	1.6			V
	V_{IN} > 4.5V	2.0			
ST_,CK_,CKB_ Input Low Level				0.6	V
CKH_,CKBH_,STH_ Rise Time (Note 4)	C_L = 5nF, R_L = 50Ω		0.5		µs
CKH_,CKBH_,STH_ Fall Time (Note 4)	C_L = 5nF, R_L = 50Ω		0.5		µs
CKH_,CKBH_ and STH_ Propagation Delay (Note 4)	C_L = 5nF, R_L = 50Ω rising edge, falling edge		60		ns

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3V, Circuit of Figure 2, V_{MAIN} = V_{SUP} = +14V, **T_A = -40°C to +85°C**, unless otherwise noted.)(Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input Supply Range	(Note 1)	2.5		6	V
IN Undervoltage Lockout Threshold	V_{IN} rising, hysteresis = 140mV	2.05		2.45	V
IN Quiescent Current	V_{FB} = V_{FBP} = 1.3V, V_{FBN} = 0V, LX not switching			3	mA
	V_{FB} = 1.2V, V_{FBP} = 1.4V, V_{FBN} = 0V, LX switching			5	
REFERENCE					
REF Output Voltage	No external load	1.238		1.262	V
REF Load Regulation	0V < I_{LOAD} < 50µA			10	mV
REF Undervoltage Lockout Threshold	Rising edge, hysteresis = 120mV		1.0	1.15	V
STEP-UP REGULATOR					
Output-Voltage Range		V_S		18	V
Frequency		1000		1400	kHz
Oscillator Maximum Duty Cycle		90		94	%
FB Regulation Voltage	No load	1.221		1.245	V
FB Line Regulation	V_{IN} = 2.5V to 6V			0.4	%/V
FB Transconductance	I = ±2.5µA, FB = COMP	75		280	µS
LX Current Limit	V_{FB} = 1.2V, duty cycle = 75%	-10		+10	mV
FBP Effective Load Regulation Error (Transconductance)	V_{DRVP} = 10V, I_{DRVP} = 50µA to 1mA			-1.5	%
DRVP Sink Current	V_{FBP} = 1.1V, V_{DRVP} = 10V	1			mA
GATE-OFF LINEAR REGULATOR CONTROLLER					
FBN Regulation Voltage	I_{DRVN} = 100µA, V_{REF} - V_{FBN}	0.985		1.015	V
FBN Line Regulation Error	V_{IN} = 2.5V to 6V, I_{DRVN} = 100µA	-5		+5	mV
FBN Effective Load Regulation Error (Transconductance)	V_{DRVN} = -10V, I_{DRVN} = 50µA to 1mA			25	mV
DRVN Source Current	V_{FBN} = 300mV, V_{DRVN} = -10V	1			mA
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES					
TGS Capacitor Charge Current	During startup, V_{TGS} = 1V	4		6	µA
TGS Turn-On Threshold		1.19		1.31	V
YV1C_ Input Low Voltage				0.6	V
YV1C_ Input High Voltage	V_{IN} < 4.5V	1.75			V
	V_{IN} > 4.5V	2.1			
GHON Input-Voltage Range				35	V

Internal-Switch Boost Regulator with Integrated Scan Driver, VCOM Calibrator, and Op Amp for TFT LCDs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 2, V_{MAIN} = V_{SUP} = +14V, **T_A = -40°C to +85°C**, unless otherwise noted.)(Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GHON Input Current	YV1C_ is high, CK_, CKB_, ST_ are low, (V_{GHON} = 32.5V, V_{GOFF} = -12.5V)			1550	µA
	YV1C_ is high, CK_, CKB_, ST_ are high, (V_{GHON} = 32.5V, V_{GOFF} = -12.5V)				
GHON to GHC_ Switch On-Resistance	V_{TGS} = 1.5V, YV1C_ = IN			12	Ω
GHD_ to GHC_ Switch On-Resistance	V_{TGS} = 1.5V, YV1C_ = AGND			60	Ω
INPUT SERIES SWITCH CONTROL					
GATE Output Sink Current	GATE = IN	44		55	µA
GATE Done Voltage Threshold	V_{IN} - V_{GATE}			2.3	V
GATE-On Voltage	V_{IN} = 5V			0.61	V
BUFFER AMPLIFIERS					
SUP Supply Range		6		18	V
SUP Overvoltage Fault Threshold		18.1		19.9	V
SUP Supply Current	All op amps are no load with V_{POS} = V_{SUP}/2			16	mA
Input Offset Voltage	$V_{POS\_}$ = V_{SUP}/2, T_A = +25°C			16	mV
Input Common-Mode Voltage Range		0		V_{SUP}	V
Output-Voltage Swing High	$I_{OUT\_}$ = 5mA	V_{SUP} - 100			mV
Output-Voltage Swing Low	$I_{OUT\_}$ = -5mA			100	mV
Short-Circuit Current	Source: $V_{POS\_}$ = V_{SUP} - 3V, V_{OUT} = V_{SUP} - 4V	115			mA
	Sink: $V_{POS\_}$ = 3V, $V_{OUT\_}$ = 4V	115			
VCOM OPERATIONAL AMPLIFIER					
SUP Supply Current	Buffer configuration, V_{COMADJ} = V_{SUP}/2, no load			4	mA
Output-Voltage Swing High	I_{VCOM} = 75mA	V_{SUP} - 1.5			V
Output-Voltage Swing Low	I_{VCOM} = 75mA		0.4	1.5	V
Short-Circuit Current	Buffer configuration, source: V_{COMADJ} = V_{SUP} - 3V, V_{VCOM} = V_{SUP} - 4V	115			mA
	Buffer configuration, sink: V_{COMADJ} = 3V, V_{VCOM} = 4V				

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 2, V_{MAIN} = V_{SUP} = +14V, **T_A = -40°C to +85°C**, unless otherwise noted.)(Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PROGRAMMABLE VCOM CALIBRATOR					
SUP Input Range	For MEMORY writing	8		18	V
RSET Voltage Resolution		7			Bits
RSET Differential Nonlinearity	Monotonic overtemperature	-1		+1	LSB
RSET Zero-Scale Error		-1		+2	LSB
RSET Full-Scale Error		-4		+4	LSB
RSET Current	V_{COMADJ} = 4V, VCOM DAC code = 7FH			120	µA
RSET External Resistance (Note 2)	To AGND, V_{SUP} = 18V	8.5		170	kΩ
	To AGND, V_{SUP} = 6V	3.3		50	
Memory Write Cycles		30			Cycles
MTP Write Time		160		250	ms
$\overline{WR}$ Input Low Voltage				1	V
$\overline{WR}$ Input High Voltage		2			V
SERIAL INTERFACE					
Logic-Input Low Voltage	SDA, SCL			0.3 x V_{IN}	V
Logic-Input High Voltage	SDA, SCL	0.7 x V_{IN}			V
Logic-Output Low Sink Current (SDA)	SDA sink 3mA	0		0.4	V
SCL Frequency (f_{CLK})		DC		400	kHz
SCL High Time (t_{CLH})		600			ns
SCL Low Time (t_{CLL})		1300			ns
SDA and SCL Rise Time (t_R)	Cb = total capacitance of bus line in pF	20 + 0.1 x Cb		300	ns
SDA and SCL Fall Time (t_F)	Cb = total capacitance of bus line in pF	20 + 0.1 x Cb		300	ns
START Condition Hold Time (t_{HDSTT})	10% of SDA to 90% of SCL	600			ns
START Condition Setup Time (t_{SUSTT})		600			ns
Data Input Hold Time (t_{HDDAT})		200		900	ns
Data Input Setup Time (t_{SUDAT})		100			ns
STOP Condition Setup Time (t_{SUST})		600			ns
Bus Free Time (t_{BF})		1300			ns
Input Filter Spike Suppression	SDA, SCL, not tested			50	ns
RESET FUNCTION					
$\overline{RST}$ Delay Threshold Voltage	V_{REF} = 1.25V	1.21		1.28	V
$\overline{RST}$ Sink Current	$V_{\overline{RST}}$ = 0.4V	10			mA
LEVEL SHIFTERS					
GHON to GOFF Voltage Range	V_{GHON} - V_{GOFF}			45	V
GHON Input-Voltage Range				35	V
GOFF Input-Voltage Range		-15			V

Internal-Switch Boost Regulator with Integrated Scan Driver, VCOM Calibrator, and Op Amp for TFT LCDs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 2, V_{MAIN} = V_{SUP} = +14V, **T_A = -40°C to +85°C**, unless otherwise noted.)(Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GHON Supply Current	YV1C_ is low, CK_, CKB_, ST_ are low, (V_{GHON} = 32.5V, V_{GOFF} = -12.5V)			830	µA
GOFF Supply Current	YV1C_ is high, CK_, CKB_, ST_ are low, (V_{GHON} = 32.5V, V_{GOFF} = -12.5V)			310	µA
	YV1C_ is high, CK_, CKB_, ST_ are high, (V_{GHON} = 32.5V, V_{GOFF} = -12.5V)			150	
CKH_, CKBH_, STH_ Output-Voltage Low	$I_{OUT\_}$ = 10mA			V_{GOFF} + 1	V
CKH_, CKBH_, STH_ Output-Voltage High	$I_{OUT\_}$ = 10mA	V_{GHON} - 1			V
ST_, CK_, CKB_ Input High Level	V_{IN} < 4.5V	1.6			V
	V_{IN} > 4.5V	2.0			
ST_, CK_, CKB_ Input Low Level				0.6	V

Note 1: For 5.5V < V_{IN} < 6.0V, use IC for no longer than 1% of IC lifetime. For continuous operation, input voltage should not exceed 5.5V.

Note 2: RSET external resistor range is verified at DAC full scale.

Note 3: Specifications to T_A = -40°C are guaranteed by design, not production tested.

Note 4: Guaranteed by design. Not production tested.

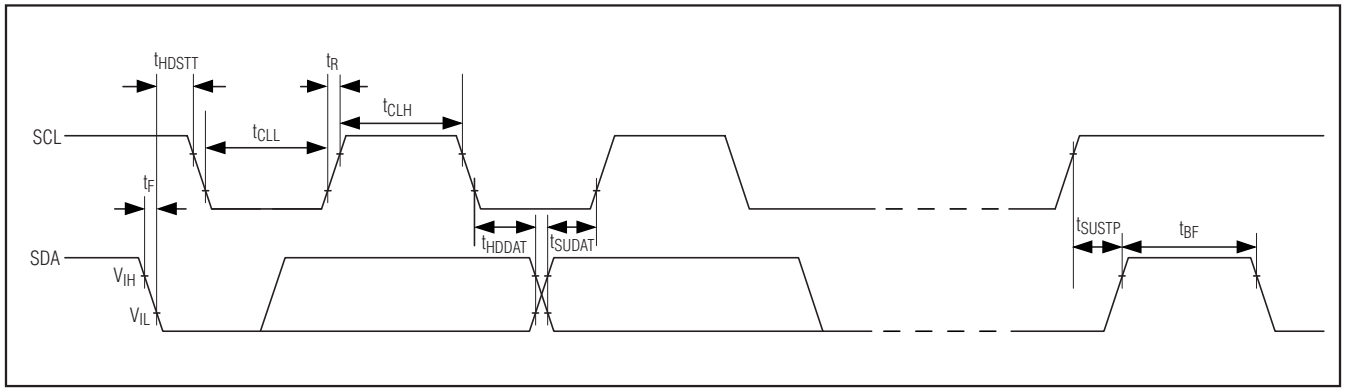
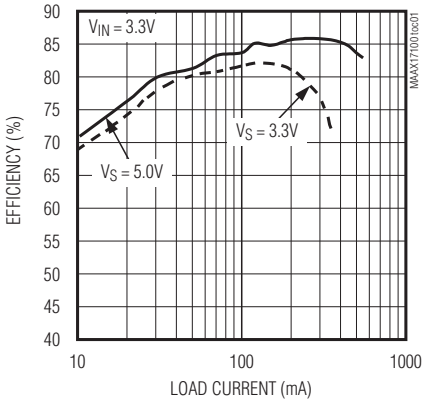


Figure 1. Timing Definitions Used in the Electrical Characteristics

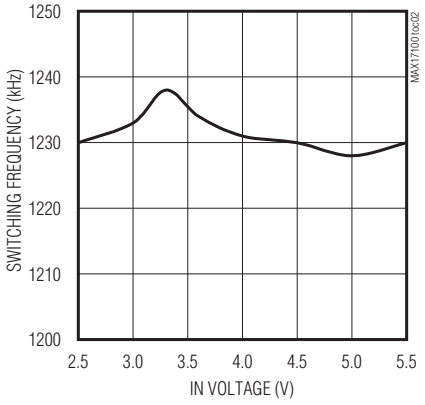
Typical Operating Characteristics

(Circuit of Figure 2, V_S = 5V, V_{MAIN} = 14V, V_{GHON} = 25V, V_{GOFF} = -10V, T_A = +25°C, unless otherwise noted.)

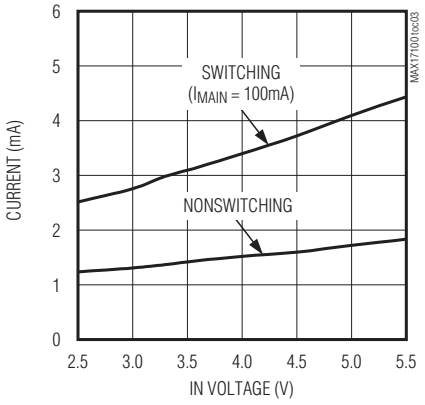
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT



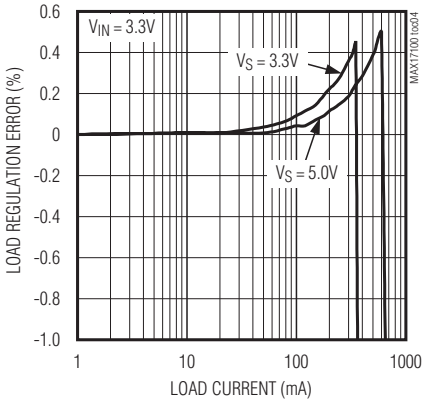
STEP-UP REGULATOR SWITCHING FREQUENCY vs. INPUT VOLTAGE



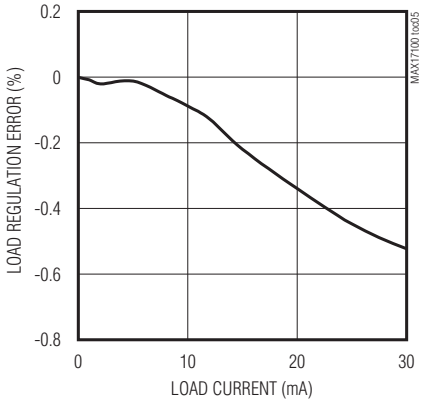
IN SUPPLY QUIESCENT CURRENT vs. IN VOLTAGE



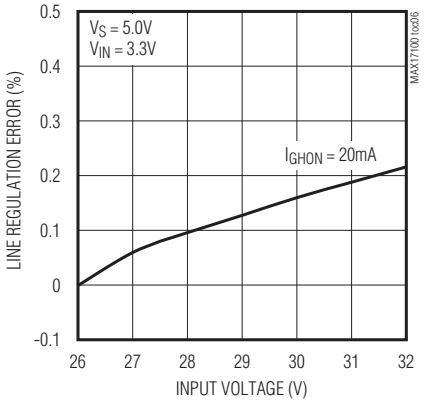
STEP-UP REGULATOR OUTPUT LOAD REGULATION vs. LOAD CURRENT



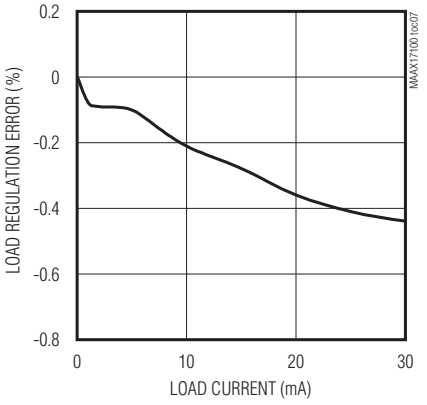
POSITIVE LINEAR REGULATOR LOAD REGULATION vs. LOAD CURRENT



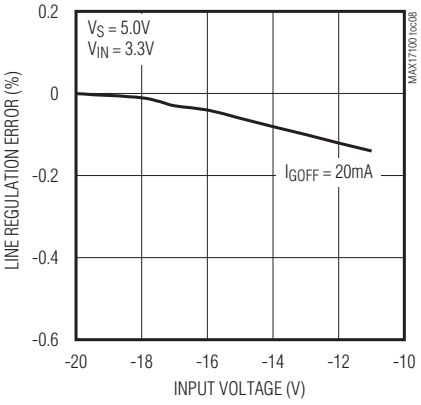
POSITIVE LINEAR REGULATOR LINE REGULATION vs. INPUT VOLTAGE



NEGATIVE LINEAR REGULATOR LOAD REGULATION vs. LOAD CURRENT



NEGATIVE LINEAR REGULATOR LINE REGULATION vs. INPUT VOLTAGE

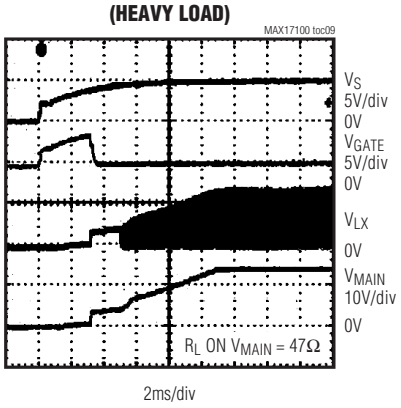


Internal-Switch Boost Regulator with Integrated Scan Driver, VCOM Calibrator, and Op Amp for TFT LCDs

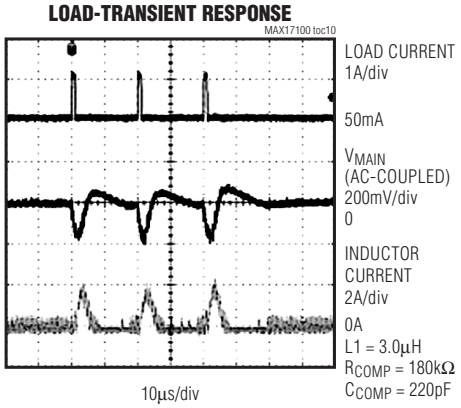
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_S = 5V, V_{MAIN} = 14V, V_{GHON} = 25V, V_{GOFF} = -10V, T_A = +25°C, unless otherwise noted.)

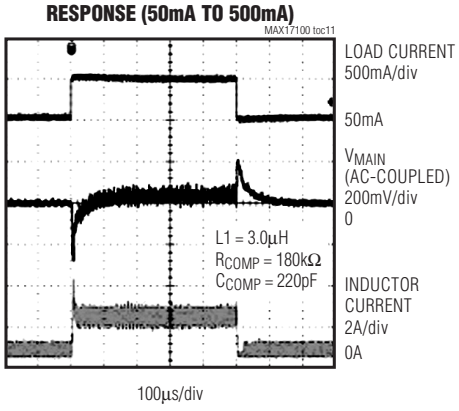
STEP-UP REGULATOR SOFT-START (HEAVY LOAD)



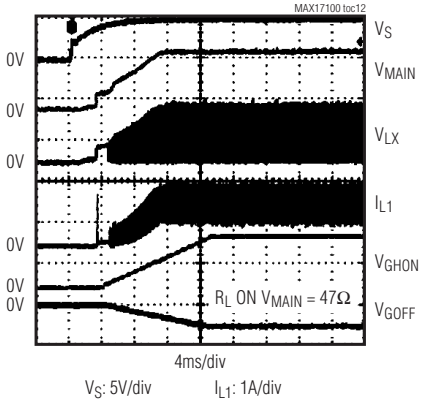
STEP-UP REGULATOR PULSED LOAD-TRANSIENT RESPONSE



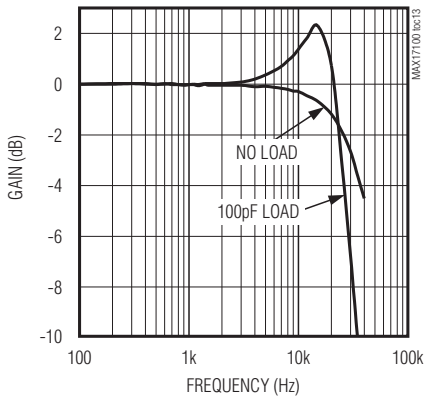
STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE (50mA TO 500mA)



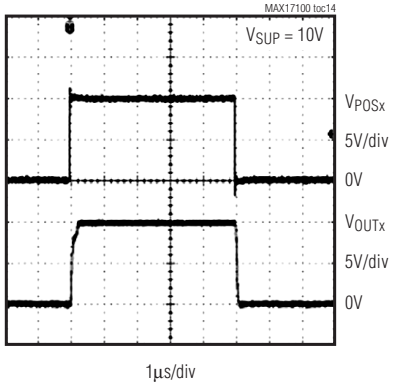
POWER-UP SEQUENCE



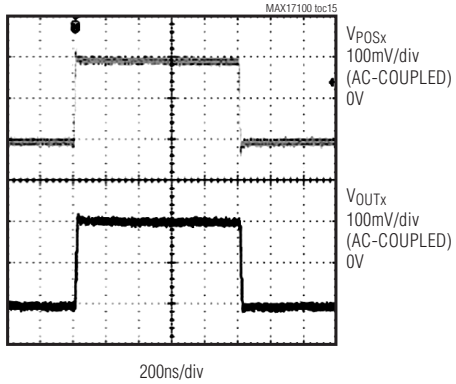
OPERATION AMPLIFIER FREQUENCY RESPONSE



OPERATIONAL AMPLIFIER LARGE-SIGNAL STEP RESPONSE



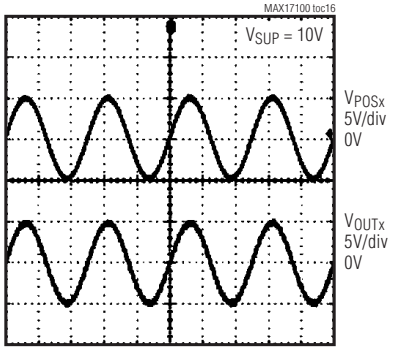
OPERATIONAL AMPLIFIER SMALL-SIGNAL STEP RESPONSE



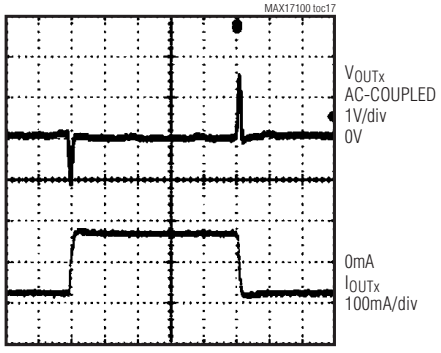
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_S = 5V, V_{MAIN} = 14V, V_{GHON} = 25V, V_{GOFF} = -10V, T_A = +25°C, unless otherwise noted.)

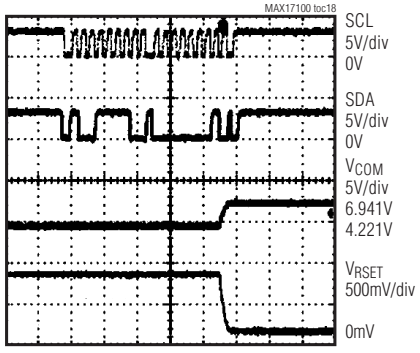
OPERATIONAL AMPLIFIER RAIL-TO-RAIL INPUT/OUTPUT



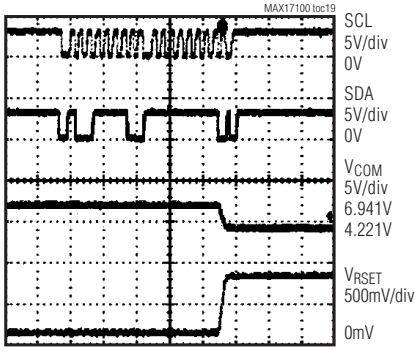
OPERATIONAL AMPLIFIER LOAD-TRANSIENT RESPONSE



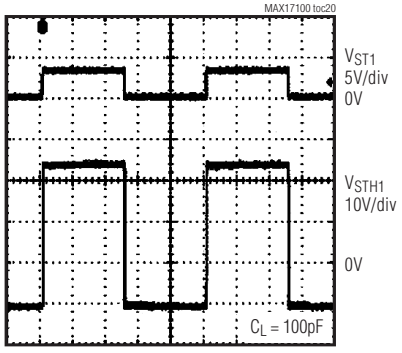
CALIBRATOR FULL-SCALE UPWARD STEP RESPONSE



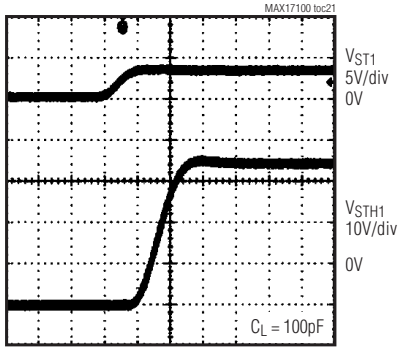
CALIBRATOR FULL-SCALE DOWNWARD STEP RESPONSE



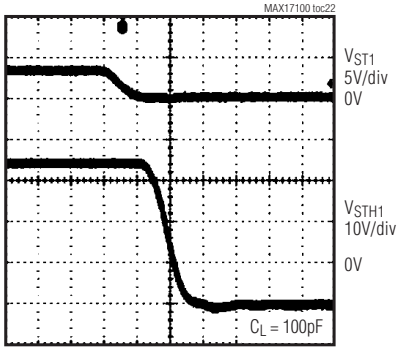
SCAN DRIVER INPUT/OUTPUT WAVEFORMS WITH LOGIC INPUT



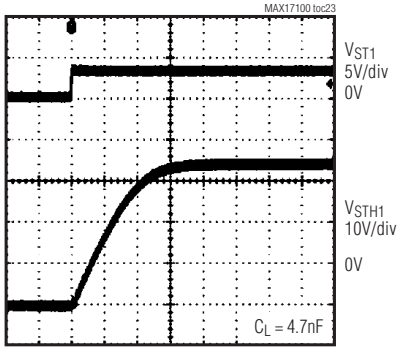
STH1 RISING EDGE PROPROPAGATION DELAY



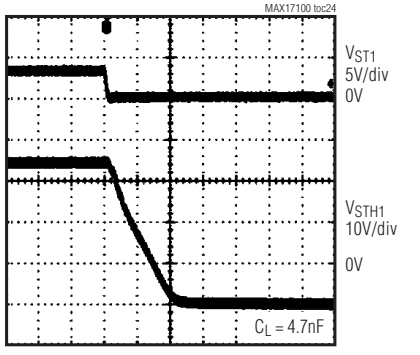
CK1 FALLING EDGE PROPAGATION DELAY



SCAN DRIVER OUTPUT RISE TIME



SCAN DRIVER OUTPUT FALL TIME



Internal-Switch Boost Regulator with Integrated Scan Driver, VCOM Calibrator, and Op Amp for TFT LCDs

Pin Description

PIN	NAME	FUNCTION
1	COMP	Step-Up Regulator Error-Amplifier Compensation Pin. Connect a series RC from COMP to AGND.
2	DRVN	Gate-Off Linear-Regulator Base-Drive Output. Open drain of an internal n-channel MOSFET. Connect DRVN to the base of an external npn pass transistor.
3	FBN	Gate-Off Linear Regulator Feedback Input. FBN regulates to 250mV (nominal). Connect FBN to the center of a resistive voltage-divider between the negative output and REF to set the gate-off linear-regulator output voltage. Place the resistive voltage-divider within 5mm of FBN.
4	REF	Reference Output. Bypass REF to AGND with a minimum 0.22µF capacitor close to the pin. All power outputs are disabled until REF exceeds its UVLO threshold.
5, 42	AGND	Analog Ground. Connect to power ground (PGND) under the IC.
6	FBP	Gate-On Linear-Regulator Feedback Input. FBP regulates to 1.25V (nominal). Connect FBP to the center of a resistive voltage-divider between the positive charge-pump regulator output and AGND to set the gate-on linear-regulator output voltage. Place the resistive voltage-divider within 5mm of FBP.
7	DRVP	Gate-On Linear-Regulator Base-Drive Output. Open drain of an internal n-channel MOSFET. Connect DRVP to the base of an external pnp pass transistor.
8	TGS	High-Voltage-Switch Delay Input. Connect a capacitor from TGS to AGND to set the high-voltage-switch startup delay.
9	GHON	High-Voltage-Switch Input. Source of the internal high-voltage p-channel MOSFET. Bypass GHON to PGND with a minimum of 0.1µF capacitor close to the pin.
10, 11	GHD_	High-Voltage-Switch Input. Drain of the internal high-voltage back-to-back p-channel MOSFETs.
12	GOFF	Gate-Off Voltage Input for Level Shifter
13	CKBH2	Level-Shifter Output
14	CKH2	Level-Shifter Output
15	STH2	Level-Shifter Output
16	CKBH1	Level-Shifter Output
17	CKH1	Level-Shifter Output
18	STH1	Level-Shifter Output
19, 26	YV1C_	High-Voltage-Switch Control Input. When YV1C_ is high, the high-voltage switch between GHON and GHC_ is on and the high-voltage switch between GHC_ and GHD_ is off. When YV1C_ is low, the switch between GHON and GHC_ is off and the switch between GHC_ and GHD_ is on. YV1C_ is inhibited by the IN undervoltage lockout and when the voltage on TGS is less than 1.25V.
20	CKB2	Level-Shifter Logic-Level Input
21	CK2	Level-Shifter Logic-Level Input
22	CKB1	Level-Shifter Logic-Level Input
23	CK1	Level-Shifter Logic-Level Input
24	ST2	Level-Shifter Logic-Level Input
25	ST1	Level-Shifter Logic-Level Input

Pin Description (continued)

PIN	NAME	FUNCTION
27, 29, 31	POS_	Operational Amplifier Noninverting Input
28, 30, 32	OUT_	Operational Amplifier Output. OUT_ is high impedance in shutdown.
33	VCOM	VCOM Buffer Operational Amplifier Output
34	COMFB	VCOM Buffer Operational Amplifier Inverting Input
35	SUP	Operational Amplifier Supply Input. Typically connected to the output of the step-up regulator (V_{MAIN}) and bypass to OGND with a 0.47µF capacitor.
36	OGND	Analog Ground for Operational Amplifiers. Connect to power ground (PGND) underneath the IC.
37	COMADJ	VCOM Buffer Operational Amplifier Noninverting Input
38	RSET	Full-Scale Sink-Current Adjustment Input. Connect a resistor, R_{RSET}, from RSET to AGND to set the full-scale adjustable sink current I_{OUT}, which is $V_{SUP}/(20 \times R_{RSET})$. I_{OUT} is equal to the current through R_{RSET}.
39	$\overline{WR}$	Serial Write-Protect Input. When $\overline{WR}$ is high, I^2C write commands to update nonvolatile memory are ignored.
40	SCL	Seria Interface Clock Input. Connect a 5.6kΩ pullup resistor to IN.
41	SDA	Seria Interface Data I/O. Output is open drain. Connect a 5.6kΩ pullup resistor to IN.
43	IN	IN Supplies the Internal Reference and Other Internal Circuitry. Connect IN to the input supply voltage and bypass IN to AGND with a minimum 1µF ceramic capacitor. It is important for the loop area between the IC and the bypass capacitor, and the trace length connecting the bypass capacitor to be minimized.
44	GATE	External p-Channel MOSFET Gate Drive. It is high to keep the switch off during fault condition, including output overload, short circuit, FB fault latch, and thermal protection. Leave the pin unconnected if the external pFET is not placed.
45	LX	Step-Up Regulator Switching Node. Connect inductor and boost diode here and minimize trace area for lowest EMI.
46	PGND	Power Ground
47	$\overline{RST}$	Reset Function Output
48	FB	Step-Up Regulator Feedback Input. FB regulates to 1.233V. Connect FB to the center of a resistive voltage-divider between the step-up regulator output and AGND to set the regulator's output voltage. Place the resistive voltage-divider within 5mm of FB.
—	EP	Exposed Pad. Connect EP to AGND.

Internal-Switch Boost Regulator with Integrated Scan Driver, VCOM Calibrator, and Op Amp for TFT LCDs

Typical Operating Circuit

The MAX17100 typical operating circuit (Figure 2) is a complete power-supply system for TFT LCDs. The circuit generates a +14V source-driver supply and +25V and -10V gate-driver supplies. The input-voltage range for the IC is from +2.5V to +6.0V. The listed load currents in Figure 2 are available from a +4.5V to +5.5V supply. Table 1 lists some recommended components and Table 2 lists the contact information of component suppliers.

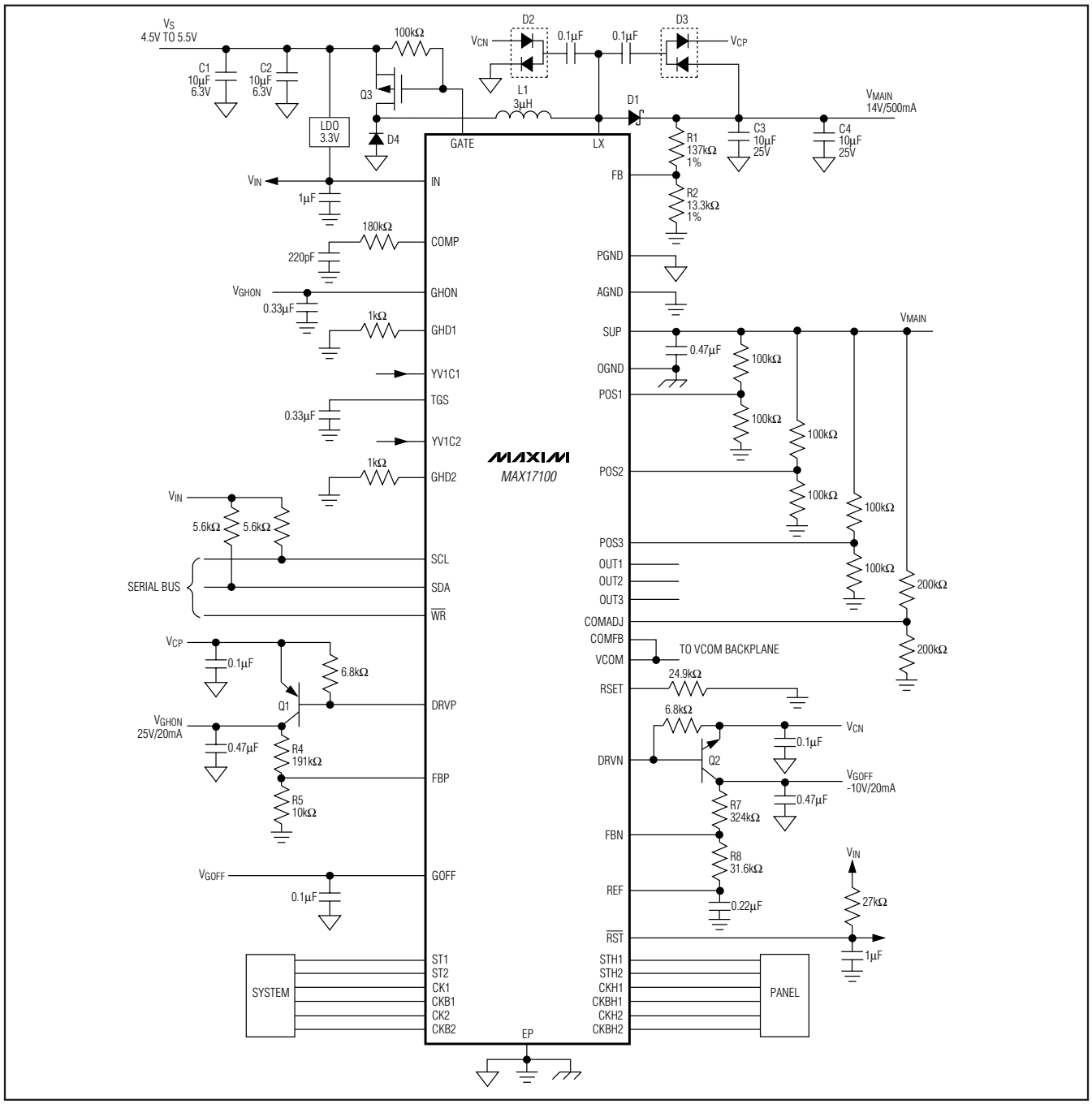


Figure 2. Typical Operating Circuit

Table 1. Component List

REFERENCE DESIGNATOR	DESCRIPTION
C1, C2	10µF, 6.3V X5R ceramic capacitors (0603), TDK C1608X5R0J106K
C3, C4	10µF, 25V X5R ceramic capacitors (1206), TDK C3216X5R1E106M
D1	3A, 30V Schottky diode (M-Flat), Toshiba CMS02
D2, D3	200mA, 100V dual diodes (SOT23), Fairchild MMBD4148SE
D4	3A, 30V diode (SMA), Vishay B350A
L1	3.0µH, 3A inductor, Sumida CDRH6D28-3R0
Q1	200mA, 40V pnp transistor (SOT23), Fairchild MMBT3906
Q2	200mA, 40V npn transistor (SOT23), Fairchild MMBT3904
Q3	-20V/63mΩ p-channel MOSFET, Vishay PowerPak SC-70 SiA443DJ

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Fairchild	408-822-2000	408-822-2102	www.fairchildsemi.com
Sumida	847-545-6700	847-545-6720	www.sumida.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Toshiba	949-455-2000	949-859-3963	www.toshiba.com/taec
Vishay	402-563-6866	402-563-6296	www.vishay.com

Detailed Description

The MAX17100 contains a high-performance step-up regulator, three high-current operational amplifiers, two linear regulators, two high-voltage-switch control blocks for gate-driver supply modulation, a digital VCOM calibrator, and six independent level-shifting scan drivers. Figure 3 shows the MAX17100 functional diagram.

Step-Up Regulator

The main step-up regulator employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast transient response to pulsed loads typical of TFT-LCD panel source drivers. The 1.2MHz switching frequency allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The integrated high-efficiency MOSFET and the IC's built-in digital soft-start functions reduce the number of external components required while controlling inrush currents. The output voltage can be set from V_{IN} to 18V with an external resistive voltage-divider. The regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

Internal-Switch Boost Regulator with Integrated Scan Driver, VCOM Calibrator, and Op Amp for TFT LCDs

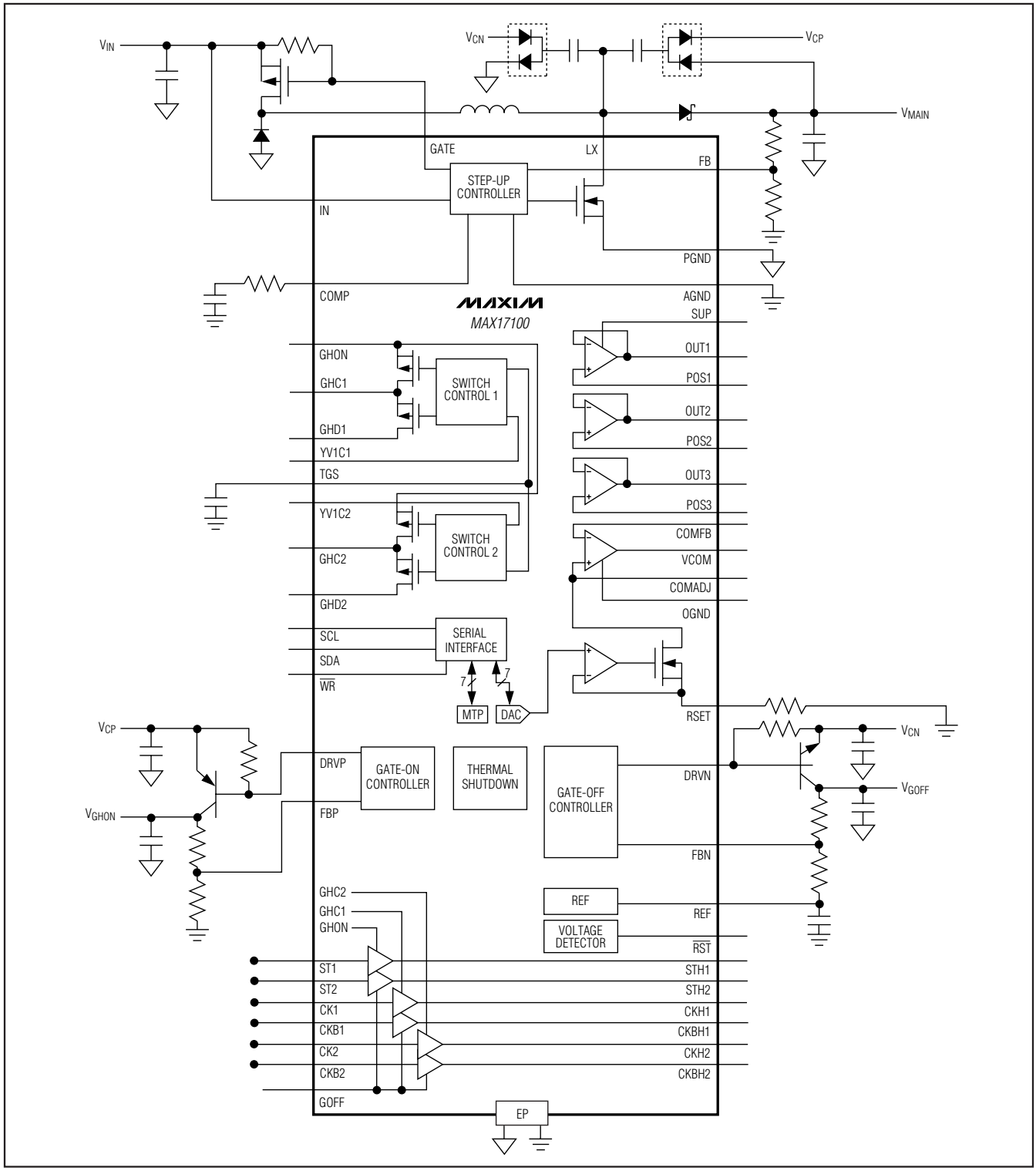


Figure 3. Functional Diagram

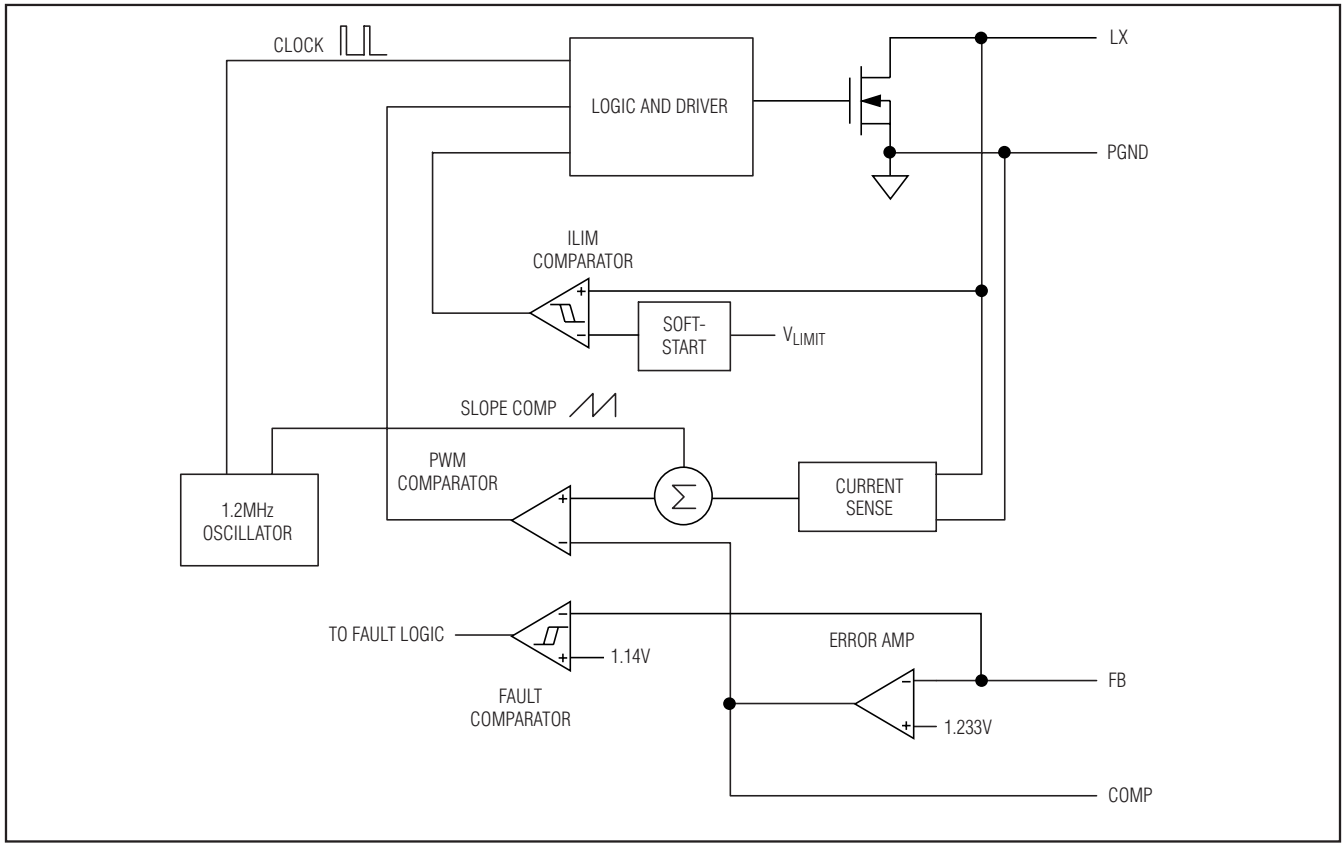


Figure 4. Step-Up Regulator Functional Diagram

Figure 4 shows the functional diagram of the step-up regulator. An error amplifier compares the signal at FB to 1.233V and changes the COMP output. The voltage at COMP sets the peak inductor current. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope-compensation signal is summed with the current-sense signal. On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceeds the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the boost diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

Internal-Switch Boost Regulator with Integrated Scan Driver, VCOM Calibrator, and Op Amp for TFT LCDs

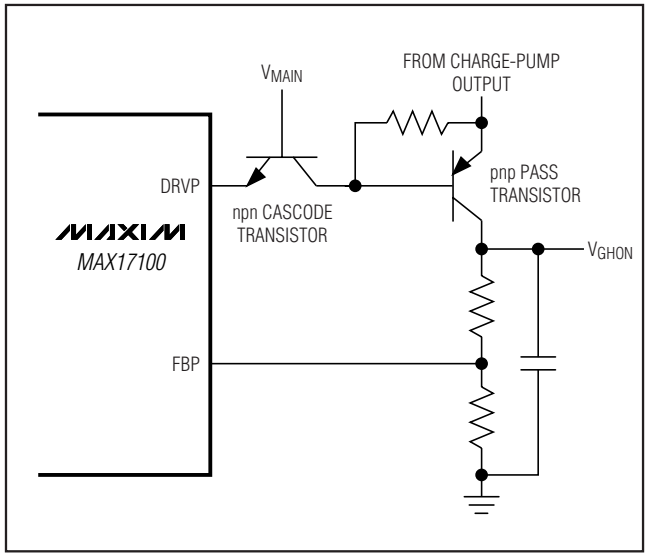


Figure 5. Using Cascaded npn for Charge-Pump Output Voltages > 36V

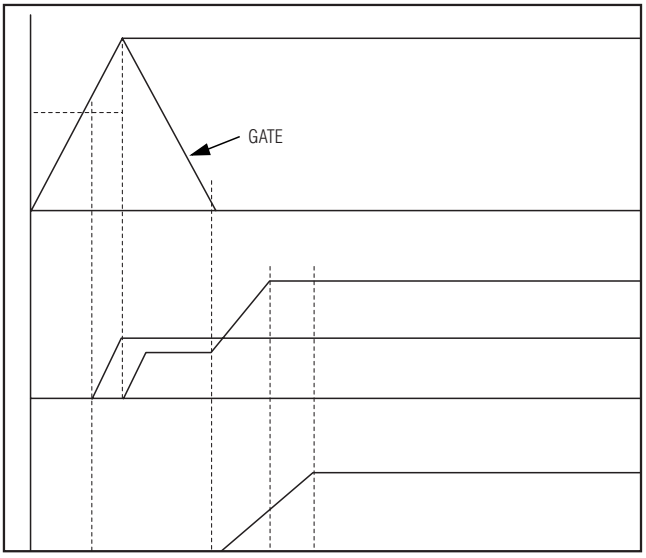


Figure 6. Linear Regulator Controls the Intermediate Charge-Pump Stage

Gate-On Linear-Regulator Controller (REG_P)

The gate-on linear-regulator controller is an analog gain block with an open-drain n-channel output. It drives an external pnp pass transistor with a 6.8kΩ base-to-emitter resistor (Figure 2). Its guaranteed base drive sink current is at least 1mA. The regulator including Q1 in Figure 2 uses a 0.47µF ceramic output capacitor and is designed to deliver 20mA at 25V. Other output voltages and currents are possible with the proper pass transistor and output capacitor. See the *Pass-Transistor Selection* and *Stability Requirements* sections. REG P is typically used to provide the TFT-LCD gate drivers' gate-on voltage. Use a charge pump with as many stages as necessary to obtain a voltage exceeding the required gate-on voltage (see the *Selecting the Number of Charge-Pump Stages* section). Note the voltage rating of DRVP is 36V. If the charge-pump output voltage can exceed 36V, an external cascode npn transistor should be added as shown in Figure 5. Alternately, the linear regulator can control an intermediate charge-pump stage while regulating the final charge-pump output (Figure 6). REG P is enabled after the GATE voltage reaches the gate-on threshold voltage (1.5V typ). Each time it is enabled, the controller goes through a soft-start routine that ramps up its internal reference DAC in 128 steps.

Gate-Off Linear-Regulator Controller (REG N)

The gate-off linear-regulator controller (REG N) is an analog gain block with an open-drain p-channel output. It drives an external npn pass transistor with a 6.8kΩ base-to-emitter resistor (Figure 2). Its guaranteed base-drive source current is at least 1mA. The regulator including Q2 in Figure 2 uses a 0.47µF ceramic output capacitor and is designed to deliver 20mA at -10V. Other output voltages and currents are possible with the proper pass transistor and output capacitor (see the *Pass-Transistor Selection* and *Stability Requirements* sections). REG N is typically used to provide the TFT-LCD gate drivers' gate-off voltage. A negative voltage can be produced using a charge-pump circuit as shown in Figure 2. REG N is enabled after the GATE voltage reaches the gate-on threshold voltage (1.5V typ). Each time it is enabled, the control goes through a soft-start routine that ramps down its internal reference DAC from V_{REF} to 250mV in 128 steps.

Operational Amplifiers

The MAX17100 has three operational amplifiers. The operational amplifiers are typically used as the gamma-correction divider string. They feature 45V/µs slew rate, and 20MHz 3dB bandwidth. The rail-to-rail input and output capability maximizes application flexibility.

Short-Circuit Current Limit

The operational amplifiers limit short-circuit current to approximately ±200mA if the output is directly shorted to SUP or to OGND. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+160°C typ). Once the junction temperature reaches the thermal-shutdown threshold, an internal thermal sensor immediately sets the thermal fault latch, shutting off all the IC's outputs. The device remains inactive until the input voltage is cycled.

Undervoltage Lockout (UVLO)

The UVLO circuit compares the input voltage at IN with the UVLO threshold (2.25V typ) to ensure the input voltage is high enough for reliable operation. The wider 140mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup procedure begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the main step-up regulator and the linear regulators, pulls GATE high to turn off the external series p-channel MOSFET and disables the switch control block. The operational-amplifier outputs become high impedance at this time.

Reference Voltage (REF)

The reference output is nominally 1.25V and can source at least 50µA. Bypass REF with a 0.22µF ceramic capacitor connected between REF and AGND.

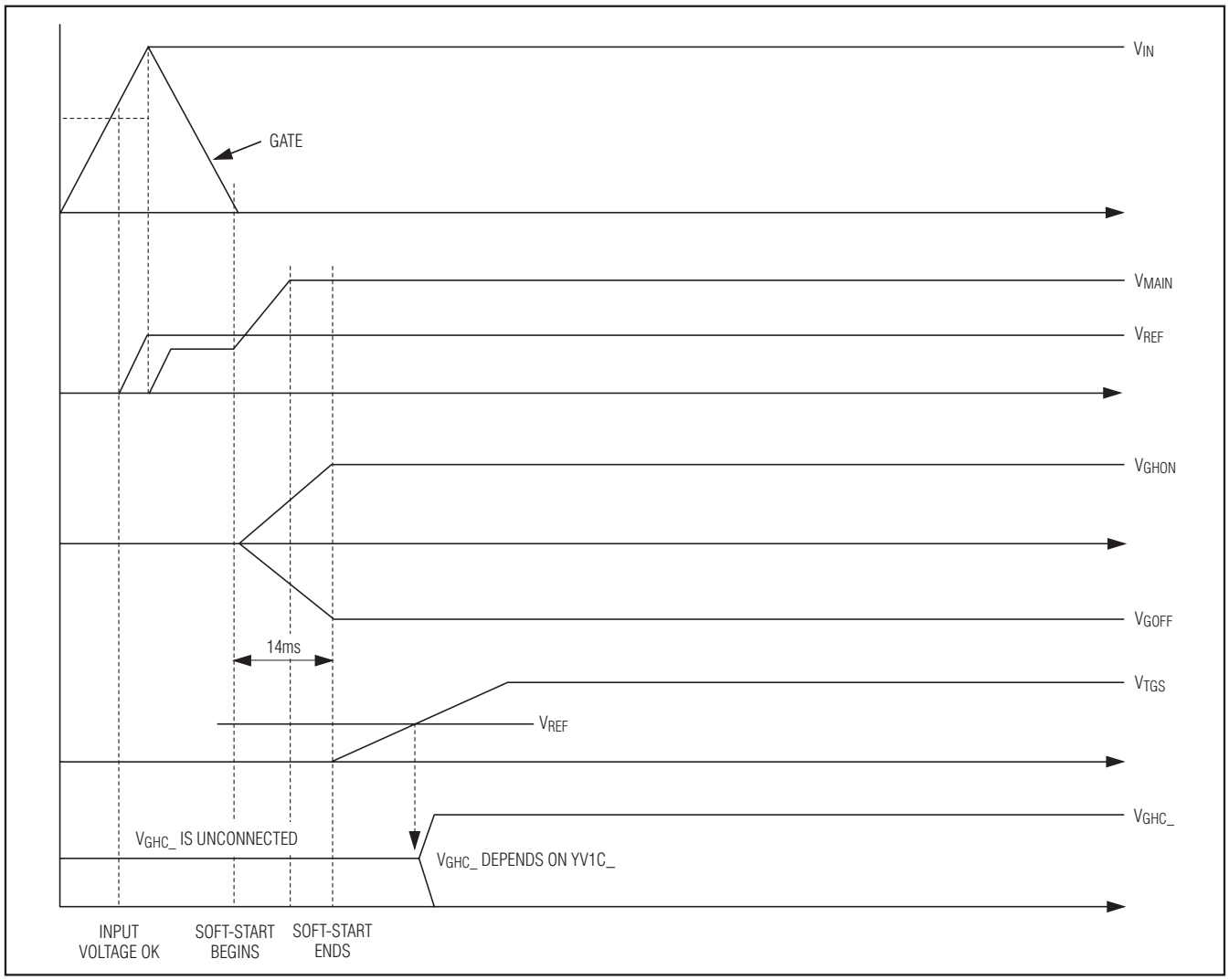


Figure 7. Power-Up Sequence

Internal-Switch Boost Regulator with Integrated Scan Driver, VCOM Calibrator, and Op Amp for TFT LCDs

Power-Up Sequence and Soft-Start

Once IN exceeds approximately 2.25V, the reference turns on. And then GATE is pulled high. When the reference voltage exceeds 1.0V (typ), GATE is pulled low to turn on the external p-channel MOSFET if no output fault is detected. Then the IC enables the main step-up regulator, the gate-on linear-regulator controller, and the gate-off linear-regulator controller simultaneously.

The IC employs soft-start for each regulator to minimize inrush current and voltage overshoot and to ensure a well-defined startup behavior. Each output uses a 7-bit soft-start DAC. For the step-up and the gate-on linear regulator, the DAC output is stepped in 128 steps from zero up to the reference voltage. For the gate-off linear regulator, the DAC output steps from the reference down to 250mV in 128 steps. The soft-start duration is 14ms (typ) for all three regulators.

A capacitor (CTGS) from TGS to AGND determines two switch-control blocks' startup delay. After the soft-start routine for each regulator is complete without any fault, a 5µA current source starts charging CTGS. Once the capacitor voltage exceeds 1.25V (typ), both the switch-control blocks are enabled as shown in Figure 7. After the switch-control blocks are enabled, GHC_ can be connected to GHON or GHD_ through the internal p-channel switches, depending upon the state of YV1C_. Before startup and when IN is less than UVLO, TGS is internally connected to AGND to discharge CTGS. Select CTGS to set the delay time using the following equation:

$$C_{TGS} = DELAY\_TIME \times \frac{5\mu A}{1.25V}$$

Switch-Control Block

The switch-control inputs (YV1C1 and YV1C2) are not activated until all four of the following conditions are satisfied: the input voltage exceeds UVLO, the soft-start routine of all the regulators is complete, a no fault condition is detected, and VTGS exceeds its turn-on threshold. Once activated and if YV1C_ is high, the 6Ω (typ) internal p-channel switch between GHON and GHC_ turns on and the 30Ω (typ) p-channel switch between GHD_ and GHC_ turns off. If YV1C_ is low, the 6Ω (typ) internal p-channel switch between GHON and GHC_ turns off and the 30Ω (typ) p-channel switch between GHD_ and GHC_ turns on.

Reset Function

The MAX17100 provides a $\overline{RST}$ signal to the system for reset purpose and at the same time the signal is used internally to control the timing when IC starts to download data from nonvolatile setting memory to the VCOM calibrator. Below is the sequence description for reset function:

a) When V_{IN} is less than 1.0V, $\overline{RST}$ is of undefined state.

b) $\overline{RST}$ will be pulled low once V_{IN} exceeds 1.0V.

c) Once V_{IN} exceeds V_{UVLO}, V_{REF} will start up. When V_{REF} is higher than 1.0V, $\overline{RST}$ will be released and its output becomes high impedance. External RC (Figure 8) will be charged up by their pullup voltage.

d) When $\overline{RST}$ reaches the threshold voltage (1.25V) during charging up, the serial controller will start to download data from the nonvolatile memory to the VCOM calibrator's internal register. At this time, the system device's like timing controller will also be reset.

The sequence is shown in Figure 9.

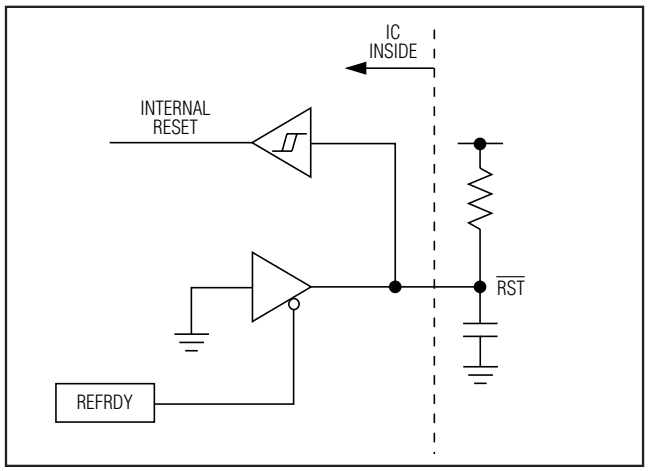


Figure 8. Reset Functional Diagram

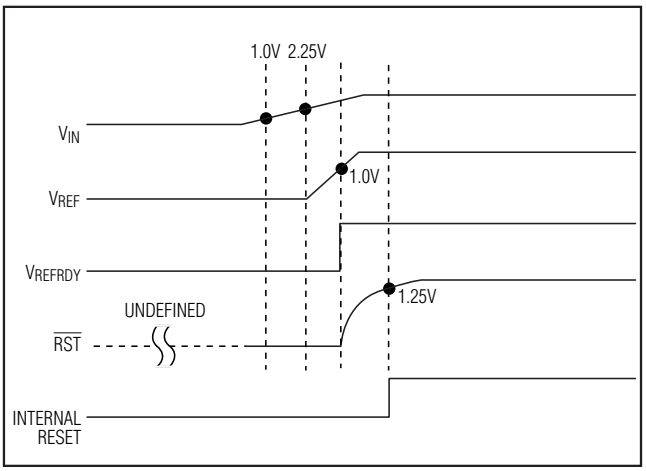


Figure 9. Reset Function Sequence

XAO Function

Once V_{IN} drops below IN UVLO, the high-side p-channel MOSFETs of the two high-voltage switch-control blocks will be forced to turn on regardless of YV1C_ and TGS. In the meantime, STH_ and CKH will be pulled high and CKBH_ will be of high-impedance state.

Fault Protection

During steady-state operation, if the output of the main regulator or any of the linear-regulator outputs does not exceed its respective fault-detection threshold, the MAX17100 activates an internal fault timer. If any condition or combination of conditions indicates a continuous fault for the fault-timer duration (218ms typ), the MAX17100 sets the fault latch to shut down all the outputs and turn off the external p-channel MOSFET (GATE is pulled high) except the reference. Once the fault condition is removed, cycle the input voltage (below the UVLO falling threshold) to clear the fault latch and reactivate the device.

The MAX17100 also provides overvoltage protection for the output of the step-up converter by monitoring the SUP pin. During normal operation, if SUP is higher than the threshold voltage (19V typ), the step-up converter will stop switching and prevent excessive voltage from damaging the MAX17100. Once SUP drops below the threshold voltage, the step-up converter will restart and regulate the needed output voltage.

Thermal-Overload Protection

Thermal-overload protection prevents excessive power dissipation from overheating the MAX17100. When the junction temperature exceeds T_J = +160°C (typ), a thermal sensor immediately activates the fault protection, which shuts down all outputs and turns off the external p-channel MOSFET (GATE is pulled high) except the reference, allowing the device to cool down. Cycling the input voltage (below the UVLO falling threshold) to clear the fault latch and reactivate the device. The thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

High-Voltage Level-Shifting Scan Driver

The MAX17100 includes six independent high-voltage level-shifting scan drivers to drive the gate lines of the TFT panel. The driver outputs (STH1, STH2, CKH1, CKBH1, CKH2, and CKBH2) swing between their power-supply rails (V_{GHON} and V_{GOFF}) according to the input logic levels on the block's inputs (ST1, ST2, CK1, CKB1, CK2, and CKB2). The driver output is at V_{GOFF} when its respective input is logic-low, and at V_{GHON} when its respective input is logic-high. These output signals have a maximum range of +35V and -15V.

VCOM Calibrator

The VCOM calibrator is a solid-state alternative to mechanical potentiometers used for adjusting the LCD backplane voltage (VCOM) in TFT LCD displays. The noninverting input of VCOM, COMADJ, is internally connected to a programmable sink current source, which sets the VCOM level (Figure 10). An internal 7-bit DAC controls the sink current and allows the user to increase or decrease the VCOM level by a 2-wire serial interface. The DAC is ratiometrically relative to the SUP voltage and is monotonic over all operating conditions. The user stores the DAC setting in the internal nonvolatile memory block. On power-up, the MTP presets the DAC to the last stored setting. The 2-wire serial interface between the system controller and the programming circuit adjusts the DAC and programs the MTP when $\overline{WR}$ is low. The resistive voltage-divider and the SUP supply set the maximum value of VCOM. The sink current from the voltage-divider reduces the COMADJ voltage level and VCOM output. The external resistor at R_{RSET} sets the full-scale sink current and the minimum value of VCOM.

Driving Pure Capacitive Load

In general, the LCD backplane (VCOM) consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation.

As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between OUT_ and the capacitive load reduces peaking but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω, and the typical value of the capacitor is 10nF.

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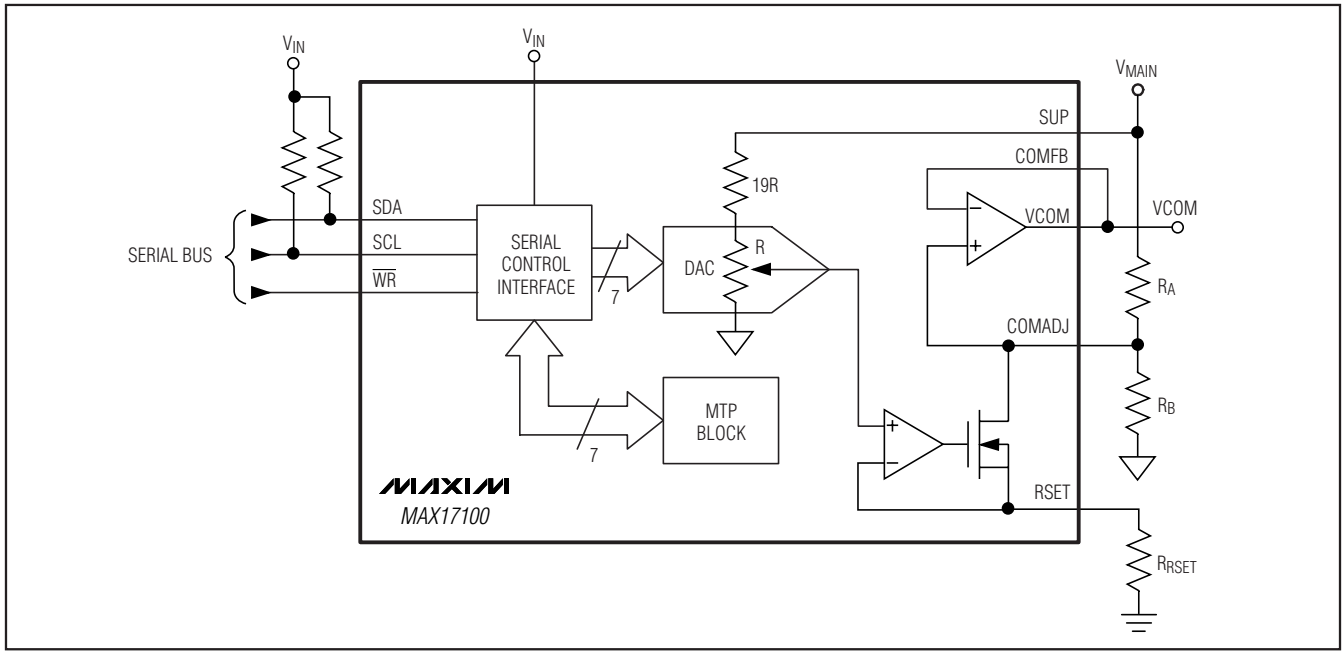

Figure 10. VCOM Calibrator Functional Diagram

Design Procedures

Step-Up Regulator

Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output load capability, transient-response time, and output voltage ripple. Size and cost are also important factors to consider.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and conduction losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase size and can increase conduction losses in the inductor. Low inductance values decrease the size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.6. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD-panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{MAIN(MAX)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics* section, and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{IN}}{V_{MAIN}}\right)\left(\frac{V_{MAIN}-V_{IN}}{I_{MAIN(MAX)} \times f_{OSC}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage ($V_{IN(MIN)}$) using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from the appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(MAX)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times (V_{MAIN} - V_{IN(MIN)}}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX17100's LX current limit (I_{LIM}) should exceed I_{PEAK}, and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical operating circuit, the maximum load current ($I_{MAIN(MAX)}$) is 500mA with a 14V output and a typical input voltage of 5V. Choosing an LIR of 0.55 and estimating efficiency of 85% at this operating point:

$$L = (\frac{5V}{14V})^2 (\frac{14V - 5V}{0.5A \times 1.2MHz})(\frac{0.85}{0.55}) \approx 3.0\mu H$$

Using the circuit's minimum input voltage (4.5V) and estimating efficiency of 80% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.5A \times 14V}{4.5V \times 0.8} = 1.94A$$

The ripple current and the peak current are:

$$I_{RIPPLE} = \frac{4.5V \times (14V - 4.5V)}{3.0\mu H \times 14V \times 1.2MHz} = 0.848A$$

$$I_{PEAK} = 1.94A + \frac{0.848A}{2} \approx 2.36A$$

Output-Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}} (\frac{V_{MAIN} - V_{IN}}{V_{MAIN} \times f_{OSC}})$$

and

$$V_{RIPPLE(ESR)} \approx I_{PEAK} \times R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input-Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. Two 10µF ceramic capacitors are used in the typical applications circuit (Figure 2) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, C_{IN} can be reduced below the values used in the typical applications circuit. Ensure a low-noise supply at IN by using adequate C_{IN}.

Rectifier Diode

The MAX17100's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 3A Schottky diode complements the internal MOSFET well.

Output-Voltage Selection

The output voltage of the main step-up regulator can be adjusted by connecting a resistive voltage-divider from the output (V_{MAIN}) to AGND with the center tap connected to FB (see Figure 2). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times (\frac{V_{MAIN}}{V_{FB}} - 1)$$

where V_{FB}, the step-up regulator's feedback set point, is 1.233V. Place R1 and R2 close to the IC.

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Loop Compensation

Choose R_{COMP} to set the high-frequency integrator gain for fast transient response. Choose C_{COMP} to set the integrator zero to maintain loop stability. For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{253 \times V_{IN} \times V_{OUT} \times C_{OUT}}{L \times I_{MAIN(MAX)}}$$

$$C_{COMP} \approx \frac{I_{OUT)} \times C_{OUT}}{10 \times I_{MAIN(MAX)} \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient-response waveforms.

Setting the VCOM Adjustment Range

See Figure 10 for the VCOM calibrator functional diagram. The external resistive voltage-divider sets the maximum value of the VCOM adjustment range. R_{RSET} sets the full-scale sink current, I_{OUT}, which determines the minimum value of the VCOM adjustment range. Large R_{RSET} values increase resolution, but decrease the VCOM adjustment range. Calculate R_A, R_B, and R_{RSET} using the following procedure:

1) Choose the maximum VCOM level (V_{MAX}), the minimum VCOM level (V_{MIN}), and the V_{MAIN} supply voltage.
2) Select R_A between 10kΩ and 500kΩ based on the acceptable power loss from the V_{MAIN} supply rail connected to SUP.
3) Calculate R_B:

$$R_B = \frac{V_{MAX}}{V_{SUP} - V_{MAX}} \times R_A$$

4) Calculate R_{RSET}:

$$R_{RSET} = \frac{V_{MAX}}{20 \times (V_{MAX} - V_{MIN})} \times R_A$$

5) Verify that I_{RSET} does not exceed 120µA:

$$I_{RSET} = \frac{V_{SUP}}{20 \times R_{RSET}}$$

6) If I_{RSET} exceeds 120µA, return to step 2 and choose a larger value for R_A.
7) The resulting resolution is:

$$\frac{(V_{MAX} - V_{MIN})}{127}$$

A complete design example follows:

V_{MAX} = 4V, V_{MIN} = 2.4V, V_{SUP} = 8V

If R_A = 200kΩ, then R_B = 200kΩ, and R_{RSET} = 24.9kΩ. Resolution = 12.5mV.

Charge Pumps

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meet the output requirement. Figures 11 and 12 show the positive and negative charge-pump output voltages for a given V_{MAIN} for one-, two-, and three-stage charge pumps. The number of positive charge-pump stages is given by:

$$n_{POS} = \frac{V_{GHON} + V_{DROPOUT} - V_{MAIN}}{V_{MAIN} - 2 \times V_D}$$

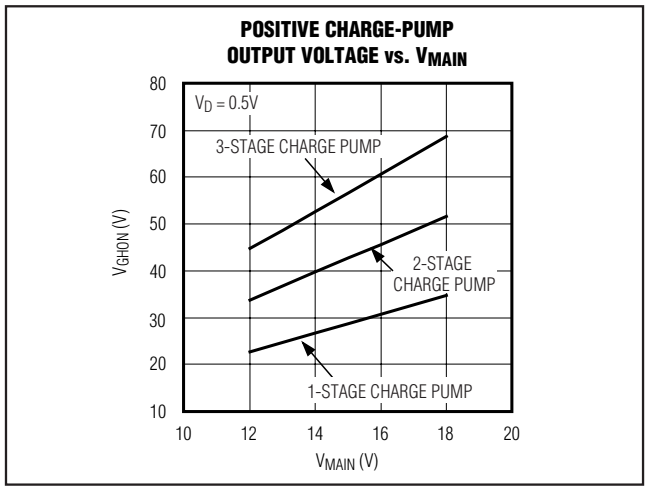

Figure 11. Positive Charge-Pump Output Voltage vs. V_{MAIN}

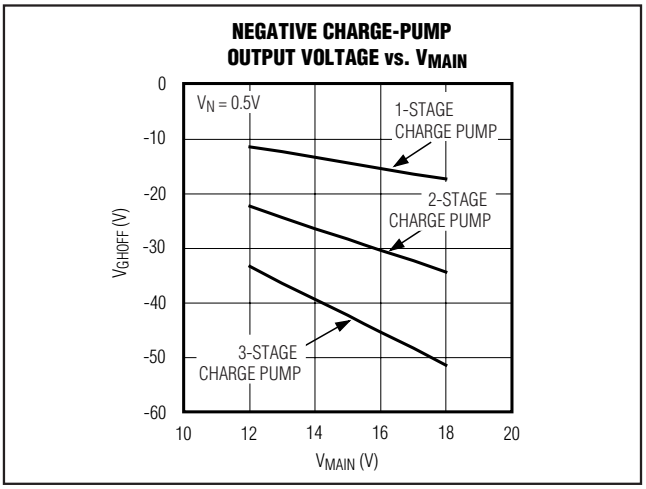

Figure 12. Negative Charge-Pump Output Voltage vs. V_{MAIN}

where n_{POS} is the number of positive charge-pump stages, V_{GHON} is the gate-on linear-regulator (REG P) output, V_{MAIN} is the main step-up regulator output, V_D is the forward-voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the linear regulator. Use $V_{DROPOUT}$ = 0.3V.

The number of negative charge-pump stages is given by:

$$n_{NEG} = \frac{-V_{GOFF} + V_{DROPOUT}}{V_{MAIN} - 2 \times V_D}$$

where n_{NEG} is the number of negative charge-pump stages, V_{GOFF} is the gate-off linear-regulator REG N output, V_{MAIN} is the main step-up regulator output, V_D is the forward-voltage drop of the charge-pump diode, and $V_{DROPOUT}$ is the dropout margin for the linear regulator. Use $V_{DROPOUT}$ = 0.3V.

The above equations are derived based on the assumption that the first stage of the positive charge pump is connected to V_{MAIN} and the first stage of the negative charge pump is connected to ground.

Sometimes fractional stages are more desirable for better efficiency. This can be done by connecting the first stage to V_{IN} or another available supply. If the first charge-pump stage is powered from V_{IN}, then the above equations become:

$$n_{POS} = \frac{V_{GHON} + V_{DROPOUT} + V_{IN}}{V_{MAIN} - 2 \times V_D}$$

$$n_{NEG} = \frac{-V_{GOFF} + V_{DROPOUT} + V_{IN}}{V_{MAIN} - 2 \times V_D}$$

Flying Capacitors

Increasing the flying capacitor (C_X) value lowers the effective source impedance and increases the output current capability. Increasing the capacitance indefinitely has a negligible effect on output-current capability because the internal switch resistance and the diode impedance place a lower limit on the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. The flying capacitor's voltage rating must exceed the following:

$$V_{CX} > n \times V_{MAIN}$$

where n is the stage number in which the flying capacitor appears and V_{MAIN} is the output voltage of the main step-up regulator.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{OUT\_CP} \geq \frac{I_{LOAD\_CP}}{2 f_{OSC} V_{RIPPLE\_CP}}$$

where C_{OUT_CP} is the output capacitor of the charge pump, I_{LOAD_CP} is the load current of the charge pump, and V_{RIPPLE_CP} is the peak-to-peak value of the output ripple.

Charge-Pump Rectifier Diodes

Use low-cost silicon switching diodes with a current rating equal to or greater than two times the average charge-pump input current. If it helps avoid an extra stage, some or all of the diodes can be replaced with Schottky diodes with an equivalent current rating.

Linear-Regulator Controllers

Output-Voltage Selection

Adjust the gate-on linear-regulator (REG P) output voltage by connecting a resistive voltage-divider from the REG P output to AGND with the center tap connected to FBP (Figure 2). Select the lower resistor of the divider R5 in the range of 10kΩ to 30kΩ. Calculate the upper resistor, R4, with the following equation:

$$R4 = R5 \times \left(\frac{V_{GHON}}{V_{FBP}} - 1\right)$$

where V_{FBP} = 1.25V (typ).

Adjust the gate-off linear-regulator REG N output voltage by connecting a resistive voltage-divider from V_{GOFF} to REF with the center tap connected to FBN (Figure 2). Select R8 in the 20kΩ to 50kΩ range. Calculate R7 with the following equation:

$$R7 = R8 \times \frac{V_{FBN} - V_{GOFF}}{V_{REF} - V_{FBN}}$$

where V_{FBN} = 250mV, V_{REF} = 1.25V. Note that REF can only source up to 50µA; avoid using a resistor less than 20kΩ for R8 that results in higher bias current than REF can supply.

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Pass-Transistor Selection

The pass transistor must meet specifications for current gain ($h_{FE(MIN)}$), input capacitance, collector-emitter saturation voltage, and power dissipation. The transistor's current gain limits the guaranteed maximum output current to:

$$I_{LOAD(MAX)} = (I_{DRV} - \frac{V_{BE}}{R_{BE}}) \times h_{FE(MIN)}$$

where I_{DRV} is the minimum guaranteed base-drive current, V_{BE} is the transistor's base-to-emitter forward voltage drop, and R_{BE} is the pullup resistor connected between the transistor's base and emitter. Furthermore, the transistor's current gain increases the linear regulator's DC loop gain (see the *Stability Requirements* section), so excessive gain destabilizes the output. Therefore, transistors with current gain over 100 at the maximum output current can be difficult to stabilize and are not recommended unless the high gain is needed to meet the load-current requirements.

The transistor's saturation voltage at the maximum output current determines the minimum input-to-output voltage differential that the linear regulator can support. Also, the package's power dissipation limits the usable maximum input-to-output voltage differential. The maximum power-dissipation capability of the transistor's package and mounting must exceed the actual power dissipated in the device. The power dissipated equals the maximum load current ($I_{LOAD(MAX)\_LR}$) multiplied by the maximum input-to-output voltage differential:

$$P = I_{LOAD(MAX)\_LR} \times (V_{IN(MAX)\_LR} - V_{OUT\_LR})$$

where $V_{IN(MAX)\_LR}$ is the maximum input voltage of the linear regulator and V_{OUT_LR} is the output voltage of the linear regulator.

Stability Requirements

The MAX17100 linear-regulator controllers use an internal transconductance amplifier to drive an external pass transistor. The transconductance amplifier, the pass transistor, the base-emitter resistor, and the output capacitor determine the loop stability. The following applies to both linear-regulator controllers in the MAX17100.

The transconductance amplifier regulates the output voltage by controlling the pass transistor's base current. The total DC loop gain is approximately:

$$A_{V\_LR} \cong (\frac{10}{V_T}) \times [1 + (\frac{I_{BIAS} \times h_{EF}}{I_{LOAD\_LR}})] \times V_{REF}$$

where V_T is 26mV at room temperature and I_{BIAS} is the current through the base-to-emitter resistor (R_{BE}). For the MAX17100, the bias currents for both the gate-on and gate-off linear-regulator controllers are 0.1mA. Therefore, the base-to-emitter resistor for both linear regulators should be chosen to set 0.1mA bias current:

$$R_{BE} = \frac{V_{BE}}{0.1mA} = \frac{0.7V}{0.1mA} = 6.8k\Omega$$

The output capacitor and the load resistance create the dominant pole in the system. However, the internal amplifier delay, pass transistor's input capacitance, and the stray capacitance at the feedback node create additional poles in the system, and the output capacitor's ESR generates a zero. For proper operation, use the following equations to verify the linear regulator is properly compensated:

1) First, determine the dominant pole set by the linear regulator's output capacitor and the load resistor:

$$f_{POLE\_LR} = \frac{I_{LOAD(MAX)\_LR}}{2 \times C_{OUT\_LR} \times V_{OUT\_LR}}$$

The unity-gain crossover of the linear regulator is:

$$f_{CROSSOVER} = A_{V\_LR} \times f_{POLE\_LR}$$

2) The pole created by the internal amplifier delay is approximately 1MHz:

$$f_{POLE\_AMP} = 1MHz$$

3) Next, calculate the pole set by the transistor's input capacitance, the transistor's input resistance, and the base-to-emitter pullup resistor:

$$f_{POLE\_IN} = \frac{1}{2 \times C_{IN} \times (R_{BE} // R_{IN})}$$

where:

$$C_{IN} = \frac{g_m}{2 f_T}, \; R_{IN} = \frac{h_{FE}}{g_m}$$

g_m is the transconductance of the pass transistor and f_T is the transition frequency. Both parameters can be found in the transistor's data sheet. Because R_{BE} is much greater than R_{IN}, the above equation can be simplified:

$$f_{POLE\_IN} = \frac{1}{2\pi \times C_{IN} \times R_{IN}}$$

Substituting for C_{IN} and R_{IN} yields:

$$f_{POLE\_IN} = \frac{f_T}{h_{FE}}$$

4) Next, calculate the pole set by the linear regulator's feedback resistance and the capacitance between FB_ and AGND (including stray capacitance):

$$f_{POLE\_FB} = \frac{1}{2\pi \times C_{FB} \times (R_{UPPER} // R_{LOWER})}$$

where C_{FB} is the capacitance between FB_ and AGND, R_{UPPER} is the upper resistor of the linear regulator's feedback divider, and R_{LOWER} is the lower resistor of the divider.

5) Next, calculate the zero caused by the output capacitor's ESR:

$$f_{POLE\_ESR} = \frac{1}{2\pi \times C_{OUT\_LR} \times R_{ESR}}$$

where R_{ESR} is the equivalent series resistance of C_{OUT_LR}. To ensure stability, choose C_{OUT_LR} large enough so the crossover occurs well before the poles and zero calculated in steps 2 to 5. The poles in steps 3 and 4 generally occur at several megahertz, and using ceramic capacitors ensures the ESR zero occurs at several megahertz as well. Placing the crossover below 500kHz is sufficient to avoid the amplifier-delay pole and generally works well, unless unusual component choices or extra capacitances move one of the other poles or the zero below 1MHz.

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the step-up regulator and the power dissipated by the operational amplifiers.

Step-Up Regulator

The largest portions of power dissipation in the step-up regulator are the internal MOSFET, the inductor, and the output diode. If the step-up regulator has 90% efficiency, approximately 3% to 5% of the power is lost in the internal MOSFET, approximately 3% to 4% in the inductor, and approximately 1% in the output diode. The remaining 1% to 3% is distributed among the input and output capacitors and the PCB traces. If the input power is about 5W, the power lost in the internal MOSFET is approximately 150mW to 250mW. Use the following formula to estimate the power loss on the built-in power MOSFET:

$$P_{LX\_ON} \approx (I_{IN(DC,MAX)} \times \sqrt{D})^2 \times R_{DSON}$$

where R_{DSON} is the on-resistance for the power MOSFET. The switching losses have not been accounted for in this calculation.

Level-Shifting Scan Driver

The power dissipation in the IC per level-shifter output depends on the level-shifter operating frequency (f_{LS}), the voltage differential between V_{GHON} and V_{GOFF}, and the level-shifter output resistance.

The power for each dissipation each channel can be calculated by:

$$P_{LSO} = \frac{C_{PANEL}(V_{GHON} - V_{GOFF})^2 \times f_{LS}}{2} \times \left(\frac{R_{d1}}{R_{PANEL} + R_{d1}} + \frac{R_{d2}}{R_{PANEL} + R_{d2}}\right)$$

where R_{PANEL} and C_{PANEL} are the equivalent resistance and capacitance of the panel, R_{d1} and R_{d2} are the output resistance of the scan drivers.

Since two channels (STH1, STH2) are used as the start-pulse signal, the operating frequency is much lower compared to other channels. The power dissipation for both channels can be ignored.

Operational Amplifiers

The power dissipated in the operational amplifier (including programmable VCOM calibrator) depends on the output current, the output voltage, and the supply voltage:

$$PD_{SOURCE} = I_{OUT\_SOURCE} \times (V_{SUP} - V_{OUT})$$

$$PD_{SINK} = I_{OUT\_SINK} \times V_{OUT}$$

where I_{OUT_SOURCE} is the output current sourced by the operational amplifier and I_{OUT_SINK} is the output current that the operational amplifier sinks.

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VCOM Calibrator Interface

The MAX17100 is a slave-only device with a serial address of 9Eh. The 2-wire serial interface (pins SCL and SDA) is designed to attach to a 1.8V to 4V serial bus. Connect both SCL and SDA lines to the V_{IN} supply through individual pullup resistors. Calculate the required value of the pullup resistors using:

$$R_{PULLUP} \le \frac{t_R}{C_{BUS}}$$

where t_R is the rise time in the *Electrical Characteristics* and C_{BUS} is the total capacitance on the bus.

The MAX17100 uses a nonstandard serial interface protocol with mostly standard voltage and timing parameters, as defined in the following subsections.

BUS Free

Both data and clock lines remain HIGH. Data transfers can be initiated only when the bus is not busy (Figure 13).

START Condition (S)

Starting from an idle bus state (both SDA and SCL are high), a HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition from a master device on the bus.

STOP Condition (P)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition from the master device.

DATA Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. The master generates one clock pulse per bit of data during write operations and the slave device outputs 1 data bit per clock pulse during read operations. Each data transfer is initiated with a START condition and terminated with a STOP condition. Two bytes are transferred between the START and STOP conditions.

Slave Address

After generating a START condition, the bus master transmits the slave address consisting of the 7-bit device code (b1001111 or 9Eh) for the MAX17100 (Figure 14). For a read operation, the 8th bit is 1 and for write operations it is 0. The MAX17100 continuously monitors the bus for its corresponding slave address. It generates an acknowledge bit if it recognizes its slave address and it is not busy programming the MTP.

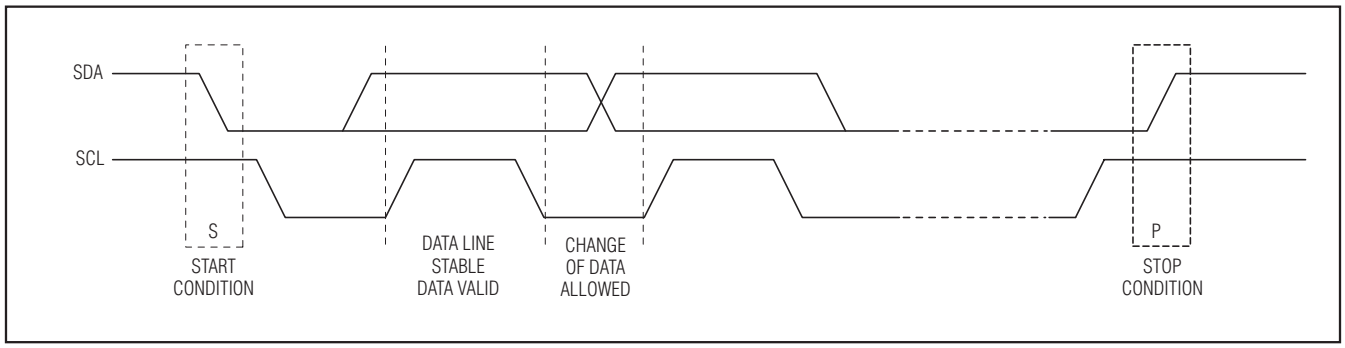

Figure 13. Serial Bus START, STOP, and Data Change Conditions

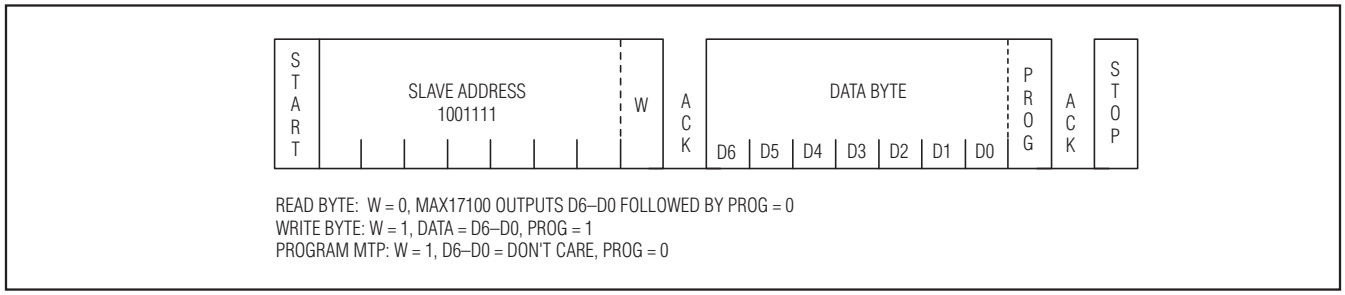

Figure 14. Serial Slave Address and Data Byte

Data Byte

The data byte follows successful transmission of the MAX17100's slave address (Figure 14). For a read operation, the MAX17100 will output the 7 bits corresponding to the current DAC setting followed by a 0 bit. For a write operation, the bus master must provide the 7-bit data corresponding to the desired DAC setting followed by a 1 bit. To program the IC's MTP, the master must make the last bit a zero, in which case the other 7 bits of data are ignored. For programming, SUP must exceed its programming threshold (8V min). Otherwise, programming will not occur and the MAX17100 will not acknowledge the programming command.

DAC Values

Table 3 lists the DAC values and the corresponding I_{RSET}, V_{RSET} and V_{VCOM} values.

Table 3. DAC Settings

7-BIT DATA BYTE	I_{RSET}	V_{RSET} (V)	V_{VCOM} (V)
0000000	$I_{RSET(MIN)}$	$V_{RSET(MIN)}$	V_{MAX}
0000001	$I_{RSET(MIN)}$ + 1 LSB	$V_{RSET(MIN)}$ + 1 LSB	V_{MAX} - 1 LSB
. . .	. . .	. . .	. . .
1111110	$I_{RSET(MAX)}$ - 1 LSB	$V_{RSET(MAX)}$ - 1 LSB	V_{MIN} + 1 LSB
1111111	$I_{RSET(MAX)}$	$V_{RSET(MAX)}$	V_{MIN}

Acknowledge/Polling

The MAX17100, when addressed, generates an acknowledge pulse after the reception of each byte (Figure 15). The master device must generate an extra clock pulse which is associated with this acknowledge bit. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. The master signals an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave leaves the data line HIGH to enable the master to generate the STOP condition.

The MAX17100 does not generate an acknowledge while an internal programming cycle is in progress. Once the internally timed write cycle has started and the MTP inputs are disabled, acknowledge polling can be initiated. This involves sending a START condition followed by the device address byte. Only if the internal write cycle has completed does the MAX17100 respond with an acknowledge pulse, allowing the read or write sequence to continue.

The MAX17100 does not acknowledge a command to program the MTP if SUP is not high enough to properly program the device. Also, a program command must be preceded by a write command. The IC does not acknowledge a program command or program the MTP unless the DAC data has been modified since the most recent program command.

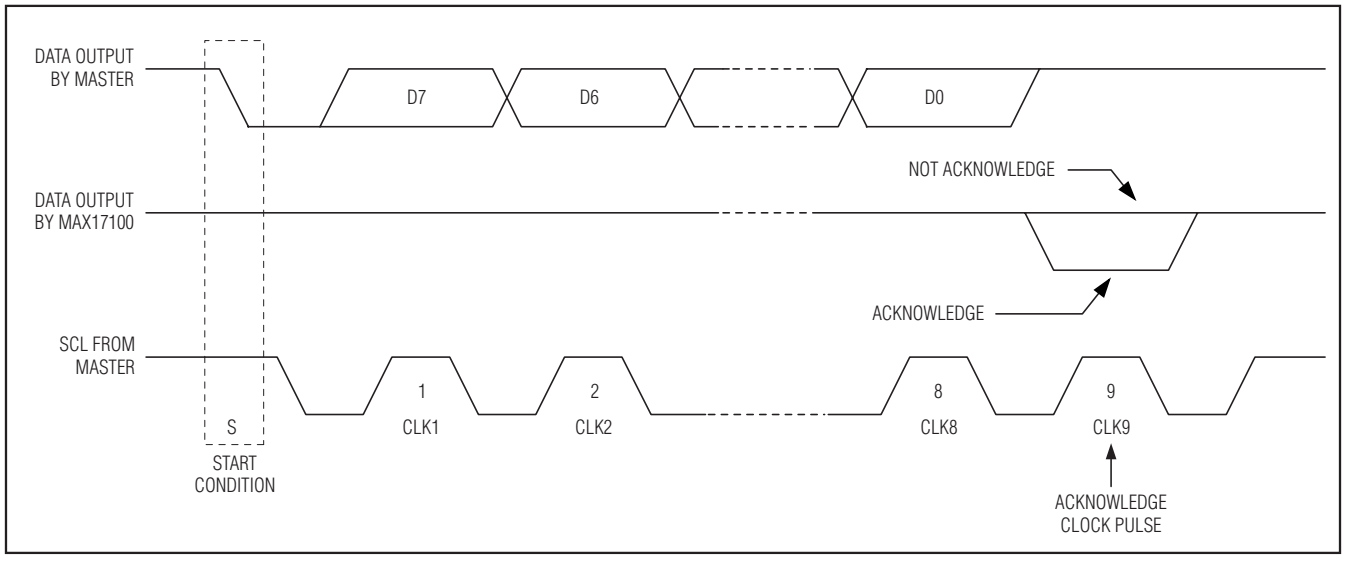

Figure 15. Serial Bus Acknowledge

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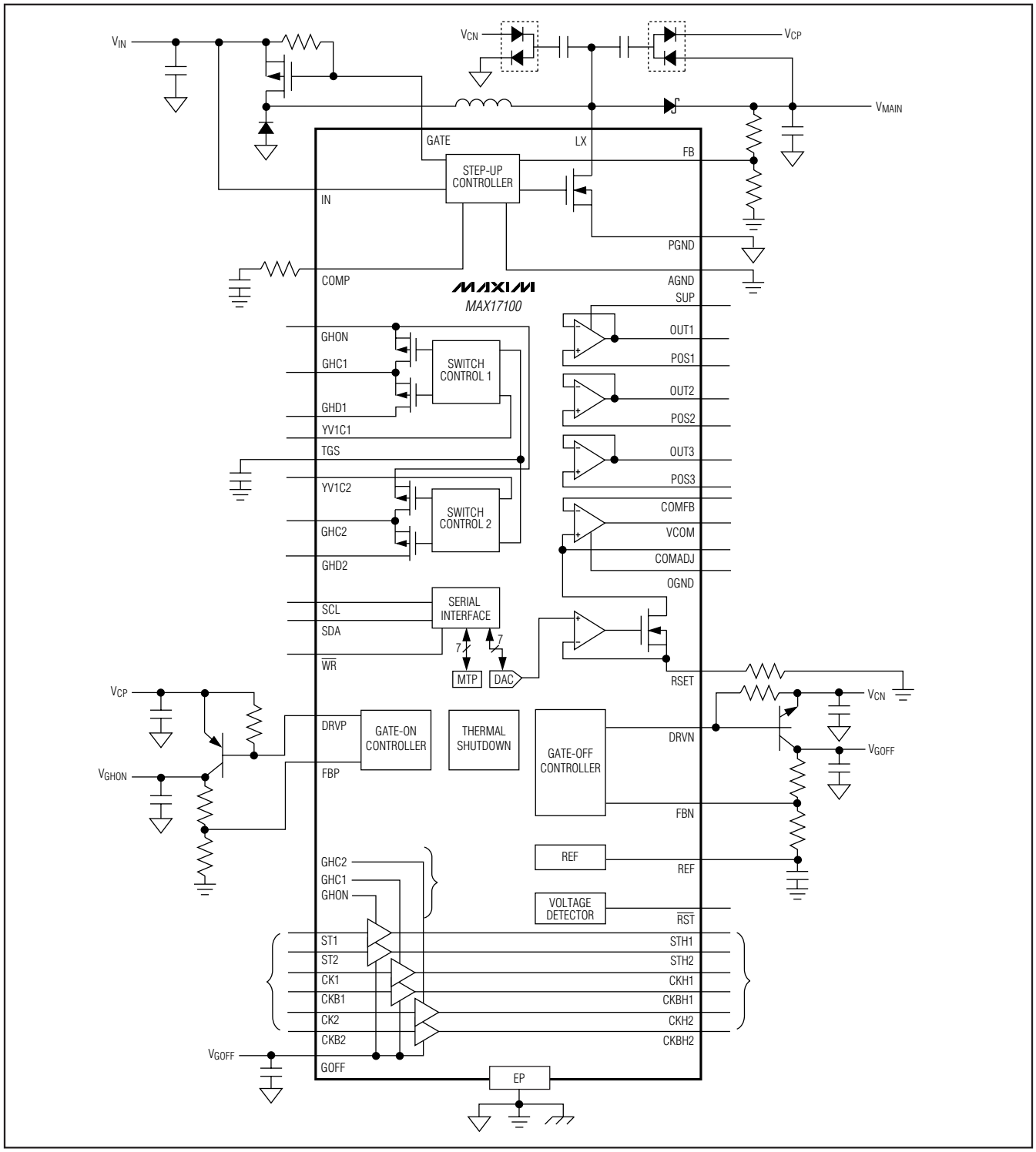
PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Minimize the area of high-current loops by placing the inductor, the output diode, and the output capacitors near the input capacitors and near the LX and PGND pins. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), and to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance. Create a power-ground island (PGND) consisting of the input and output capacitor grounds, PGND pin, and any charge-pump components. Connect all of these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes. Create an analog ground plane (AGND) consisting of the AGND pin, all the feedback-divider ground connections, the operational-amplifier divider ground connections, the COMP and TGS capacitor ground connections, and the device's exposed backside pad. Connect the AGND and PGND islands by connecting the PGND pin directly to the exposed backside pad. Make no other connections between these separate ground planes.
- Place all feedback voltage-divider resistors within 5mm of their respective feedback pins. The divider's center trace should be kept short. Placing the resistors far away causes their FB traces to become antennas that can pick up switching noise. Take care to avoid running any feedback trace near LX or the switching nodes in the charge pumps, or provide a ground shield.
- Place the IN pin and REF pin bypass capacitors as close to the device as possible. The ground connection of the IN bypass capacitor should be connected directly to the AGND pin with a wide trace.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from feedback nodes (FB, FBP, and FBN) and analog ground. Use DC traces to shield if necessary.

Refer to the MAX17100 Evaluation Kit for an example of proper PCB layout.

Minimal Operating Circuit



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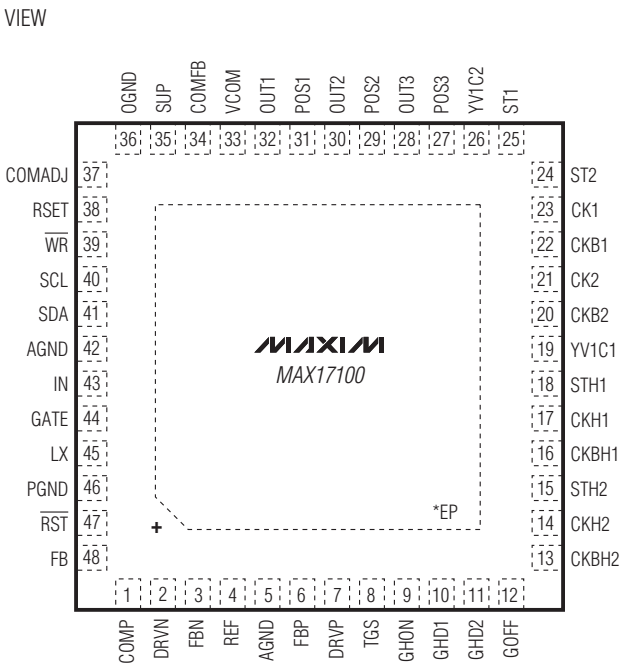
Pin Configuration



THIN QFN

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
48 TQFN	T4866+1	21-0141	90-0056

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/9	Initial release	—
1	8/10	Reduced test time	2, 3, 4, 6–10, 15, 21, 34, 35