

# DS21352DK T1 Single-Chip Transceiver Design Kit Daughter Card

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## GENERAL DESCRIPTION

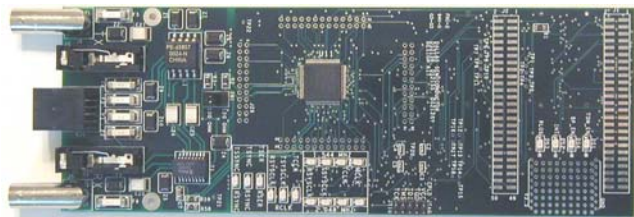
The DS21352 design kit is an easy-to-use evaluation board for the DS21352 T1 single-chip transceiver (SCT). The DS21352DK is intended to be used as a daughter card with either the DK2000 or the DK101 motherboards. The DS21352DK comes complete with an SCT, transformers, termination resistors, configuration switches, line-protection circuitry, network connectors, and motherboard connectors. The DK101/DK2000 motherboard and Dallas' ChipView software give point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status, as well as multiple clock and signal routing configurations.

Each DS21352DK is shipped with a free DK101 motherboard. For complex applications, the DK2000 high-performance demo kit motherboard can be purchased separately.

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## ORDERING INFORMATION

PART	DESCRIPTION
DS21352DK	DS21352 Design Kit Daughter Card (with included DK101 motherboard)



## FEATURES

- Demonstrates Key Functions of DS21352 T1 SCT Transceiver
- Includes DS21352 SCT, Transformers, Bantam, BNC and RJ48 Network Connectors, and Termination Passives
- Compatible with DK101 and DK2000 Demo Kit Motherboards
- DK101/DK2000 and ChipView Software Provide Point-and-Click Access to the DS21352 Register Set
- Software-Controlled (Register Mapped) Configuration Switches to Facilitate Clock and Signal Routing
- All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink
- LEDs for Loss-Of-Signal and Interrupt Status as well as Multiple Clock and Signal Routing Configurations
- Easy-to-Read Silk Screen Labels Identify the Signals Associated with all Connectors, Jumpers and LEDs
- Network Interface Protection for Overvoltage and Overcurrent Events

## DEMO KIT CONTENTS

- DS21352DK Design Kit Daughter Card
- DK101 Low-Cost Motherboard
- CD ROM
  - ChipView Software
  - DS21352DK Data Sheet
  - DK101 Data Sheet
  - DS21352 Data Sheet
  - DS21352 Errata Sheet

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## TABLE OF CONTENTS

<b>COMPONENT LIST</b> .....	<b>3</b>
<b>BASIC OPERATION</b> .....	<b>4</b>
HARDWARE CONFIGURATION .....	4
QUICK SETUP (DEMO MODE) .....	4
QUICK SETUP (REGISTER VIEW) .....	4
<b>REGISTER MAP</b> .....	<b>5</b>
CPLD REGISTER MAP .....	5
<b>DS21352 INFORMATION</b> .....	<b>8</b>
<b>DS21352DK INFORMATION</b> .....	<b>8</b>
<b>TECHNICAL SUPPORT</b> .....	<b>8</b>
<b>SCHEMATICS</b> .....	<b>8</b>
<b>DOCUMENT REVISION HISTORY</b> .....	<b>8</b>

## LIST OF TABLES

Table 1. Daughter Card Address Map .....	5
Table 2. CPLD Register Map .....	5

## COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1–C5, C8–C12, C15–C19, C21, C22, C29–C34	23	0.1 $\mu$ F 10%, 16V ceramic capacitors (0603)	Digi-Key	311-1088-1-ND
C7, C36	2	1 $\mu$ F 10%, 16V ceramic capacitors (1206)	Digi-Key	PCC1882CT-ND
C13, C14	2	0.1 $\mu$ F 10%, 16V ceramic capacitors (0805)	Digi-Key	311-1142-1-ND
C23	1	0.1 $\mu$ F 10%, 25V ceramic capacitor (1206)	Digi-Key	PCC1883CT-ND
C24–C27	4	0.22 $\mu$ F, 50V ceramic capacitors	Digi-Key	UNK
C35	1	10 $\mu$ F 20%, 16V tantalum capacitor (B case)	Digi-Key	PCS3106CT-ND
DS1, DS4–DS18	16	LED, green, SMD	Digi-Key	P501CT-ND
DS2, DS3	2	LED, red, SMD	Digi-Key	P500CT-ND
F1–F6	6	250V, 1.25A fuse, SMT	Teccor Electronics	F1250T
J1, J2	2	Male 0.1, SMD, 50-pin, dual-row vertical	Samtec	TSM-125-01-T-DV
J3, J4	2	Bantam connectors	SWK	RTT34B02
J5, J6	2	Connector BNC RA 5-pin	Kruvand	UCBJR220
J7–J9	3	Socket, SMD, 50-pin, dual-row vertical	Samtec	TFM-125-02-S-D-LC
JT10	1	Connector, 10-pin, dual-row vertical	Digi-Key	S2012-05-ND
L1	1	Choke, dual 4-line 24 $\mu$ H, 8-pin SO	Pulse Engineering	PE-65857
R1, R14, R21	3	51.1 $\Omega$ 1%, 1/8W resistors (1206)	Digi-Key	P51.1FCT-ND
R2, R3, R58, R59	4	0 $\Omega$ 5%, 1/8W resistors (1206)	Digi-Key	P0.0ETR-ND
R4, R5, R60	3	51.1 $\Omega$ 1%, 1/10W resistors (0805)	Digi-Key	P51.1CCT-ND
R6, R9, R10, R13, R15–R19, R22, R23, R25–R29, R32, R37, R38, R44, R47–R49, R61	24	10k $\Omega$ 1%, 1/10W resistors (0805)	Digi-Key	P10.0KCCT-ND
R7, R8, R11, R12, R30, R31, R35, R36, R39–R43, R45, R50–R53	18	330 $\Omega$ 0.1%, 1/10W MF resistors (0805)	Digi-Key	P330ZCT-ND
R24	1	1.0k $\Omega$ 1%, 1/10W resistor (0805)	Digi-Key	P1.00KCCT-ND
R33, R34	2	Not populated	—	Not populated
R46	1	4.7k $\Omega$ 1%, 1/8W resistor (0805)	Digi-Key	9C08052A4701FK HFT
R54, R55	2	61.9 $\Omega$ 1%, 1/8W resistors (1206)	Digi-Key	P61.9FCT-ND
R56, R57	2	49.9 $\Omega$ 1%, 1/8W resistors (1206)	Digi-Key	P49.9FCT-ND
RJ1	1	RJ48 connector	Molex	43223
SW1	1	Switch DPDT slide 6-pin TH	Avnet	SSA22
T1	1	XFMR 16-pin SMT	Pulse Engineering	TX1099
U1–U4, U6	5	BBUS switch 10-bit CMOS, 150-mil, 24-pin SO	IDT	IDTQS3R861Q
U5	1	144-pin macrocell CPLD	Avnet	XC95144XL- 10TQ100C
U7–U10	4	Quad bus switch, 150-mil, 16-pin SO	IDT	IDTQS3125Q
U11	1	T1/E1/J1 XCVR 100-pin QFP, 0°C to +70°C	Dallas Semiconductor	DS2156L
Z1, Z6–Z8	4	160V, 500A Sidactor	Teccor Electronics	P1800SCMC
Z2, Z3	2	58V, 500A Sidactor	Teccor Electronics	P0640SCMC
Z4, Z5	2	6V, 50A Sidactor	Teccor Electronics	P0080SAMC
Z9, Z10	2	25V, 500A Sidactor	Teccor Electronics	P0300SCMC

## BASIC OPERATION

This design kit relies upon several supporting files, which can be downloaded from our website at [www.maxim-ic.com/DS21352DK](http://www.maxim-ic.com/DS21352DK). See the DS21352DK QuickView data sheet for these files.

### Hardware Configuration

#### *Using the DK101 processor board:*

- Connect the daughter card to the DK101 processor board.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC\_3.3V. (The external 5V connector and the TIM 5V supply headers are unused.)
- All processor board DIP switch settings should be in the ON position with exception for the flash programming switch, which should be OFF.
- From the Programs menu, launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

#### *Using the DK2000 processor board:*

- Connect the daughter card to the DK2000 processor board.
- Connect J1 to the power supply that is delivered with the kit. Alternately, a PC power supply can be connected to connector J2.
- From the Programs menu, launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

#### *General:*

- Upon power-up the RLOS LED is lit, as well as the MCLK-2.048MHz and TCLK-2.048MHz LEDs.

### Quick Setup (Demo Mode)

- The PC loads the program, offering a choice among Demo Mode, Register View, and Terminal Mode. Select Demo Mode.
- The program requests a configuration file, then select DS21352DK\_DRVR.cfg.
- The Demo Mode screen appears. Upon external loopback, the LOS and OOF indicators extinguish.

### Quick Setup (Register View)

- The PC loads the program, offering a choice among Demo Mode, Register View, and Terminal Mode. Select Register View.
- The program requests a definition file, then select DS21352.def.
- The Register View screen appears, showing the register names, acronyms, and values. Note: During the definition file load process, all registers are initialized according to the init value filed in the definition file (because the SETUP field in the .def file is turned on).
- Predefined register settings for several functions are available as initialization files.
  - INI files are loaded by selecting the menu **File**→**Reg Ini File**→**Load Ini File**.
  - Load the INI file DS21352t1\_b8zs\_esf.ini.
  - After loading the INI file the following may be observed:
    - The RLOS LED extinguishes upon external loopback.
    - The device is now configured for T1 B8ZS ESF.

#### *Miscellaneous:*

- Clock frequencies and certain pin bias levels are provided by a register-mapped CPLD, which is on the DS21352 daughter card.
- The definition file for this CPLD is named DS215x\_35x\_CPLD\_V2.def. See the [CPLD Register Map](#) section for definitions.
- All files referenced above are available for download in the section marked “File Locations.”

## REGISTER MAP

The DK101 daughter card address space begins at 0x81000000.

The DK2000 daughter card address space begins at:

0x30000000 for slot 0  
 0x40000000 for slot 1  
 0x50000000 for slot 2  
 0x60000000 for slot 3

All offsets given in [Table 1](#) are relative to the beginning of the daughter card address space.

**Table 1. Daughter Card Address Map**

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0015	CPLD	Board identification and clock/signal routing
0X1000 to 0X10ff	Single-Chip Transceiver	Board is populated with one of the following: DS2155, DS2156, DS21352, or DS21354. Please see the data sheet(s) for details.

Registers in the CPLD can be easily modified using ChipView.exe, a host-based user interface software, along with the definition file named *DS215x\_35x\_CPLD\_V2.def*. Definition files for the SCT are named *DS2155.def*, *DS21352.def*, or *DS21354.def*, depending on the board population option.

## CPLD Register Map

**Table 2. CPLD Register Map**

OFFSET	NAME	TYPE	DESCRIPTION
0X0000	BID	Read-Only	Board ID
0X0002	XBIDH	Read-Only	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Board FAB Revision
0X0006	AREV	Read-Only	Board Assembly Revision
0X0007	PREV	Read-Only	PLD Revision
0X0011	SWITCH1	Read-Write	Pin to 1.544MHz
0X0012	SWITCH2	Read-Write	Pin to 2.048MHz
0X0013	SWITCH3	Read-Write	Pin-to-Pin Connect
0X0014	SWITCH4	Read-Write	Pin-to-Pin Connect
0X0015	LEVELS	Read-Write	Set Level on Pin 1 = 3.3V

## ID Registers

OFFSET	NAME	TYPE	VALUE	DESCRIPTION
0X0000	BID	Read-Only	0xD	Board ID
0X0002	XBIDH	Read-Only	0x0	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	0x0	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	0x5	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Displays current FAB revision	Board FAB Revision
0X0006	AREV	Read-Only	Displays current assembly revision	Board Assembly Revision
0X0007	PREV	Read-Only	Displays current PLD firmware revision	PLD Revision

## Control Registers

The control registers are used primarily to control several banks of FET switches that route clocks and backplane signals. Please note that certain register settings cause line contention, e.g., setting SWITCH1.4 and SWITCH2.4 both to 0 would drive MCLK with both 1.544MHz and 2.048MHz.

### SWITCH1: PIN TO 1.544MHz (OFFSET = 0x0011) INITIAL VALUE = 0xF

(MSB)

(LSB)

—	—	—	—	MCLK	TCLK	RSYSCLK	TSYSCLK
---	---	---	---	------	------	---------	---------

NAME	POSITION	FUNCTION
MCLK	SWITCH1.3	0 = Connect MCLK to the 1.544MHz clock 1 = Open Switch 1.4
TCLK	SWITCH1.2	0 = Connect TCLK to the 1.544MHz clock 1 = Open Switch 1.3
RSYSCLK	SWITCH1.1	0 = Connect RSYSCLK to the 1.544MHz clock 1 = Open Switch 1.2
TSYSCLK	SWITCH1.0	0 = Connect TSYSCLK to the 1.544MHz clock 1 = Open Switch 1.1

### SWITCH2: PIN TO 2.048MHz (Offset = 0x0012) INITIAL VALUE = 0x3

(MSB)

(LSB)

—	—	—	—	MCLK	TCLK	RSYSCLK	TSYSCLK
---	---	---	---	------	------	---------	---------

NAME	POSITION	FUNCTION
MCLK	SWITCH2.3	0 = Connect MCLK to the 2.048MHz clock 1 = Open Switch 2.4
TCLK	SWITCH2.2	0 = Connect TCLK to the 2.048MHz clock 1 = Open Switch 2.3
RSYSCLK	SWITCH2.1	0 = Connect RSYSCLK to the 2.048MHz clock 1 = Open Switch 2.2
TSYSCLK	SWITCH2.0	0 = Connect TSYSCLK to the 2.048MHz clock 1 = Open Switch 2.1

### SWITCH3: PIN-TO-PIN CONNECT (Offset = 0x0013) INITIAL VALUE = 0xF

(MSB)

(LSB)

—	—	—	—	TSS_RS	TCL_RC	RSY_RC	TSY_RC
---	---	---	---	--------	--------	--------	--------

NAME	POSITION	FUNCTION
TSS_RS	SWITCH3.3	0 = Connect TSSYNC to RSYNC 1 = Open Switch 3.4
TCL_RC	SWITCH3.2	0 = Connect TCLK to RCLK 1 = Open Switch 3.3
RSY_RC	SWITCH3.1	0 = Connect RSYSCLK to RCLK 1 = Open Switch 3.2
TSY_RC	SWITCH3.0	0 = Connect TSYSCLK to RCLK 1 = Open Switch 3.1

**SWITCH4: PIN-TO-PIN CONNECT (Offset = 0x0014) INITIAL VALUE = 0x3****(MSB)****(LSB)**

—	—	—	—	URCLK_2048	UTCLK_2048	RSER_TSER	RSYNC_TSYNC
---	---	---	---	------------	------------	-----------	-------------

NAME	POSITION	FUNCTION
URCLK_2048	SWITCH4.3	0 = Connect UR_CLK (TSSYNC) to 2.048MHz 1 = Open Switch 4.4
UTCLK_2048	SWITCH4.2	0 = Connect UT_CLK (TCHCLK) to 2.048MHz 1 = Open Switch 4.3
RSER_TSER	SWITCH4.1	0 = Connect RER to TSER 1 = Open Switch 4.2
RSYNC_TSYNC	SWITCH4.0	0 = Connect RSYNC to TSYNC 1 = Open Switch 4.1

**LEVELS: SET LEVEL ON PIN (Offset = 0x0015) INITIAL VALUE = 0x6****(MSB)****(LSB)**

—	—	—	—	—	BP_EN	PPCTDM_EN	TUSEL
---	---	---	---	---	-------	-----------	-------

NAME	POSITION	FUNCTION
—	LEVELS1.3	—
BP_EN	LEVELS1.2	0 = Enable IDT switches that connect the UTOPIA bus to daughter card header
PPCTDM_EN	LEVELS1.1	0 = Enable IDT switches that connect the TDM bus to the daughter card header
TUSEL	LEVELS1.0	0 = Set DS2156.TUSEL to enable TDM backplane 1 = Set DS2156.TUSEL to enable UTOPIA backplane

**Note (DS2156 only):** When the UTOPIA backplane is enabled (LEVELS.TUSEL = 1) there is a possibility for contention between the UTOPIA bus master and TSYCLK, TSER, and RSER. To avoid this, the following switches should be opened when the UTOPIA backplane is enabled: SWITCH1.0, SWITCH2.0, SWITCH3.0, and SWITCH4.1

## DS21352 INFORMATION

For more information about the DS21352, please consult the DS21352 data sheets available on our website at [www.maxim-ic.com/DS21352](http://www.maxim-ic.com/DS21352). Software downloads are also available for this design kit.

## DS21352DK INFORMATION

For more information about the DS21352DK, including software downloads, please consult the DS21352DK data sheet available on our website at [www.maxim-ic.com/DS21352DK](http://www.maxim-ic.com/DS21352DK).

## TECHNICAL SUPPORT

For additional technical support, please e-mail your questions to [telecom.support@dalsemi.com](mailto:telecom.support@dalsemi.com).

## SCHEMATICS

The DS21352DK schematics are featured in the following 13 pages.

## DOCUMENT REVISION HISTORY

REVISION DATE	DESCRIPTION
060303	Initial DS21352DK data sheet release.
011904	Updated the <i>General Description</i> and <i>Features</i> sections; added the <i>Demo Kit Contents</i> section.
012705	Updated schematics (removed component values for Fuse and Sidactor; see <i>Component List</i> ).
110106	Updated schematics.



# DS2156, DS2155, DS2135Y DESIGN KIT

### CONTENTS

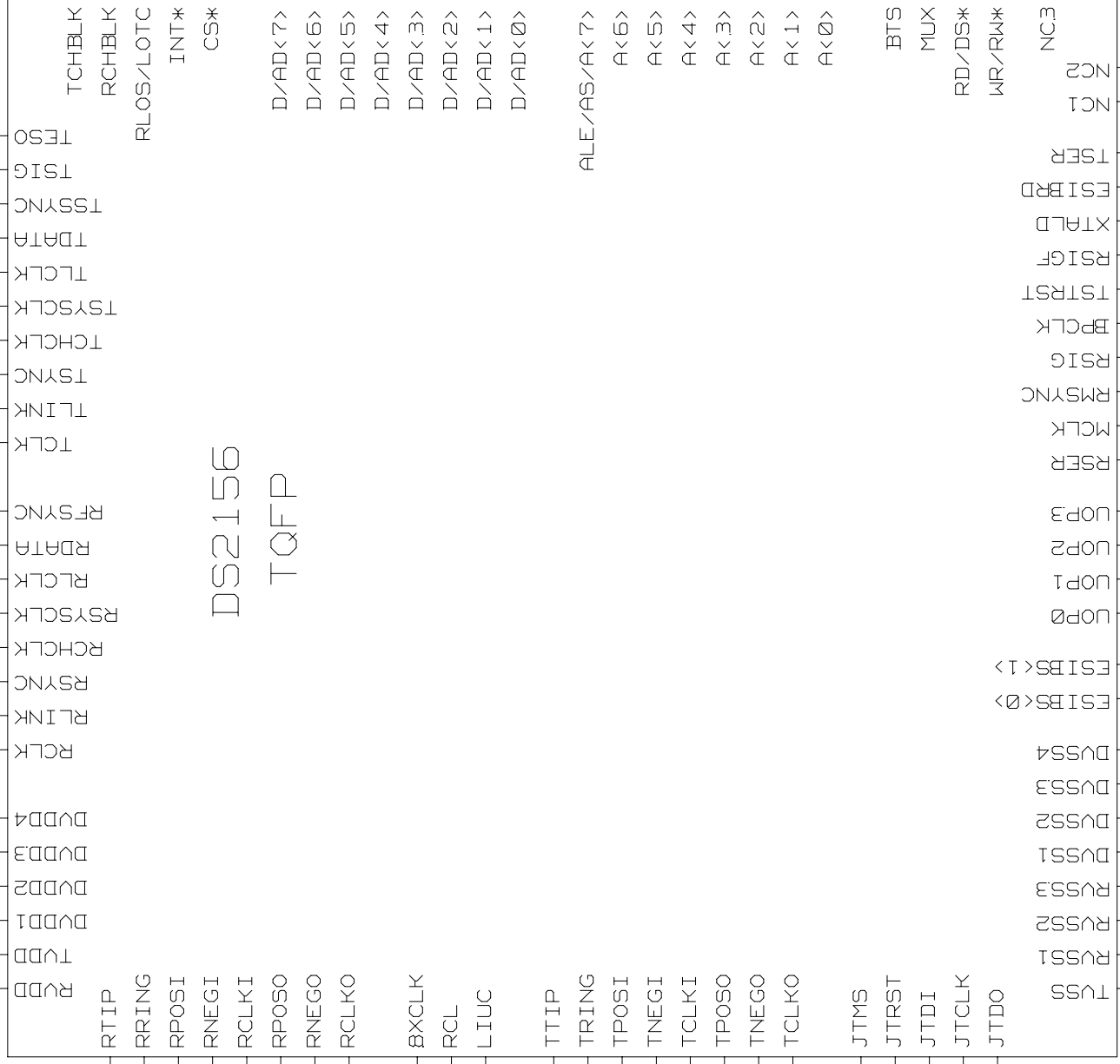
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2. SCT POPULATION OPTION (DS2155, DS2156, DS21352 OR DS21354)
3. TX AND RX ANALOG PATHS
4. TIM ADDRESS AND DATA BUS
5. CPLD ADDRESS DATA CONNECTIONS, BIAS LEVELS FOR SCT
6. UTOPIA: TIM HEADER AND BUS SWITCHES
7. TESTPOINTS FOR UTOPIA 2
8. UTOPIA: NETLIST ASSOCIATIONS
9. SWITCHING FOR CLOCKS AND TDM
10. SUPPLY DECOUPLING
11. SCT TESTPOINTS
12. NETLIST CROSS-REFERENCE
13. PART CROSS-REFERENCE

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ENGINEER:	STEVE SCULLY	PAGE:	1 / 13

DS2156L

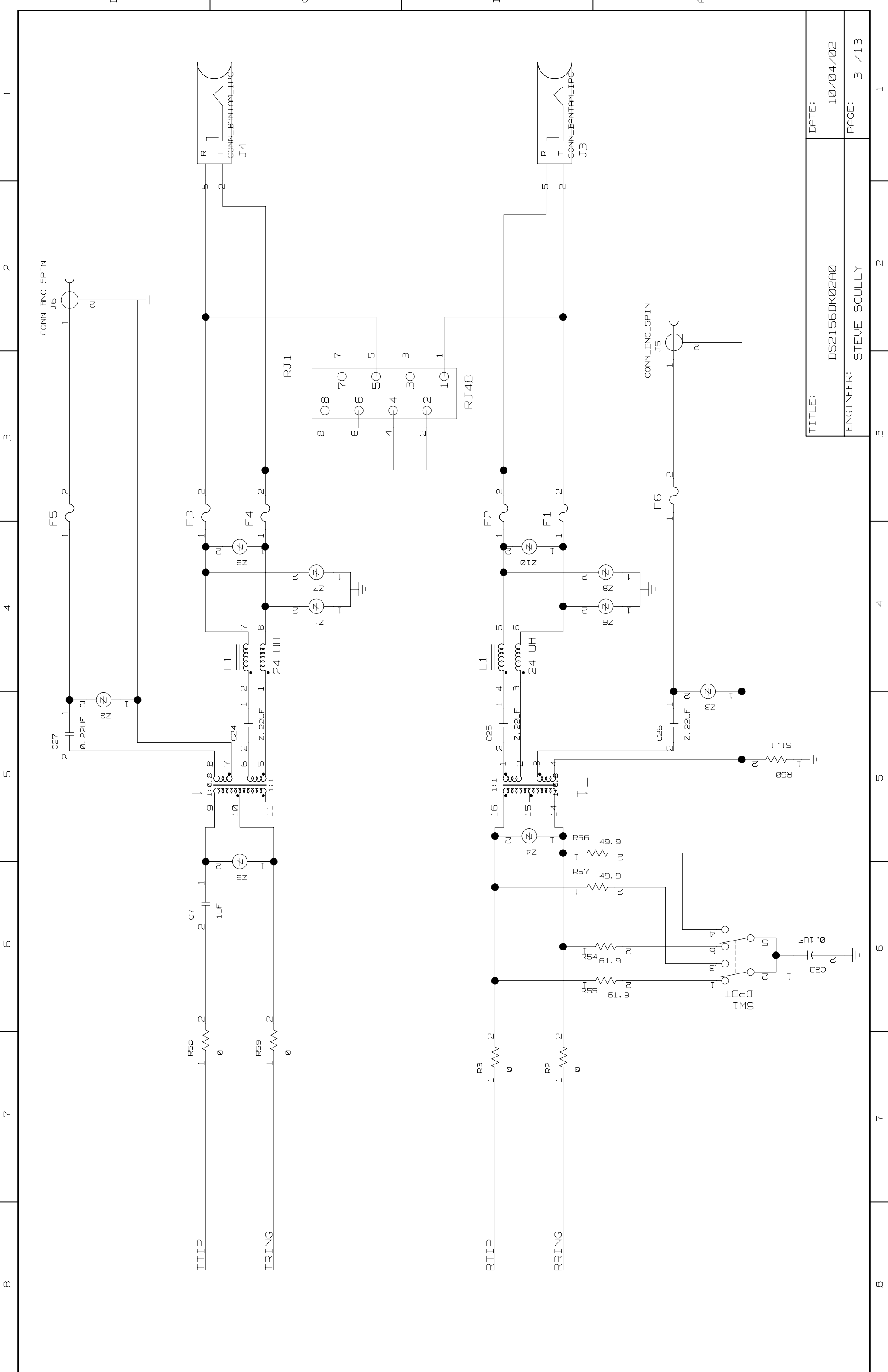
U11

- RTIP 16
- RRING 17
- RPOSI 86
- RNEGI 87
- RCLKI 88
- RPOSO 91
- RNEGO 90
- RCLKO 89
- 8XCLK 13
- RCL 6
- LIUC 12
- TTIP 29
- TRING 32
- TPOSI 38
- TNEGI 39
- TCLKI 40
- TPOSO 43
- TNEGO 42
- TCLKO 41
- JTMS 2
- JTRST 5
- JTDI 7
- JTCLK 4
- JTDO 10

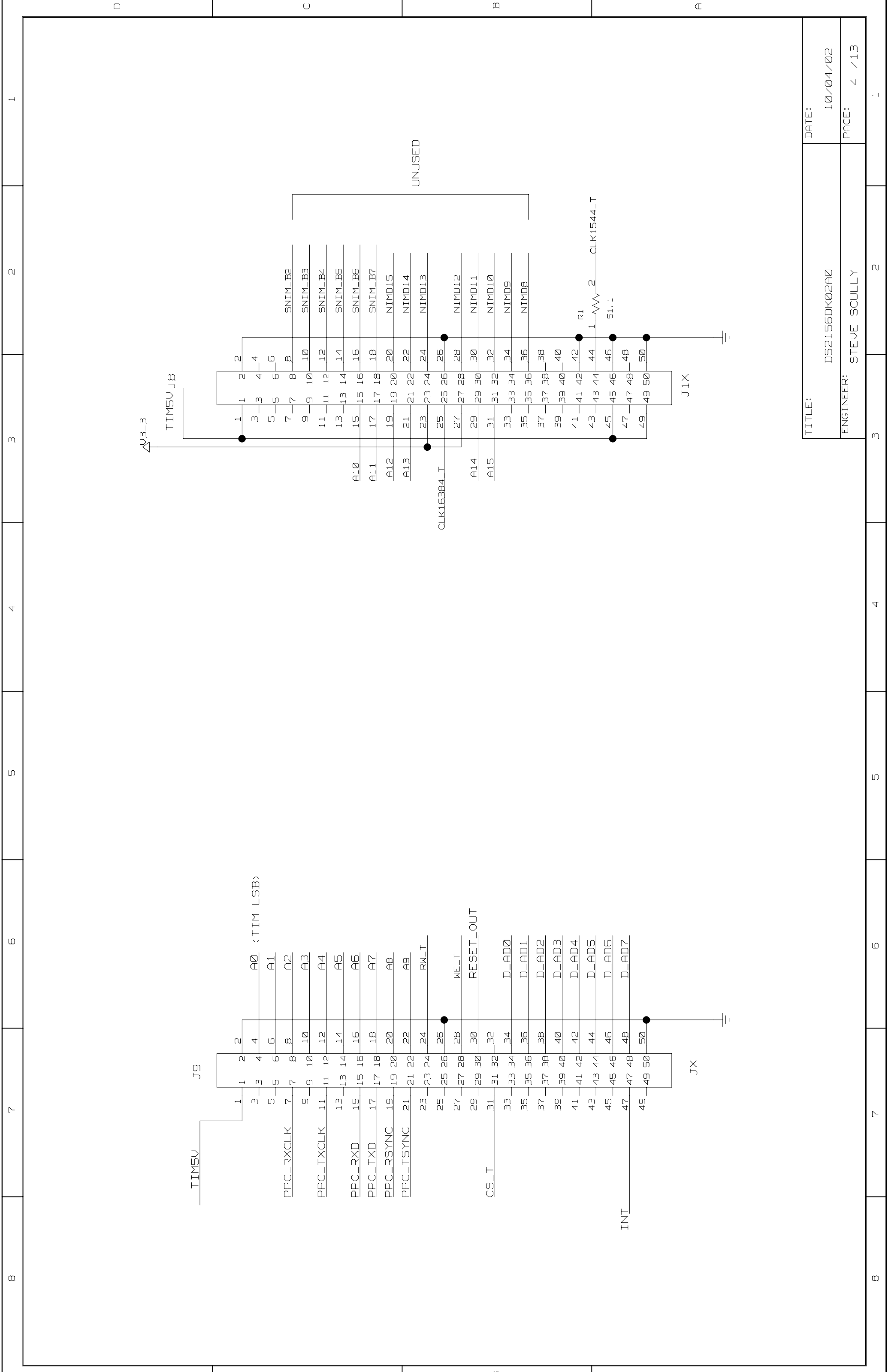


DS2156  
TQFP

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ENGINEER:	STEVE SCULLY	PAGE:	2 / 13



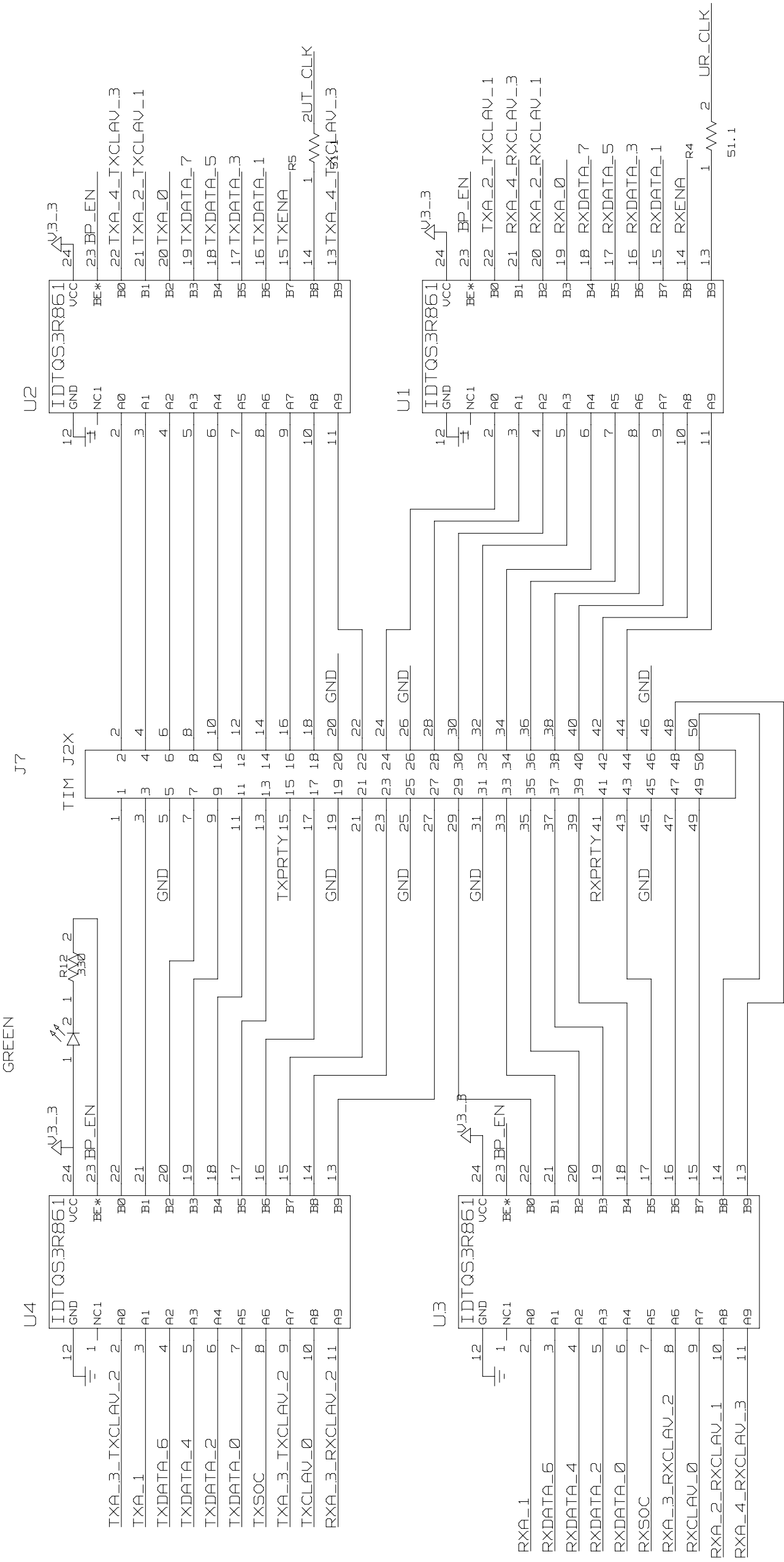
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ENGINEER:	STEVE SCULLY
DATE:	10/04/02
PAGE:	3 / 13



TITLE:	DS2156DK02A0	DATE:	10/04/02
ENGINEER:	STEVE SCULLY	PAGE:	4 / 13



DS4  
GREEN



BP\_EN IS BIT MAPPED TO  
PLD ADDRESS 0X15 BIT 2  
LOGIC 0 CLOSSES SWITCHES

TITLE:	DS2156DK02A0	DATE:	10/04/02
ENGINEER:	STEVE SCULLY	PAGE:	6 / 13

J1

CONN\_50P1

TXDATA_0	1	2	TXDATA_1
TXDATA_2	3	4	TXDATA_3
GND	5	6	TXDATA_4
TXDATA_5	7	8	TXDATA_6
TXDATA_7	9	10	GND
	11	12	
	13	14	
	15	16	
	17	18	
	19	20	GND
	21	22	TXSOC
TXADDR0	23	24	TXADDR1
GND	25	26	TXADDR2
TXADDR3	27	28	TXADDR4
TXCLAV0	29	30	GND
	31	32	
	33	34	TXENABLE
	35	36	R14 2 LUT_CLK
	37	38	
	39	40	
	41	42	
	43	44	
	45	46	
	47	48	
	49	50	

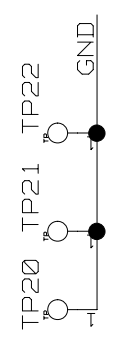
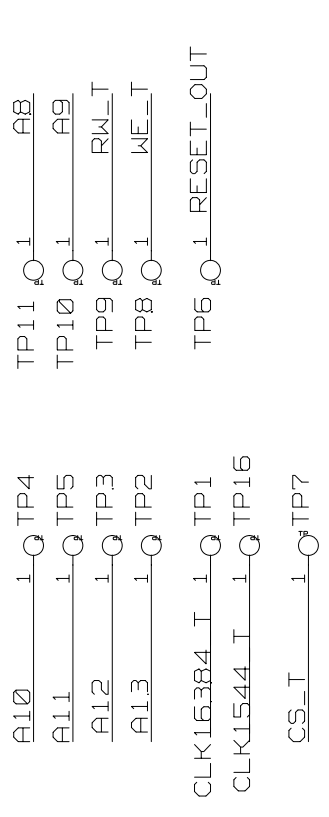
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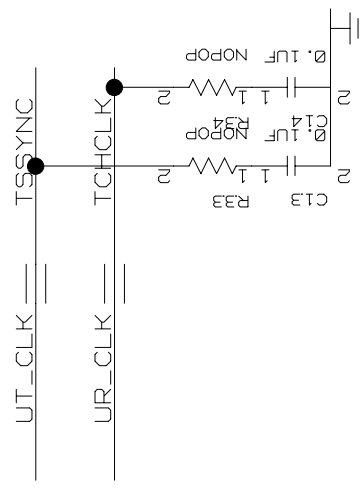
J2

CONN\_50P1

RXDATA_0	1	2	RXDATA_1
RXDATA_2	3	4	RXDATA_3
GND	5	6	RXDATA_4
RXDATA_5	7	8	RXDATA_6
RXDATA_7	9	10	GND
	11	12	
	13	14	
	15	16	
	17	18	
	19	20	GND
	21	22	RXSOC
	23	24	
	25	26	
	27	28	
	29	30	
	31	32	
	33	34	
	35	36	
RXADDR0	37	38	RXADDR1
RXADDR2	39	40	GND
RXADDR3	41	42	RXADDR4
RXCLAV0	43	44	
GND	45	46	
	47	48	RXENB
UR_CLK_1	49	50	

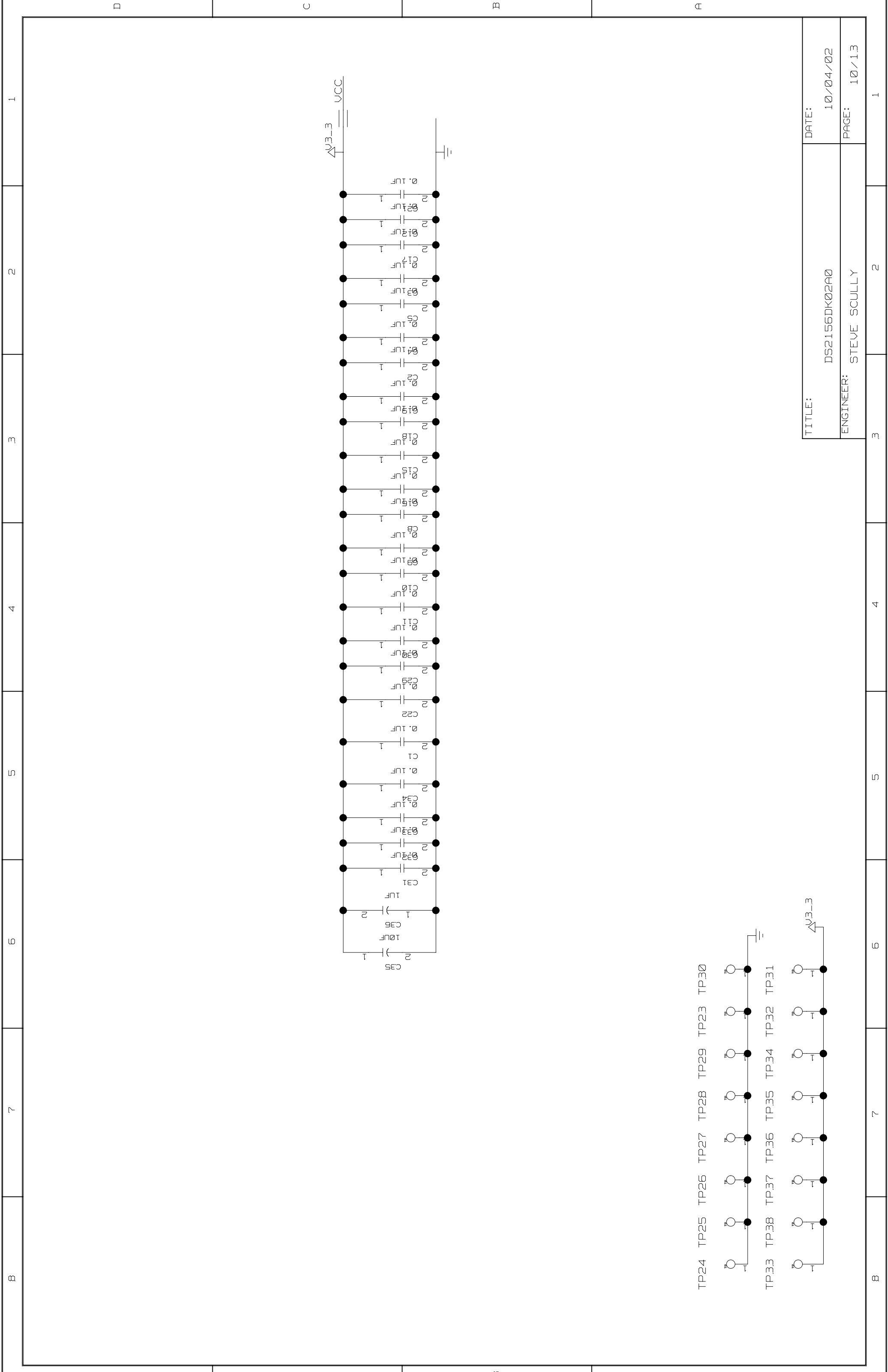
ADTECH RX



8	7	6	5	4	3	2	1
D	D	C	B	A			
RXADDR0 == RXA_0 == UR_ADDR0 == RCHCLK == RXADDR1 == RXA_1 == UR_ADDR1 == RSIGF == RXADDR2 == RXA_2_RXCLAV_1 == UR_ADDR2 == RSIG == RXADDR3 == RXA_3_RXCLAV_2 == UR_ADDR3 == RMSYNC == RXADDR4 == RXA_4_RXCLAV_3 == UR_ADDR4 == RFSYNC == RXCLAV0 == RXCLAV_0 == UR_CLAV == RSER == RXDATA_0 == RXDATA_0 == UR_DATA0 == RLINK == RXDATA_1 == RXDATA_1 == UR_DATA1 == RLCLK == RXDATA_2 == RXDATA_2 == UR_DATA2 == RPOSI == RXDATA_3 == RXDATA_3 == UR_DATA3 == RNEGI == RXDATA_4 == RXDATA_4 == UR_DATA4 == RCLKI == RXDATA_5 == RXDATA_5 == UR_DATA5 == RCLKO == RXDATA_6 == RXDATA_6 == UR_DATA6 == RNEGO == RXDATA_7 == RXDATA_7 == UR_DATA7 == RPOSO ==	RXENB == RXENA == UR_ENB == BPCLK == RXSOC == RXSOC == UR_SOC == RCHBLK == TXADDR0 == TXA_0 == UT_ADDR0 == UOP3 == TXADDR1 == TXA_1 == UT_ADDR1 == TCHBLK == TXADDR2 == TXA_2_TXCLAV_1 == UT_ADDR2 == TLCLK == TXADDR3 == TXA_3_TXCLAV_2 == UT_ADDR3 == TLINK == TXADDR4 == TXA_4_TXCLAV_3 == UT_ADDR4 == TPOSI == TXCLAV0 == UT_CLAV == TXCLAV_0 == LIUC == TXDATA_0 == TXDATA_0 == UT_DATA0 == TNEGI == TXDATA_1 == TXDATA_1 == UT_DATA1 == TCLKI == TXDATA_2 == TXDATA_2 == UT_DATA2 == TCLKO == TXDATA_3 == TXDATA_3 == UT_DATA3 == TNEGO == TXDATA_4 == TXDATA_4 == UT_DATA4 == TPOSO == TXDATA_5 == TXDATA_5 == UT_DATA5 == TSEI ==	TXDATA_6 == TXDATA_6 == UT_DATA6 == TSIG == TXDATA_7 == TXDATA_7 == UT_DATA7 == TSYSCLK == TXENABLE == TXENA == UT_ENB == UOP1 == TXSOC == TXSOC == UT_SOC == UOP0 ==	UT_CLK == TSSYNC UR_CLK == TCHCLK 				
D	C	B	A				
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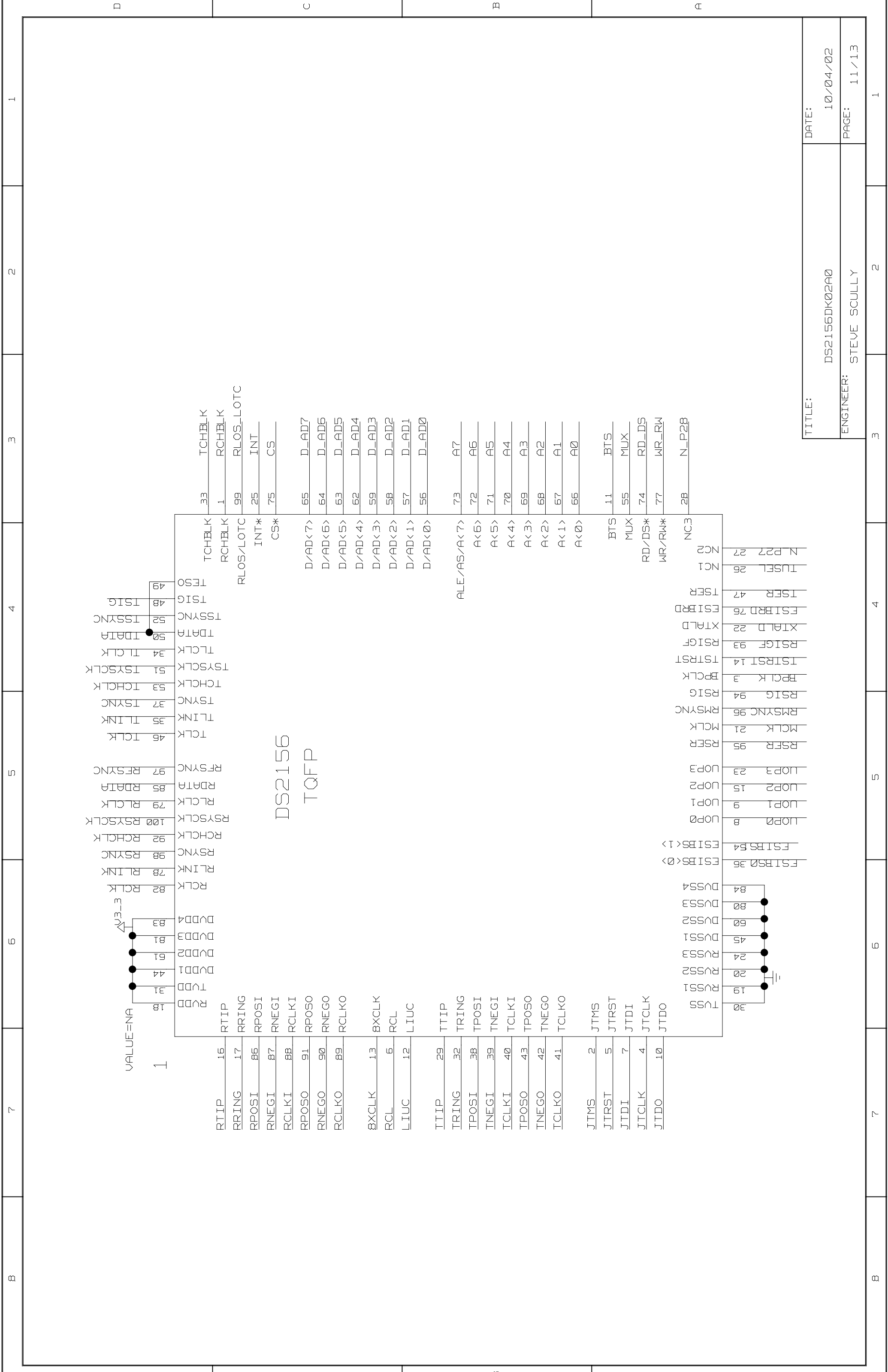






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ENGINEER:	STEVE SCULLY
PAGE:	10/13

TP24 TP25 TP26 TP27 TP28 TP29 TP30 TP23 TP30  
 TP33 TP38 TP37 TP36 TP35 TP34 TP32 TP31  
 TP31 TP32 TP33 TP34 TP35 TP36 TP37 TP38



TITLE: DS2156DK02A0  
 DATE: 10/04/02  
 ENGINEER: STEVE SCULLY  
 PAGE: 11/13

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*** Signal Cross-Reference for the entire design ***
BXCLK      2CB<> 11C7>
A0         4C6<> 5C4<> 2B3<> 11B3<>
A1         4C6<> 5C4<> 2B3<> 11B3<>
A2         4C6<> 5C4<> 2B3<> 11B3<>
A3         4C6<> 5C4<> 2B3<> 11B3<>
A4         4C6<> 5C4<> 2B3<> 11B3<>
A5         4C6<> 5C4<> 2B3<> 11B3<>
A6         4C6<> 5C4<> 2B3<> 11B3<>
A7         4C6<> 5C4<> 2B3<> 11B3<>
A8         4B6<> 7B1<>
A9         4B6<> 7B1<>
A10        4C3<> 7C3<>
A11        4C3<> 5C1<> 7C3<>
A12        4C3<> 5C1<> 7B3<>
A13        4B3<> 7B3<>
A14        4B3<>
A15        4B3<>
BPCLK      2A5<> BD4<> 11A4>
BP_EN      5C1<> 6B2<> 6B6<> 6C2<> 6C6<>
BTS        5D4<> 2B3<> 5A6<> 11A3<>
CLK1544_T  7B3<> 9DB<> 4B2<>
CLK204B    5D3<> 9B3<> 9B8<>
CLK163B4_T 4B4<> 5D3<> 7B3<>
CS         5B4<> 2C3<> 11C3<>
CS_T       4B8<> 5B1<> 7B3<>
D_AD0      2B3<> 4B6<> 5C1<> 11B3<>
D_AD1      2C3<> 4B6<> 5C1<> 11B3<>
D_AD2      2C3<> 4B6<> 5C1<> 11C3<>
D_AD3      2C3<> 4B6<> 5C1<> 11C3<>
D_AD4      2C3<> 4B6<> 5C1<> 11C3<>
D_AD5      2C3<> 4B6<> 5C1<> 11C3<>
D_AD6      2C3<> 4A6<> 5C1<> 11C3<>
D_AD7      2C3<> 4A6<> 5D1<> 11C3<>
ESIBR0     2A5<> 11A4<> 5A8<>
ESIBS0     2A6<> 11A6<>
ESIBS1     2A6<> 11A5<>
INT         2C3<> 4A8<> 5A2<> 11C3> 5A6<>
INT_INDICATOR
JTCLK      2A8<> 11A7<>
JTDI       2A8<> 11A7<>
JTDO       2A8<> 11A7>
JTMS       2B8<> 11B7<>
JTRST      2B8<> 5A8<> 11A7<>
LIUC       B84> 2CB<> 5A6<> 11B7<>
MCLK       9B6<> 9C6<> 2A5<> 11A5<>
MUX        5C4<> 2A3<> 5A8<> 11A3<>
NIMDB      4B2<>
NIMD0      4B2<>
NIMD10     4B2<>
NIMD11     4B2<>
NIMD12     4B2<>
NIMD13     4B2<>
NIMD14     4B2<>
NIMD15     4C2<>
NLP27      2A4<> 11A4<>
NLP28      2A3<> 11A3<>
PPC_RSXCLK 4C8<> 9A4<>
PPC_RXCLK  4C8<> 9A4<>
PPC_RXD    4C8<> 9A4<>
PPC_TDMLEN 5C1<> 9A4<>
PPC_TSYNC  4B8<> 9A4<>
PPC_TXCLK  4C8<> 9A4<>
PPC_TXD    4C8<> 9A4<>
RCHCLK     2C3> BD4> 11C3>
RCHCLK     2D6> BD7> 11D5>
RCL        2CB> 11C7>
RCLK       2D6> 9A6<> 9C1<> 9C1<> 9D1<> 11D6>
RCLKI      B87> 2CB<> 5A8<> 11C7<>
RCLKO      2CB> B87> 11C7>
RDATA      2D6> 11D5>
RD_DS      5C4<> 2A3<> 11A3<>
RESET_OUT  4B6<> 5B1<> 7B1<>
RFSYNC     2D6> BC7> 11D5>
RLCLK      2D6> B87> 11D5>

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RLINK      2D6> B87> 11D6>
RLOS_LOTC  2C3> 5B2<> 11C3>
RLOS_LOTC_INDICATOR 5A2<>
RMSYNCR    2A5> BC7> 11A5>
RNEGI      B87> 2CB<> 5A8<> 11C7<>
RNEGO      2CB> B87> 11C7>
RPOSI      B87> 2CB<> 5A8<> 11C7<>
RPOSO      2CB> B87> 11C7>
RRING      2CB<> 3B8<> 11C7<>
RSEI       2A5> BC7> 9A6<> 9B3<> 11A5>
RSIG       2A5> BD7> 11A5>
RSIGF      2A5> BD7> 11A4>
RSYNCR     2D6<> 9A6<> 9B3<> 9C1<> 11D5<>
          5A6<>
RSYSCLK    9B6<> 9C3<> 9D6<> 2D6<> 5A8<> 11D5<>
RTIP       2CB<> 3B8<> 11C7<>
RWLT       4B6<> 5B1<> 7B1<>
RXADDR0    7B8<> 8D8
RXADDR1    7B8<> 8D8
RXADDR2    7B8<> 8D8
RXADDR3    7B8<> 8D8
RXADDR4    7B6<> 8CB
RXA_0      6B2<> 8D7>
RXA_1      6B7<> 8D7>
RXA_2_RXCLAVL_1 6A7<> 6B2<> 8D7>
RXA_3_RXCLAVL_2 6A7<> 6C7<> 8C7>
RXA_4_RXCLAVL_3 6A7<> 6B2<> 8C7>
RXCLAVL0   7A8<> 8CB
RXCLAVL_0  6A7<> 8C7>
RXDATA_0   6B7<> 7C8<> 8B7> 8B8
RXDATA_1   6A2<> 7C6<> 8B7> 8B8
RXDATA_2   6B7<> 7C8<> 8B7> 8B8
RXDATA_3   6B2<> 7C6<> 8B7> 8B8
RXDATA_4   6B7<> 7C6<> 8A7> 8A8
RXDATA_5   6B2<> 7C8<> 8A7> 8A8
RXDATA_6   6B7<> 7C6<> 8A7> 8A8
RXDATA_7   6B2<> 7C8<> 8A7> 8A8
RXENAR     6A2<> 8D4>
RXENBR     7A6<> 8D5
RXPRTY     6B5<>
RXSOC      6B7<> 7B6<> 8D4> 8D5
SNIM_B2    4C2<>
SNIM_B3    4C2<>
SNIM_B4    4C2<>
SNIM_B5    4C2<>
SNIM_B6    4C2<>
SNIM_B7    4C2<>
SW1_B0EN   5A4<> 9D8<>
SW1_B1EN   5A4<> 9D8<>
SW1_B2EN   5A3<> 9D6<>
SW1_B3EN   5A3<> 9D6<>
SW2_B0EN   5A3<> 9B8<>
SW2_B1EN   5A3<> 9B8<>
SW2_B2EN   5A3<> 9B6<>
SW2_B3EN   5A3<> 9B6<>
SW3_B0EN   5A3<> 9D3<>
SW3_B1EN   5A3<> 9D1<>
SW3_B2EN   5A3<> 9D1<>
SW3_B3EN   5A3<> 9D1<>
SW4_B0EN   5B4<> 9B3<>
SW4_B1EN   5B4<> 9B3<>
SW4_B2EN   5B4<> 9B2<>
SW4_B3EN   5B4<> 9B2<>
TCHCLK     2D3> BC4> 11C3>
TCHCLK     2D5> 11D4> 8A1<>
TCK        5B8<> 5D8<>
TCLK       9A6<> 9B6<> 9C3<> 9C6<> 2D5<> 5A6<>
          11D5<>
TCLKI      B84> 2B8<> 5A8<> 11B7<>
TCLKO      2B8> B84> 11B7>
TDATA      2D5<> 11D4<>
TDI        5B8<> 5D7<>
TDO        5B8<> 5C7<>
TIMSV      4D3<> 4D8<>
TLCLK      2D5> BC4> 11D4>
TLINK      BC4> 2D5<> 5B6<> 11D5<>
TMS        5B8<> 5C7<>

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TNEGI      B84> 2B8<> 5A8<> 11B7<>
TNEGO      2B8> B84> 11B7>
TPOSI      8C4> 2B8<> 5A8<> 11B7<>
TPOSO      2B8> B84> 11B7>
TRING      2B8> 11B7> 3CB<>
TRSER      B84> 9A6<> 9B2<> 2A5<> 5A8<> 11A4<>
TSIG       B01> 2D5<> 5B6<> 11D4<>
TSSYNCR    9C3<> 2D5<> 5B6<> 8A1<> 11D4<>
TSTRST     2A5<> 5A8<> 11A4<>
TSYNCR     2D5<> 9A6<> 9B2<> 11D5<> 5A6<>
TSYSCLK    B01> 9B6<> 9D3<> 9D6<> 2D5<> 5A8<>
          11D4<>
TTIP       2B8> 11B7> 3CB<>
TUSEL      5D2<> 2A4<> 11A4<>
TXADDR0    7B5<> 8D5
TXADDR1    7B4<> 8C5
TXADDR2    7B4<> 8C5
TXADDR3    7B5<> 8C5
TXADDR4    7B4<> 8C5
TXA_0      6C2<> 8D4>
TXA_1      6C7<> 8C4>
TXA_2_TXCLAVL_1 6B2<> 6C2<> 8C4>
TXA_3_TXCLAVL_2 6C7<> 6C7<> 8C4>
TXA_4_TXCLAVL_3 6C2<> 6C2<> 8C4>
TXCLAVL0   7B5<> 8B5
TXCLAVL_0  6C7<> 8B5
TXDATA_0   6C7<> 7C5<> 8B4> 8B5
TXDATA_1   6C2<> 7C4<> 8B4> 8B5
TXDATA_2   6C7<> 7C5<> 8A4> 8A5
TXDATA_3   6C2<> 7C4<> 8A4> 8A5
TXDATA_4   6C7<> 7C4<> 8A4> 8A5
TXDATA_5   6C2<> 7C5<> 8A4> 8A5
TXDATA_6   6C7<> 7C4<> 8D1> 8D2
TXDATA_7   6C2<> 7C5<> 8D1> 8D2
TXENAR     6C2<> 8C1>
TXENABLE   7B4<> 8C2
TXPRTY     6C5<>
TXSOC      6C7<> 7B4<> 8B1> 8B2
UOP0       2A6> 8B1> 11A5>
UOP1       2A6> 8C1> 11A5>
UOP2       2A6> 11A5>
UOP3       2A6> 8D4> 11A5>
UR_ADDR0    B8B
UR_ADDR1    B8B
UR_ADDR2    B8B
UR_ADDR3    B8B
UR_ADDR4    B8B
UR_CLAV    B8B
UR_CLK     9B2<> 6A1<> 7A8<> 8A2<>
UR_DATA0    B8B
UR_DATA1    B8B
UR_DATA2    B8B
UR_DATA3    B8B
UR_DATA4    B8B
UR_DATA5    B8B
UR_DATA6    B8B
UR_DATA7    B8B
UR_ENB     B8B
UR_SOC     B8B
UR_ADDR0    B8B
UR_ADDR1    B8B
UR_ADDR2    B8B
UR_ADDR3    B8B
UR_ADDR4    B8B
UR_CLAV    B8B
UR_CLK     9B2<> 6C1<> 7B4<> 8A2<>
UT_DATA0    B8B
UT_DATA1    B8B
UT_DATA2    B8B
UT_DATA3    B8B
UT_DATA4    B8B
UT_DATA5    B8B
UT_DATA6    B8B
UT_DATA7    B8B
UT_ENB     B8B
UT_SOC     B8B
WE_T       4B5<> 5B1<> 7B1<>

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WR_LRA
XTALD      5C4<> 2A3<> 11A3<>
          2A5> 11A4>

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\*\*\* Part Cross-Reference for the entire design \*\*\*

1	DS2156_TQFP 11D7
C1	CAP 10B5
C2	CAP 10B3
C3	CAP 10B2
C4	CAP 10B2
C5	CAP 10B2
C7	CAP 3D6
C8	CAP 10B4
C9	CAP 10B4
C10	CAP 10B4
C11	CAP 10B4
C12	CAP 10B2
C13	CAP 8A1
C14	CAP 8A1
C15	CAP 10B3
C16	CAP 10B3
C17	CAP 10B2
C18	CAP 10B3
C19	CAP 10B3
C21	CAP 10B2
C22	CAP 10B5
C23	CAP 3A6
C24	CAP 3C5
C25	CAP 3B5
C26	CAP 3A5
C27	CAP 3D5
C29	CAP 10B4
C30	CAP 10B4
C31	CAP 10B6
C32	CAP 10B5
C33	CAP 10B5
C34	CAP 10B5
C35	CAP 10B5
C36	CAP 10B6
DS1	LED 9B4
DS2	LED 5A2
DS3	LED 5A2
DS4	LED 6D5
DS5	LED 5A3
DS6	LED 5A4
DS7	LED 5A3
DS8	LED 5A4
DS9	LED 5A4
DS10	LED 5A3
DS11	LED 5A4
DS12	LED 5A3
DS13	LED 5A3
DS14	LED 5A3
DS15	LED 5A3
DS16	LED 5B5
DS17	LED 5B5
DS18	LED 5A3
F1	FUSE 3B4
F2	FUSE 3B4
F3	FUSE 3D4
F4	FUSE 3C4
F5	FUSE 3D4
F6	FUSE 3A3
J1	CONN_50P1 7D5
J2	CONN_50P1 7D7
J3	CONN_BANTAM_IPC 3B1
J4	CONN_BANTAM_IPC 3C1
J5	CONN_BNC_SPIN 3A3
J6	CONN_BNC_SPIN 3D2
J7	CONN_50P2 6D4
J8	CONN_50P2 4D3
J9	CONN_50P2 4D7
JT10	CONN_10P 5CB
L1	CHOKE_DUAL-T1 3B4 3C4
R1	RES1 4B2
R2	RES 3B7
R3	RES 3B7
R4	RES 6A2
R5	RES 6C2
R6	RES1 5A7

R7	RES 9B4
R8	RES1 5A2
R9	RES1 5A7
R10	RES1 5A7
R11	RES1 5A2
R12	RES 6D5
R13	RES1 5B6
R14	RES1 7B4
R15	RES1 5B6
R16	RES1 5A7
R17	RES1 5B6
R18	RES1 5A6
R19	RES1 5A6
R21	RES1 7A8
R22	RES1 5A7
R23	RES1 5A7
R24	RES1 5B8
R25	RES1 5D7
R26	RES1 5D8
R27	RES1 5D8
R29	RES1 5A6
R30	RES 5A3
R31	RES 5A3
R32	RES1 5A6
R33	RES1 8A1
R34	RES1 8A1
R35	RES 5A3
R36	RES 5A3
R37	RES1 5A6
R39	RES 5A3
R40	RES 5A4
R41	RES 5A3
R42	RES 5A4
R43	RES 5A3
R44	RES1 5A7
R45	RES 5A3
R46	RES1 5B7
R47	RES1 5A7
R49	RES1 5A6
R50	RES 5A3
R51	RES 5B4
R52	RES 5B4
R53	RES 5A3
R54	RES1 3B6
R55	RES1 3B6
R56	RES 3B5
R57	RES 3B6
R58	RES 3D7
R59	RES 3C7
R60	RES 3A5
R61	RES1 5A7
RJ1	RJ4B_CON 3C3
SW1	SWITCH_DPDT_SLIDE_6P 3A6
T1	XFMR_2IN_4OUT_U 3B5 3D5
TP1	TSTPNT_SNG 7B2
TP2	TSTPNT_SNG 7B2
TP3	TSTPNT_SNG 7B2
TP4	TSTPNT_SNG 7C2
TP5	TSTPNT_SNG 7C2
TP6	TSTPNT_SNG 7B2
TP7	TSTPNT_SNG 7B2
TP8	TSTPNT_SNG 7B2
TP9	TSTPNT_SNG 7B2
TP10	TSTPNT_SNG 7B2
TP11	TSTPNT_SNG 7B2
TP12	TSTPNT_SNG 5D2
TP13	TSTPNT_SNG 5D2
TP14	TSTPNT_SNG 5A6
TP15	TSTPNT_SNG 5A6
TP16	TSTPNT_SNG 7B2
TP17	TSTPNT_SNG 5D2
TP18	TSTPNT_SNG 5A6
TP20	TSTPNT_SNG 7B2
TP21	TSTPNT_SNG 7B1

TP22	TSTPNT_SNG 7B1
TP23	TSTPNT_SNG 10A7
TP24	TSTPNT_SNG 10A8
TP25	TSTPNT_SNG 10A7
TP26	TSTPNT_SNG 10A7
TP27	TSTPNT_SNG 10A7
TP28	TSTPNT_SNG 10A7
TP29	TSTPNT_SNG 10A7
TP30	TSTPNT_SNG 10A7
TP31	TSTPNT_SNG 10A4
TP32	TSTPNT_SNG 10A4
TP33	TSTPNT_SNG 10A5
TP34	TSTPNT_SNG 10A5
TP35	TSTPNT_SNG 10A5
TP36	TSTPNT_SNG 10A5
TP37	TSTPNT_SNG 10A5
TP38	TSTPNT_SNG 10A5
U1	IDT053R861_U 6B3
U2	IDT053R861_U 6D3
U3	IDT053R861_U 6B6
U4	IDT053R861_U 6D6
U5	XILINX_XC9572XL 5D4 5D7
U6	IDT053R861_U 9B5
U7	IDT053125_U 9D3
U8	IDT053125_U 9D7
U9	IDT053125_U 9B3
U10	IDT053125_U 9B7
U11	DS2156_TQFP 2D7
Z1	SIDACTOR_2 3C4
Z2	SIDACTOR_2 3D5
Z3	SIDACTOR_2 3A5
Z4	SIDACTOR_2 3B5
Z5	SIDACTOR_2 3C6
Z6	SIDACTOR_2 3A4
Z7	SIDACTOR_2 3C4
Z8	SIDACTOR_2 3A4
Z9	SIDACTOR_2 3C4
Z10	SIDACTOR_2 3B4