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# FDMC86012

## N-Channel Power Trench® MOSFET

### 30 V, 88 A, 2.7 mΩ

#### Features

- Max  $r_{DS(on)}$  = 2.7 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 23$  A
- Max  $r_{DS(on)}$  = 4.7 mΩ at  $V_{GS} = 2.5$  V,  $I_D = 17.5$  A
- High performance technology for extremely low  $r_{DS(on)}$
- Termination is Lead-free
- 100% UIL Tested
- RoHS Compliant

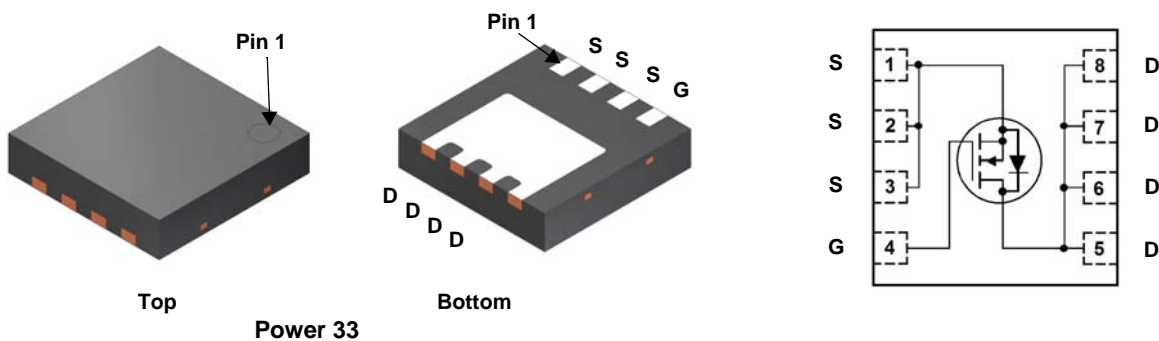


#### General Description

This device has been designed specifically to improve the efficiency of DC/DC converters. Using new techniques in MOSFET construction, the various components of gate charge and capacitance have been optimized to reduce switching losses. Low gate resistance and very low Miller charge enable excellent performance with both adaptive and fixed dead time gate drive circuits. Very low  $r_{DS(on)}$  has been maintained to provide a sub logic-level device.

#### Applications

- 3.3 V input synchronous buck switch
- Synchronous rectifier



#### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	±12	V
$I_D$	Drain Current -Continuous	$T_C = 25$ °C	A
	-Continuous	$T_A = 25$ °C (Note 1a)	
	-Pulsed	(Note 4)	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	mJ
$P_D$	Power Dissipation	$T_C = 25$ °C	W
	Power Dissipation	$T_A = 25$ °C (Note 1a)	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

#### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	2.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86012	FDMC86012	Power33	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		43		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12\ \text{V}, V_{DS} = 0\ \text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	0.8	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-4		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 4.5\ \text{V}, I_D = 23\ \text{A}$		2.2	2.7	m $\Omega$
		$V_{GS} = 2.5\ \text{V}, I_D = 17.5\ \text{A}$		3.4	4.7	
		$V_{GS} = 4.5\ \text{V}, I_D = 23\ \text{A}, T_J = 125\text{ }^\circ\text{C}$		3.5	4.3	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\ \text{V}, I_D = 23\ \text{A}$		144		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$		3625	5075	pF
$C_{oss}$	Output Capacitance			1230	1725	pF
$C_{rss}$	Reverse Transfer Capacitance			185	260	pF
$R_g$	Gate Resistance		0.1	0.9	3.0	$\Omega$

### Switching Characteristics

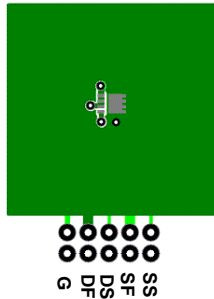
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\ \text{V}, I_D = 23\ \text{A}, V_{GS} = 4.5\ \text{V}, R_{GEN} = 6\ \Omega$		20	32	ns	
$t_r$	Rise Time			11	20	ns	
$t_{d(off)}$	Turn-Off Delay Time			43	69	ns	
$t_f$	Fall Time			8	16	ns	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\ \text{V to } 4.5\ \text{V}$		27	38	nC
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\ \text{V to } 2.5\ \text{V}$		16	23	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 15\ \text{V}, I_D = 23\ \text{A}$		5.8		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge			5.4		nC	

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 23\ \text{A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\ \text{V}, I_S = 1.9\ \text{A}$ (Note 2)		0.7	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 23\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		40	64	ns
$Q_{rr}$	Reverse Recovery Charge			23	37	nC

#### Notes:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\ \text{in}^2$  pad of 2 oz copper pad on a  $1.5 \times 1.5\ \text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $53\text{ }^\circ\text{C/W}$  when mounted on a  $1\ \text{in}^2$  pad of 2 oz copper



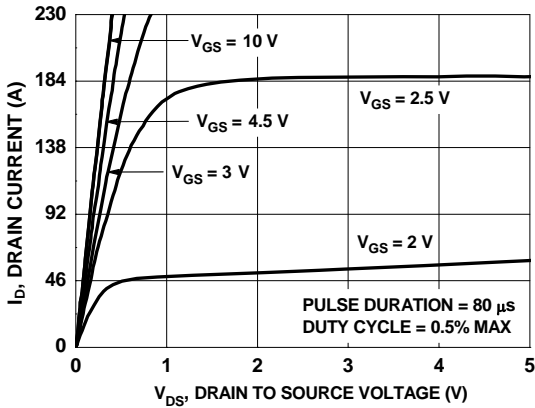
b.  $125\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width <  $300\ \mu\text{s}$ , Duty cycle < 2.0%.

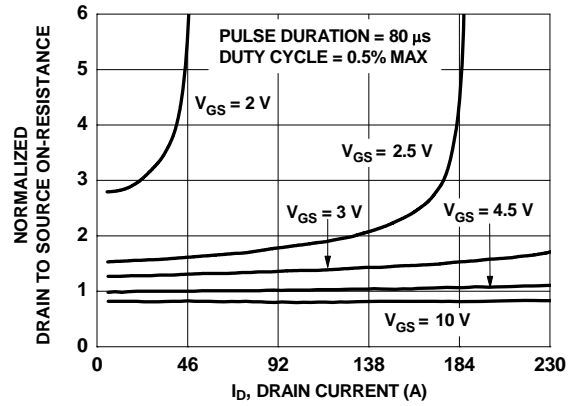
- EAS of 337 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ; N-ch: L = 3 mH, IAS = 15 A, VDD = 30 V, VGS = 10 V. 100% test at L = 0.3 mH, IAS = 33 A.

- Pulsed Id limited by junction temperature,  $t_d \leq 100\ \mu\text{s}$ , please refer to SOA curve for more details.

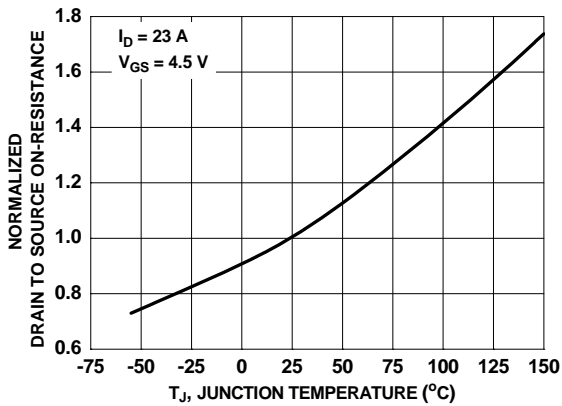
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



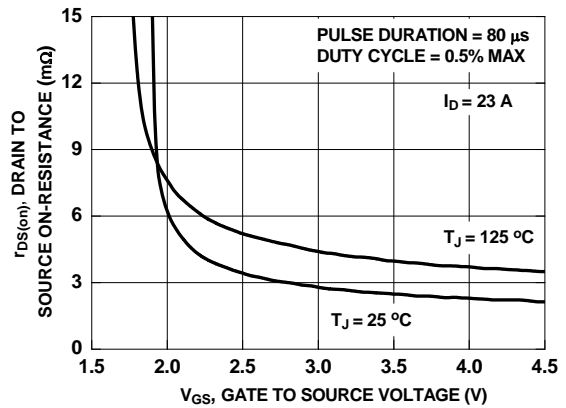
**Figure 1. On-Region Characteristics**



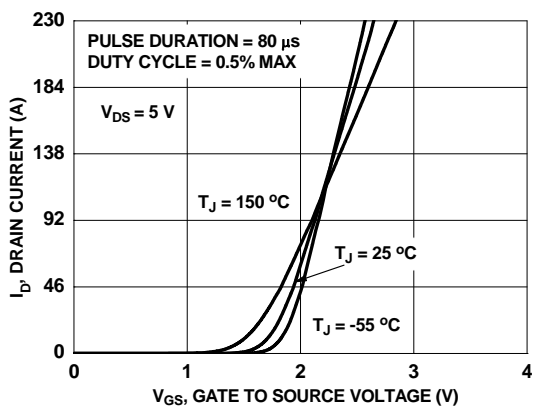
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



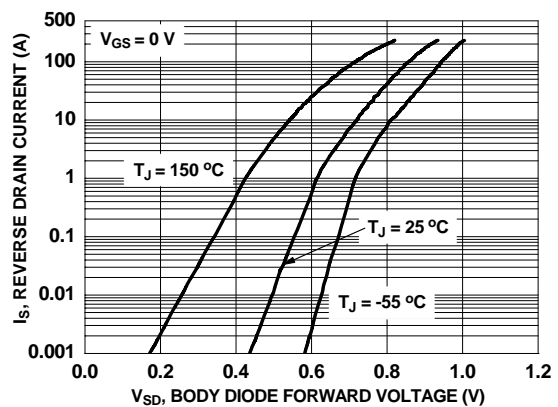
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

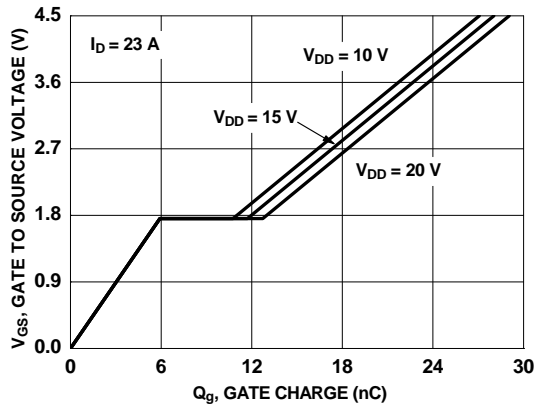


**Figure 5. Transfer Characteristics**

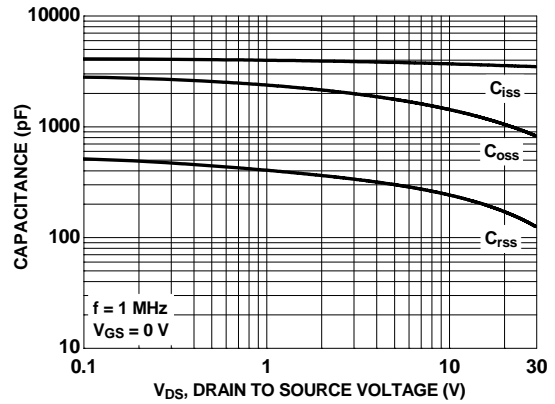


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

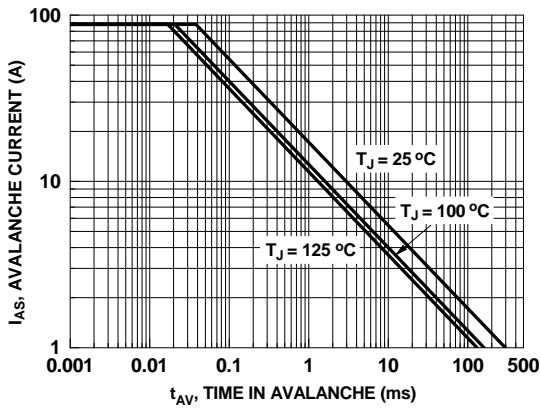
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



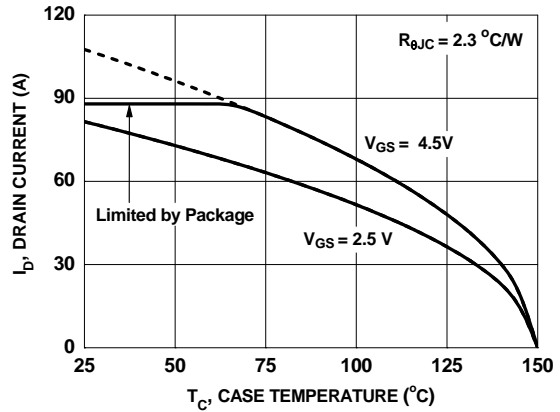
**Figure 7. Gate Charge Characteristics**



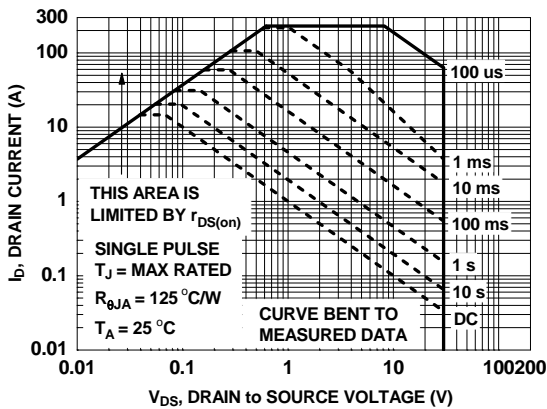
**Figure 8. Capacitance vs Drain to Source Voltage**



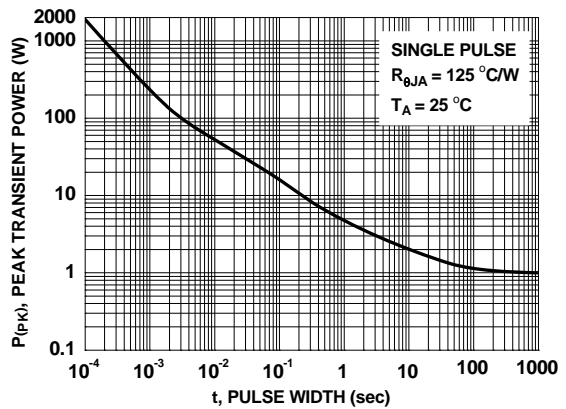
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

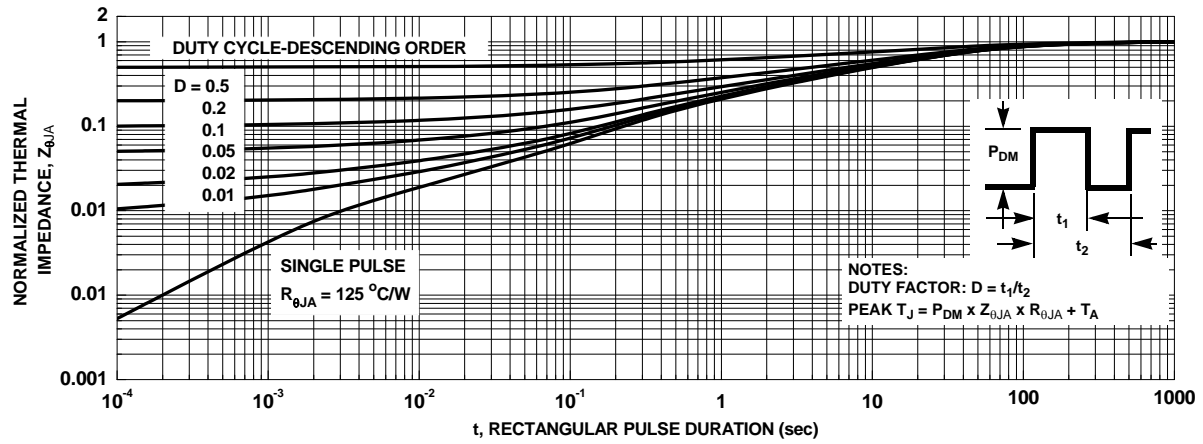


**Figure 11. Forward Bias Safe Operating Area**



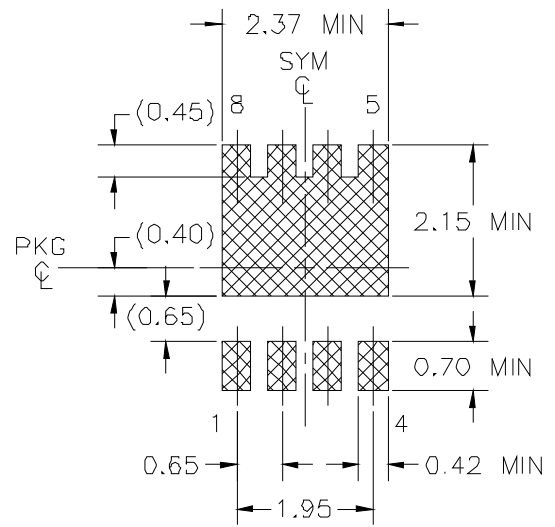
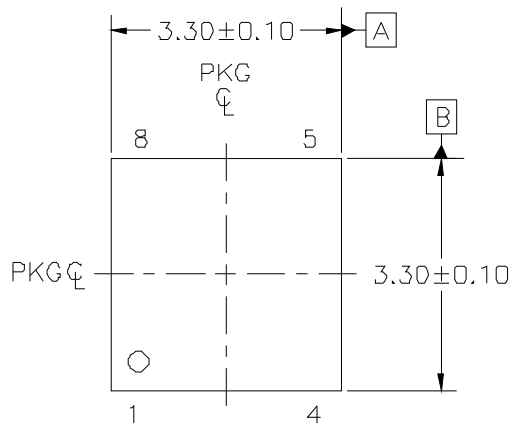
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

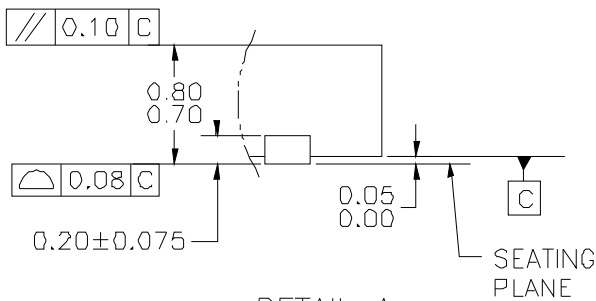
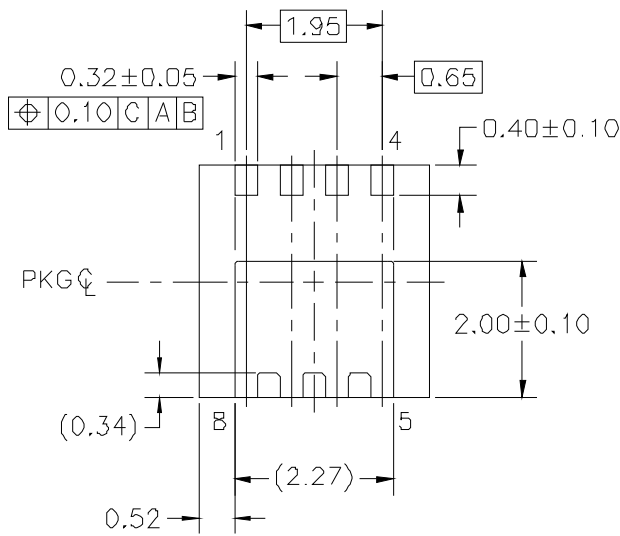
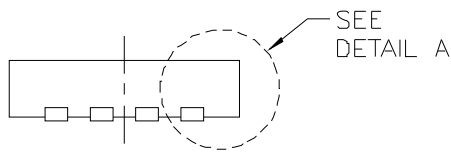


**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

### Dimensional Outline and Pad Layout



LAND PATTERN RECOMMENDATION



DETAIL A  
SCALE: 2X




NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.



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