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December 2015

# FCP650N80Z

## N-Channel SuperFET<sup>®</sup> II MOSFET

800 V, 10 A, 650 mΩ



### Features

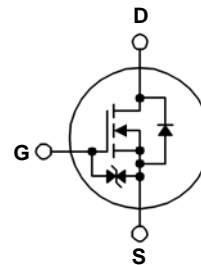
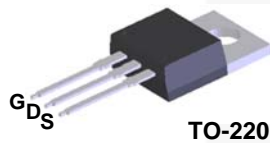
- $R_{DS(on)} = 530 \text{ m}\Omega$  (Typ.)
- Ultra Low Gate Charge (Typ.  $Q_g = 27 \text{ nC}$ )
- Low  $E_{oss}$  (Typ.  $2.8 \text{ }\mu\text{J @ 400V}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 124 \text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant
- ESD Improved Capability

### Description

SuperFET<sup>®</sup> II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance,  $dv/dt$  rate and higher avalanche energy. In addition, internal gate-source ESD diode allows to withstand over 2kV HBM surge stress. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as Audio, Laptop adapter, Lighting, ATX power and industrial power applications.

### Applications

- AC - DC Power Supply
- LED Lighting



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCP650N80Z	Unit
$V_{DSS}$	Drain to Source Voltage	800	V
$V_{GSS}$	Gate to Source Voltage	- DC	$\pm 20$
		- AC ( $f > 1 \text{ Hz}$ )	$\pm 30$
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	10
		- Continuous ( $T_C = 100^\circ\text{C}$ )	6.3
$I_{DM}$	Drain Current	- Pulsed (Note 1)	24
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	204
$I_{AR}$	Avalanche Current	(Note 1)	1.6
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	1.62
$dv/dt$	MOSFET $dv/dt$	100	V/ns
	Peak Diode Recovery $dv/dt$	(Note 3)	
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	162
		- Derate Above $25^\circ\text{C}$	1.30
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCP650N80Z	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.77	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

FCP650N80Z — N-Channel SuperFET<sup>®</sup> II MOSFET

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP650N80Z	FCP650N80Z	TO-220	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	800	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{ mA}$ , Referenced to $25^\circ\text{C}$	-	0.8	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 640\text{ V}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	-	250	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 0.8\text{ mA}$	2.5	-	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 4\text{ A}$	-	530	650	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 4\text{ A}$	-	7.8	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	1178	1565	$\text{pF}$
$C_{oss}$	Output Capacitance		-	36	48	$\text{pF}$
$C_{rss}$	Reverse Transfer Capacitance		-	0.84	-	$\text{pF}$
$C_{oss}$	Output Capacitance	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	18	-	$\text{pF}$
$C_{oss (eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$	-	124	-	$\text{pF}$
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 640\text{ V}, I_D = 8\text{ A}, V_{GS} = 10\text{ V}$	-	27	35	$\text{nC}$
$Q_{gs}$	Gate to Source Gate Charge	(Note 4)	-	6	-	$\text{nC}$
$Q_{gd}$	Gate to Drain "Miller" Charge		-	11	-	$\text{nC}$
ESR	Equivalent Series Resistance		$f = 1\text{ MHz}$	-	1.9	-

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 8\text{ A}, V_{GS} = 10\text{ V}, R_g = 4.7\ \Omega$	-	17	44	ns
$t_r$	Turn-On Rise Time		-	11	32	ns
$t_{d(off)}$	Turn-Off Delay Time		-	40	90	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	3.4	17

### Drain-Source Diode Characteristics

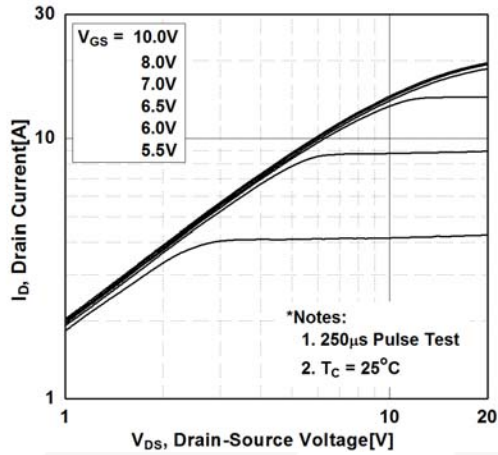
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	10	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	24	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 8\text{ A}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 8\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	-	365	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	5.9	-	$\mu\text{C}$

#### Notes:

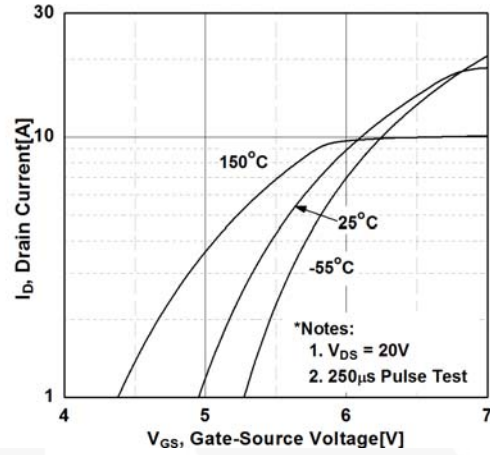
1. Repetitive rating: pulse width limited by maximum junction temperature.
2.  $I_{AS} = 1.6\text{ A}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 10\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

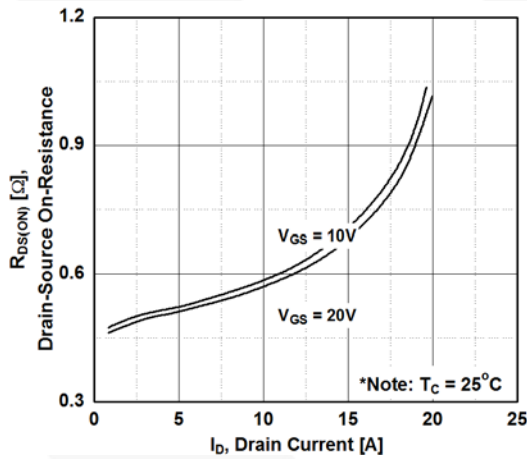
**Figure 1. On-Region Characteristics**



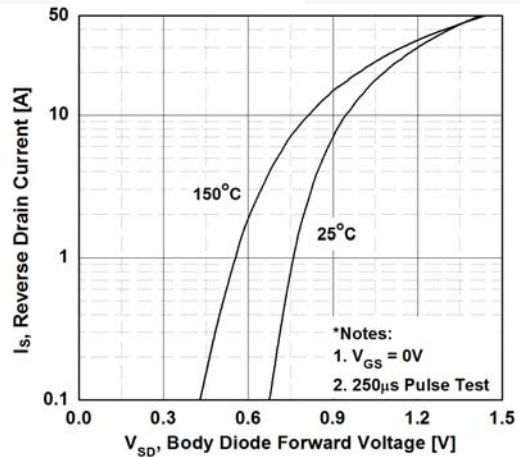
**Figure 2. Transfer Characteristics**



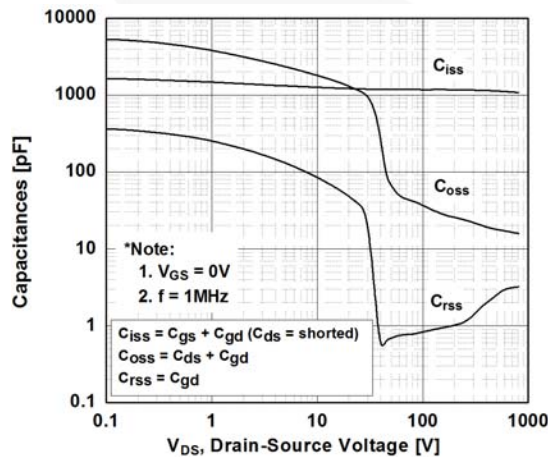
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



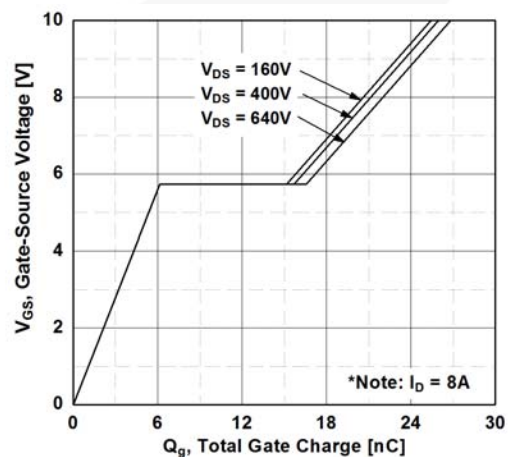
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

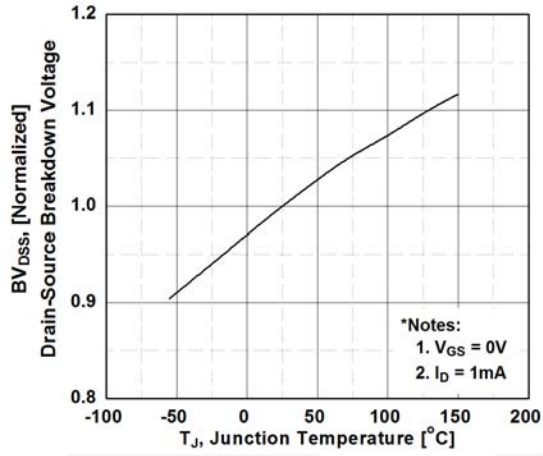


**Figure 6. Gate Charge Characteristics**

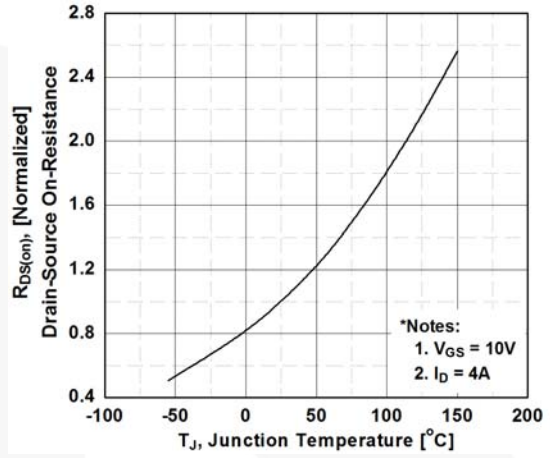


**Typical Performance Characteristics** (Continued)

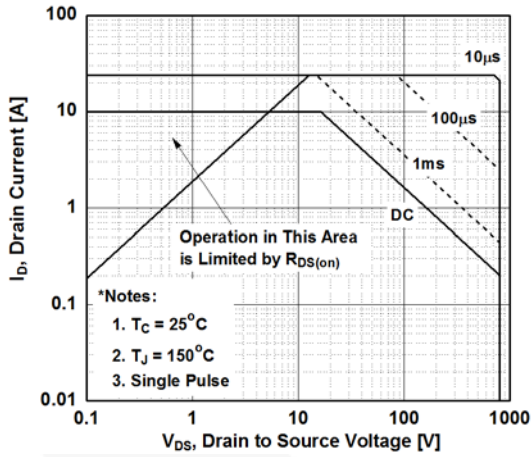
**Figure 7. Breakdown Voltage Variation vs. Temperature**



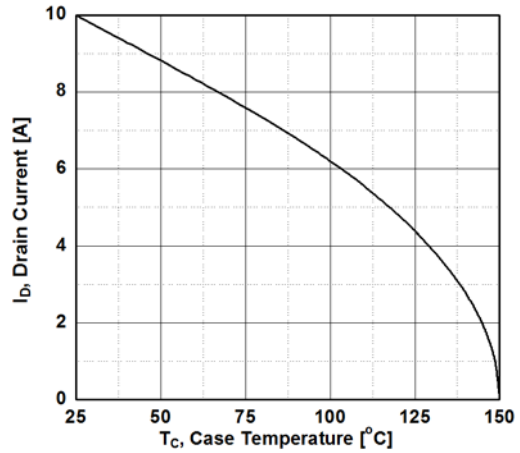
**Figure 8. On-Resistance Variation vs. Temperature**



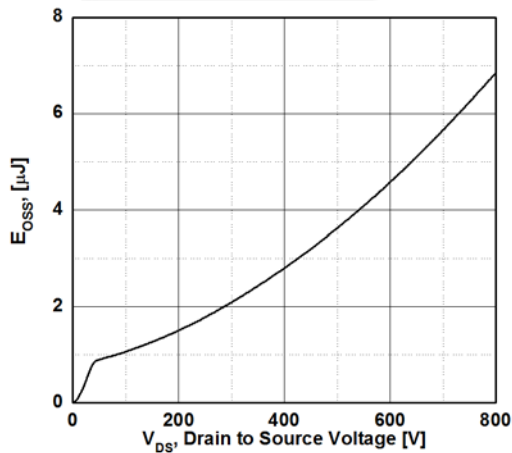
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**

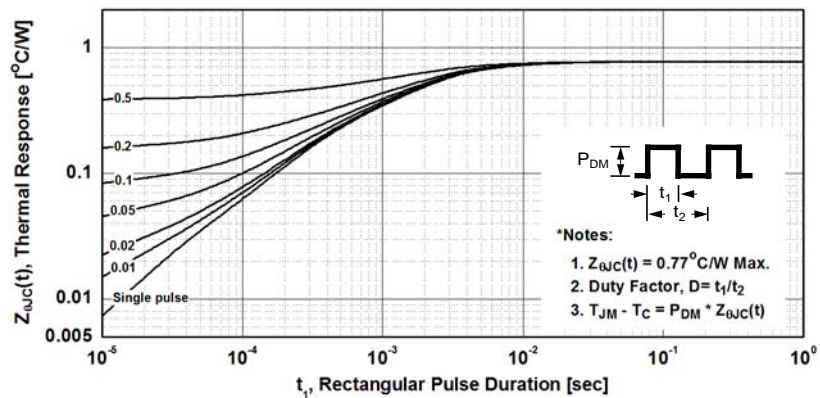


**Figure 11. E\_oss vs. Drain to Source Voltage**



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



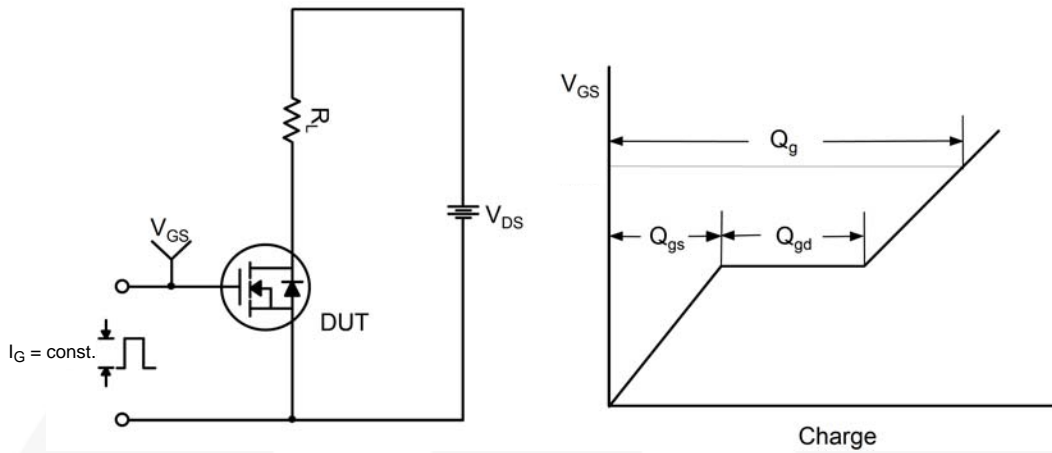


Figure 13. Gate Charge Test Circuit & Waveform

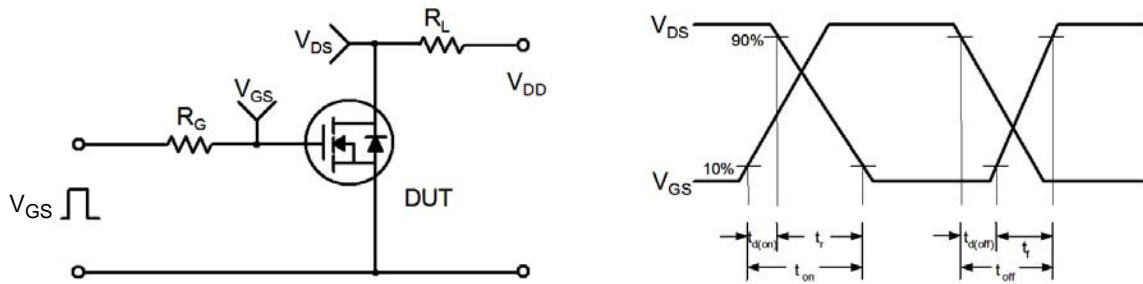


Figure 14. Resistive Switching Test Circuit & Waveforms

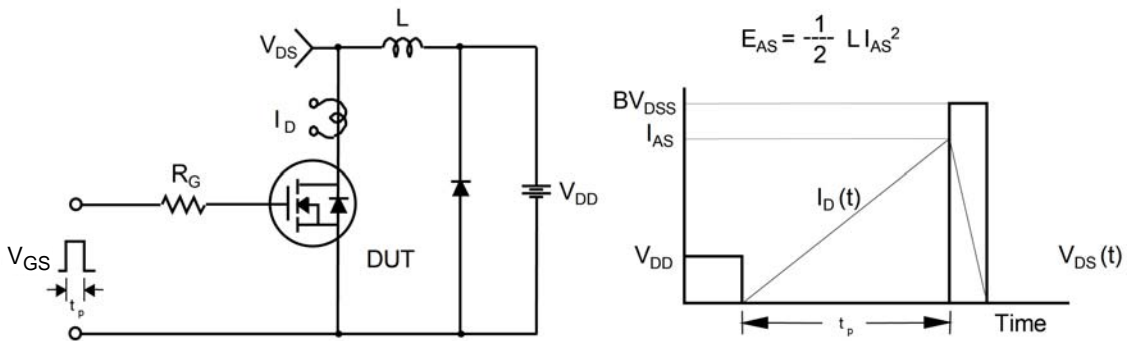


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

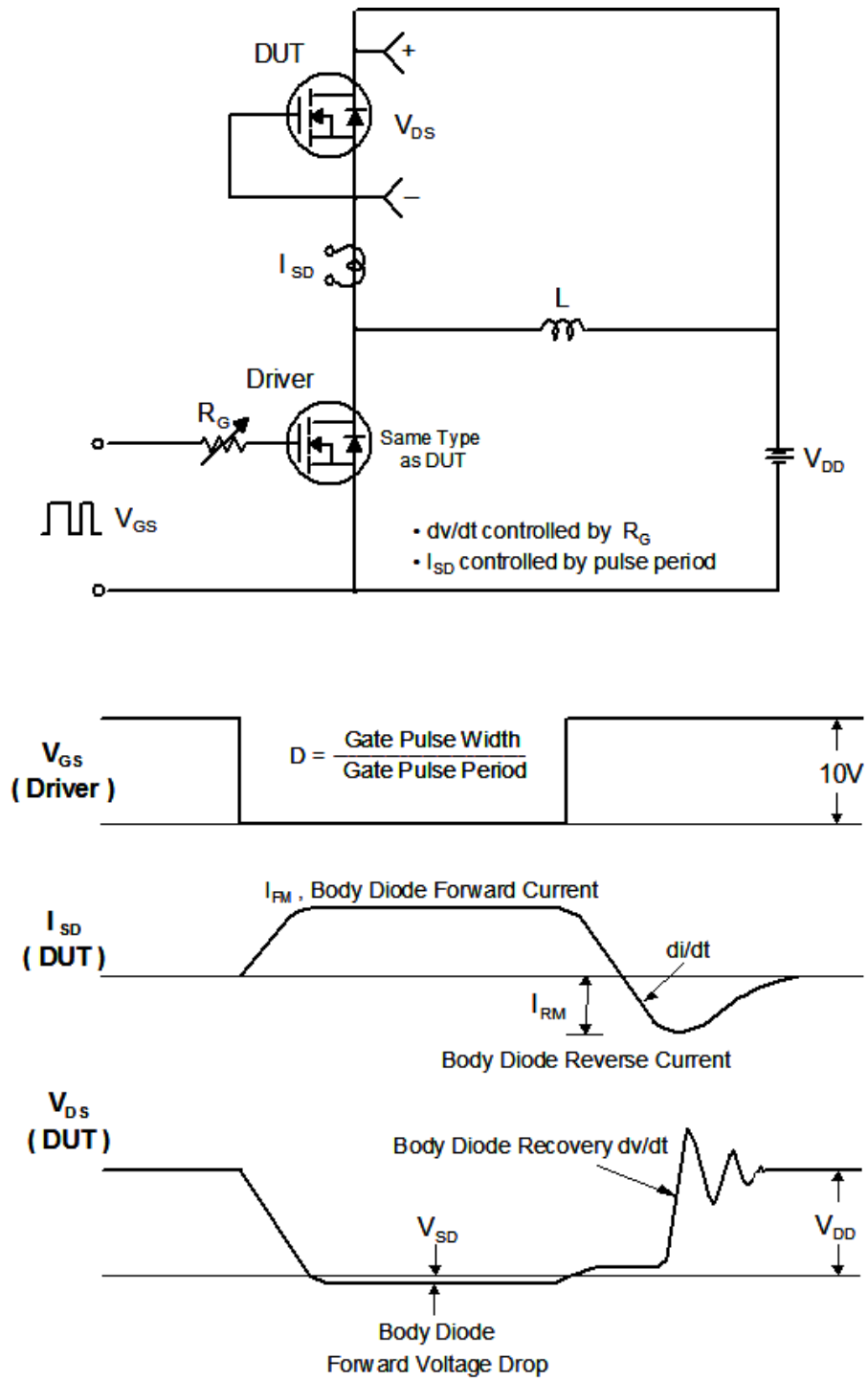


Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms





- NOTES:
- A) REFERENCE JEDEC, TO-220, VARIATION AB
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
  - D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
  - E) DOES NOT COMPLY JEDEC STANDARD VALUE.
  - F) "A1" DIMENSIONS AS BELOW:  
 SINGLE GAUGE = 0.51 - 0.61  
 DUAL GAUGE = 1.10 - 1.45
  - G) DRAWING FILE NAME: TO220B03REV9
  - H) PRESENCE IS SUPPLIER DEPENDENT
  - I) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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