LTM2887
SPI/Digital or I²C µModule Isolator with Dual Adjustable 5V Regulators

DESCRIPTION

Demonstration circuit 1791A is a serial peripheral interface bus (SPI) or inter-IC bus (I²C) µModule isolator with dual adjustable 5V regulators featuring the LTM®2887. The demo circuit features an EMI optimized circuit configuration and printed circuit board layout. All components are integrated into the µModule isolator. The demo circuit operates from a single external supply on V_{CC}. The part generates output voltages on V_{CC2} and V_{L2} which may be adjusted by external programming resistors. It communicates all necessary signaling across the isolation barrier through LTC's isolator µModule technology.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Input Supply Range	LTM2887-3	3.0	3.3	3.6	V
		LTM2887-5	4.5	5.0	5.5	V
V_{CC2}	Regulated Output Voltage		4.75	5	5.25	V
	Adjustable Output Voltage Range		0.6		5.5	V
	Internal Current Limit	ΔV_{CC2} = –5%	110			mA
V_{L2}	Regulated Output Voltage		4.75	5	5.25	V
	Adjustable Output Voltage Range		1.62		5.5	V
	Internal Current Limit	ΔV_{L2} = –5%	110			mA
f_{MAX}	Maximum Data Rate	DI1 → O1, Ix → DOx, CL = 15pF	20			MHz
		LTM2887-S, Bidirectional Communication LTM2887-S, Unidirectional Communication	4 8			MHz MHz
		LTM2883-I	400			kHz
V_{IORM}	Maximum Working Insulation Voltage	GND to GND2	560			V_{DC}
			400			V_{RMS}
	Common Mode Transient Immunity		30			kV/µs

OPERATING PRINCIPLES

The LTM2887 contains an isolated DC/DC conversion system with multiple LDOs to deliver power to the two output voltage rails from V_{CC}. Isolation is maintained by the separation of GND and GND2 where significant operating voltages and transients can exist without affecting the operation of the LTM2887. The logic side ON pin enables or shuts down the LTM2887. All logic side signals are referenced to the logic supply pin V_L. The LTM2887 is available in two data bus configurations, SPI (–S) or I²C (–I), and with two input voltage ranges, 3.0 to 3.6 volts (–3) or 4.5 to 5.5 volts (–5).

OPERATING PRINCIPLES

SPI signaling is controlled by the logic inputs $\overline{CS}$, SDI, and SCK. $\overline{SDOE}$ controls the SDO output and is normally connected to $\overline{CS}$. The corresponding isolated side output signals are $\overline{CS2}$, SDI2, and SCK2. SDO2 is the isolated side SPI data input. All of the SPI communication channels may be used as generic digital I/O.

I^2C signaling is controlled by the logic inputs SDA and SCL, corresponding to SDA2 and SCL2 on the isolated side. The SCL channel is unidirectional supporting master mode only I^2C communication. SCL2 output is standard CMOS push-pull drive. SDA signaling is bidirectional, and includes an internal current source pull-up on SDA2 supporting up to 200pF of load capacitance.

Demo circuit 1791A is available in four configurations supporting all versions of the LTM2887. Table 1 details the demo circuit configurations.

Table 1.

DEMO CIRCUIT	INPUT VOLTAGE	COMMUNICATION
DC1791A-A	3.0V to 3.6V	SPI/Digital
DC1791A-B	4.5V to 5.5V	SPI/Digital
DC1791A-C	3.0V to 3.6V	I^2C
DC1791A-D	4.5V to 5.5V	I^2C

The demo circuit has been designed and optimized for low RF emissions. To this end some features of the LTM2887 are not available for evaluation on the demo circuit. The logic supply voltage V_L is tied to V_{CC} on the demo circuit, and the ON pin is not available on the input pin header, but may be controlled by jumper JP1. EMI mitigation techniques used include the following.

1. Four layer PCB, allowing for isolated side to logic side "bridge" capacitor. The bridge capacitor is formed between an inner layer of floating copper which overlaps the logic side and isolated side ground planes. This structure creates two series capacitors, each with approximately .008" of insulation, supporting the full dielectric withstand rating of $2500V_{RMS}$. The bridge capacitor provides a low impedance return path for injected currents due to parasitic capacitances of the LTM2887's signal and power isolating elements.
2. Discrete bridge capacitors (C3, C4) mounted between GND2 and GND. The discrete capacitors provide additional attenuation at frequencies below 400MHz. Capacitors are safety rated type Y2, manufactured by Murata, part # GA342QR7GF471KW01L.
3. Board/ground plane size has been minimized. This reduces the dipole antenna formed between the logic side and isolated side ground planes.
4. Top signal routing and ground floods have been optimized to reduce signal loops, minimizing differential mode radiation.
5. Common mode filtering is integrated into the input and output pin headers. Filtering helps to reduce emissions caused by conducted noise and minimizes the effects of cabling to common mode emissions.
6. A combination of low ESL and high ESR decoupling is used. A low ESL ceramic capacitor is located close to the module minimizing high frequency noise conduction. A high ESR tantalum capacitor is included to minimize board resonances and prevent voltage spikes due to hot plugging of the supply voltage.

EMI performance is shown in Figure 1, measured using a Gigahertz Transverse Electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, "Testing and Measurement Techniques – Emission and Immunity Testing in Transverse Electromagnetic Waveguides".

OPERATING PRINCIPLES

LTM2887 Low EMI Demo Board Radiated Emissions

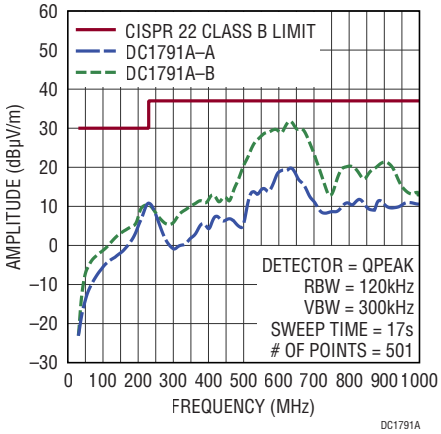


Figure 1. DC1791A Radiated Emissions

The demo circuit includes provisions for programming the two output voltage rails. Resistors R6, R7 and R5, R10 allow the V_{L2} and V_{CC2} power rails, respectively, to be reduced from their nominal operating voltages. The value of R6 or R5 should be no greater than 6.04k to minimize errors in the output voltage caused by the internal voltage dividers. The formulas presented in Table 2 allow selection of the appropriate resistor values. In addition the current limit of each output voltage rail may also be programmed. The current limit threshold is set by resistors R8 and R9 for I_{VL2} and I_{VCC2} respectively. The current limit is nominally 100mA. The current limit may be reduced for either output by the following equation:

$$R_{IMAX}(R8, R9) = [119.22–(0.894) \bullet (V_{L2}, V_{CC2})]/I_{LIMIT}$$

Table 2.

VOLTAGE RAIL	RESISTOR TO REDUCE OUTPUT
V_{CC2}	= 0.6V(1 + R7/R6)
V_{L2}	= 0.6V(1 + R10/R5)

QUICK START PROCEDURE

Demonstration circuit 1791A is easy to set up and evaluate the performance of the LTM2887. Refer to Figure 2 for proper measurement equipment setup and follow the procedure below.

NOTE: When measuring the input or output voltage ripple or high speed signals, care must be taken to avoid a long ground lead on the oscilloscope probe.

1. Install JP1 in the ON (default) position.
2. With power off, connect the input power supply to V_{CC} and GND on pin header J1.
3. Turn on the power at the input.

NOTE: Make sure that the input voltage does not exceed 6V.

4. Check for the proper output voltages. V_{CC2} = 5V and V_{L2} = 5V on pin header J2.
5. Once the proper output voltages are established, connect signals to J1 and J2 pin headers as appropriate. The header pin names and locations are detailed on the demo board silkscreen below the pin headers.

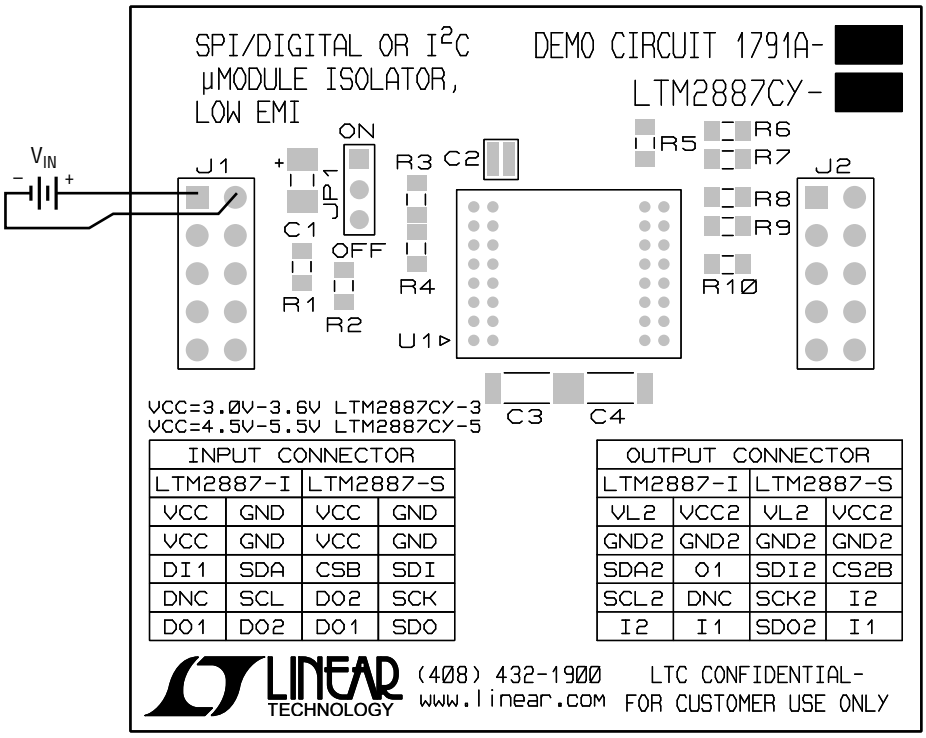
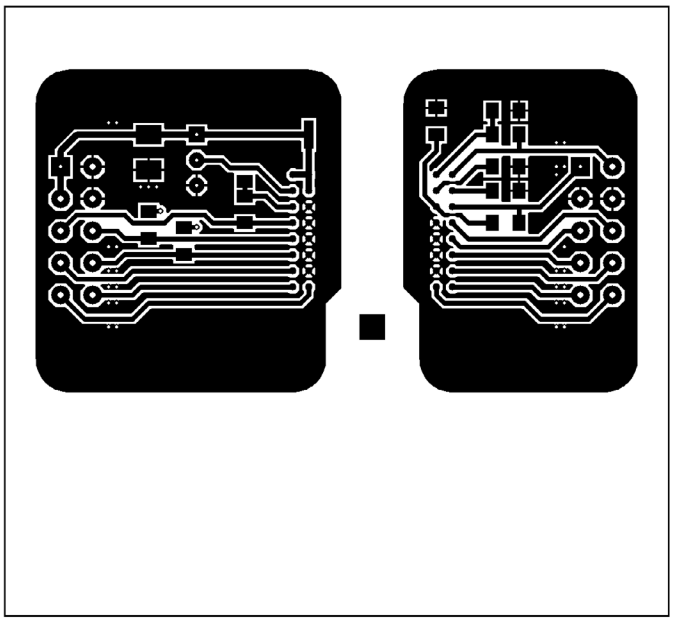


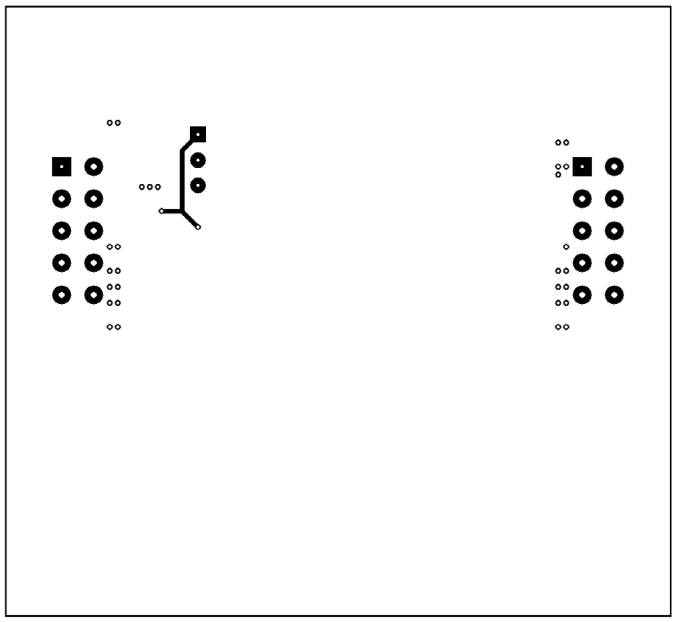
Figure 2. Demo Board Setup

PCB LAYOUT

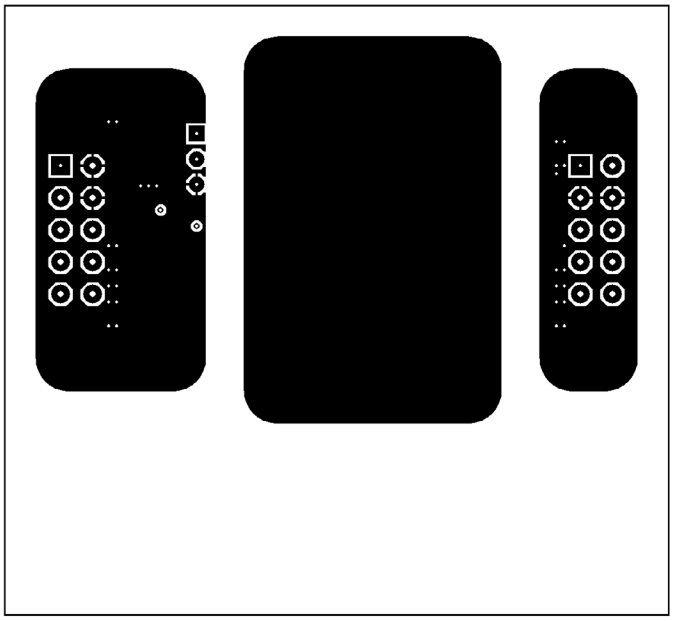
Layer 1. Top Layer



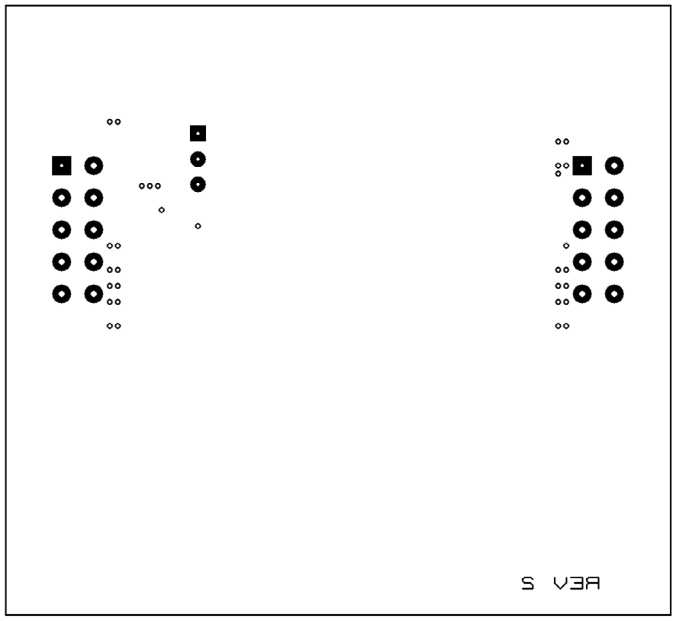
Layer 3. Signal Layer



Layer 2. Ground Plane



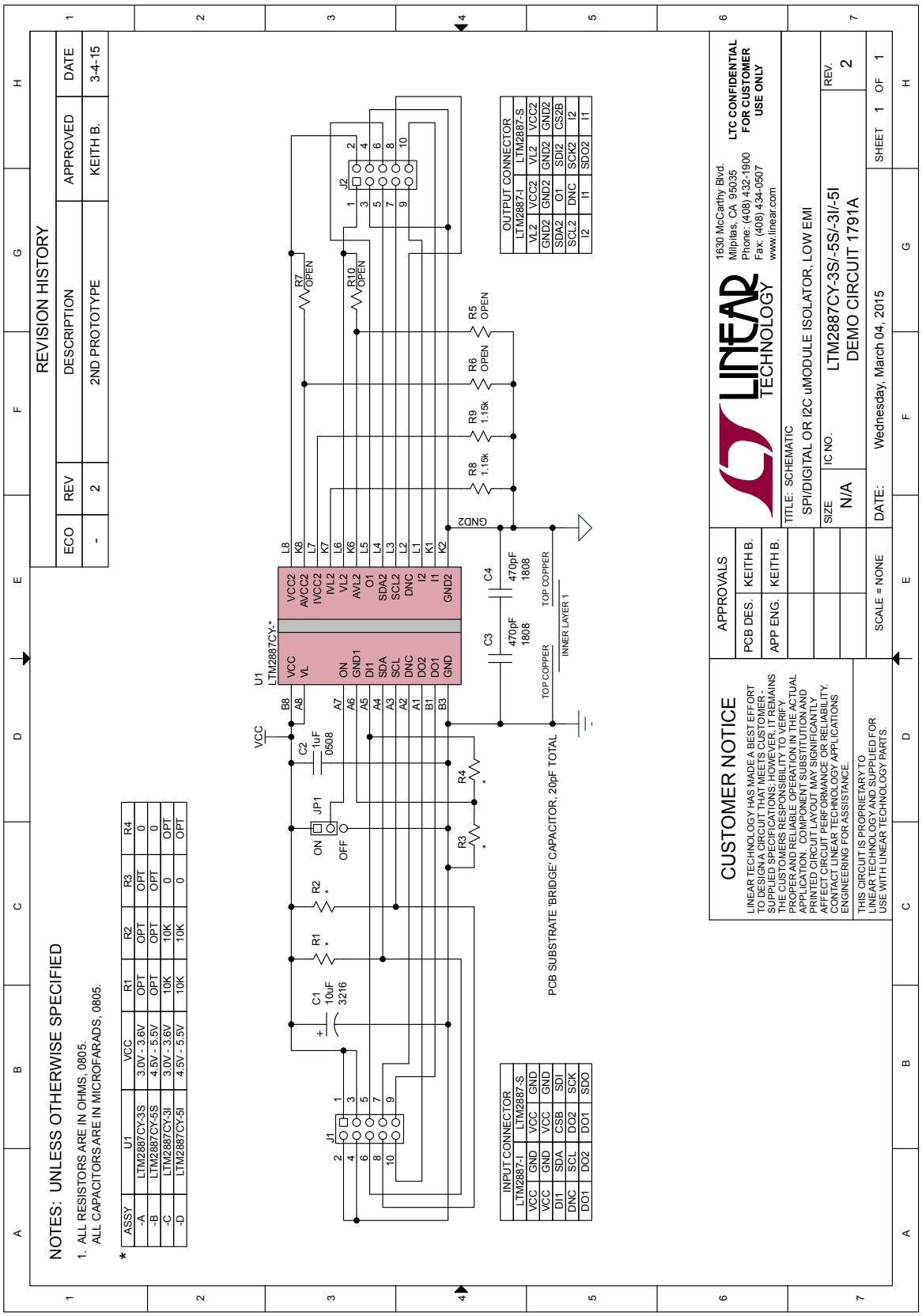
Layer 4. Bottom Layer



PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	U1 –A –B –C –D	I.C., LTM2887CY-3S I.C., LTM2887CY-5S I.C., LTM2887CY-3I I.C., LTM2887CY-5I	LINEAR LTM2887CY-3S#PBF LINEAR LTM2887CY-5S#PBF LINEAR LTM2887CY-3I#PBF LINEAR LTM2887CY-5I#PBF
Hardware/Components (For Demo Board Only)				
2	1	C1	CAP., TANT 10µF 10V 20% 1206	AVX TAJA106M016RNJ
3	1	C2	CAP., CER 1µF 10V 20% 0508	MURATA LLL219R71A105MA01L
4	2	C3, C4	CAP., CER 470pF 250Vac 10% 1808	MURATA GA342QR7GF471KW01L
5	2	J1, J2	0.1" DOUBLE ROW HEADER, 5 × 2 PIN	SAMTEC TSW-105-22-G-D
6	2	J1, J2	0.1" FERRITE PLATE, 5 × 2 HOLE	FAIR RITE 2644247101
7	1	JP1	Header, 1 × 3 2mm	WURTH 62000311121
8	1	JP1	SHUNT, 1 × 2 2mm	WURTH 60800213421
9	1	R1 –C –D	RES., CHIP 10kΩ 1% 0805 RES., CHIP 10kΩ 1% 0805	YAGEO RC0805FR-0710KL YAGEO RC0805FR-0710KL
10	1	R2 –C –D	RES., CHIP 10kΩ 1% 0805 RES., CHIP 10kΩ 1% 0805	YAGEO RC0805FR-0710KL YAGEO RC0805FR-0710KL
11	1	R3 –C –D	RES., CHIP 0 0805 RES., CHIP 0 0805	YAGEO RC0805FR-070RL YAGEO RC0805FR-070RL
12	1	R4 –A –B	RES., CHIP 0 0805 RES., CHIP 0 0805	YAGEO RC0805FR-070RL YAGEO RC0805FR-070RL
13	2	R6, R7	RES., CHIP 1.15kΩ 1% 0805	YAGEO RC0805FR-071K15L

SCHEMATIC DIAGRAM



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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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