TLF51801ELV

10 A synchronous DC/DC Step-Down Controller

Data sheet

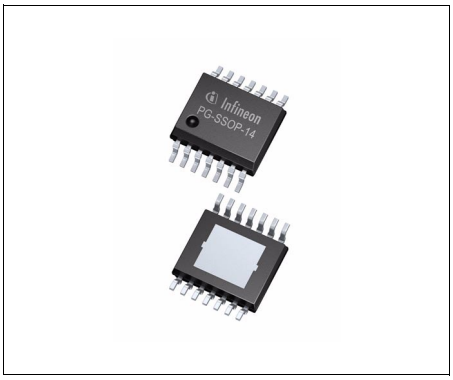
Rev. 1.0.1, 2013-04-15

Automotive Power

AEC Qualified RoHS

1 Overview

- 10 A synchronous step down Controller
- Current limitation adjustable with Shunt resistor or Rdson
- Adjustable output voltage
- ± 2% output voltage tolerance
- External power transistors
- Integrated bootstrap diode
- PWM regulation
- Very Low Dropout Operation: max Duty Cycle higher than 99%
- Input voltage range from 4.75V to 45V
- Adjustable switching frequency from 100 to 700 kHz
- Synchronization input
- Very low shutdown current consumption (<2µA)
- Soft-start function
- Input undervoltage lockout
- Suited for automotive applications: T_j = -40°C to +150°C
- Green Product (RoHS compliant)
- AEC Qualified



PG-SSOP-14

Description

The TLF51801ELV is a PWM step-down DC/DC controller with external power switches, packaged in a small PG-SSOP-14 with exposed pad. The controller is capable to drive external power MOSFETs for load currents up to 10 A. A current limitation feature is included, it is done by measuring the voltage over the high-side switch (when switch is closed) in Rdson-configuration or by including a shunt resistor above the high-side switch in Shunt-configuration.

Type	Package	Marking
TLF51801ELV	PG-SSOP-14	TLF51801

2 Block Diagram

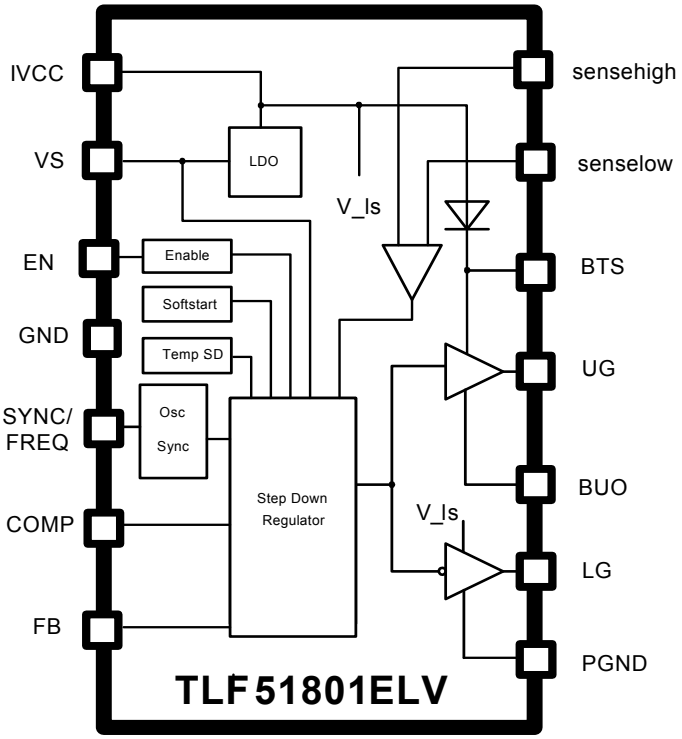


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

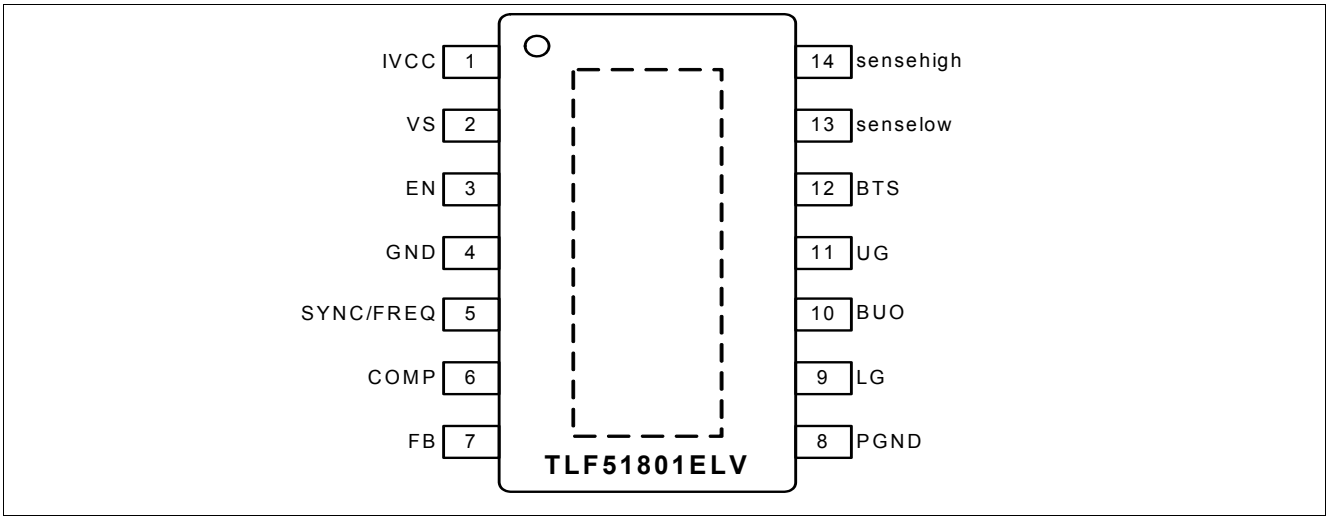


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	IVCC	**Internal Voltage Supply** Output of the internal linear regulator, supply for low-side driver and through internal bootstrap diode to high-side driver, connect a capacitor between this pin and GND
2	VS	**Input Voltage** Connect to input voltage for internal power supply
3	EN	**Enable Input** Active-high enable input with integrated pull down resistor
4	GND	**Ground** Connect to ground plane
5	SYNC/ FREQ	**Synchronization and Oscillator frequency set Input** Connect to an external clock signal in order to synchronize/adjust the switching frequency (SYNC-mode). Connect an external resistor to set the frequency (FREQ-mode)
6	COMP	**Compensation Input** Frequency compensation for regulation loop stability Connect to compensation network
7	FB	**Feedback Input** Connect via voltage divider to output capacitor
8	PGND	**Power Ground** Connect to Ground plane
9	LG	**Low-side MOSFET driver output** Driving output for the low-side external power MOSFET, connect to gate
10	BUO	**Buck Switch Out** Connect this point between the switching transistors, floating ground for high-side driver

Pin	Symbol	Function
11	UG	**Up-side MOSFET driver output** Driving output for the high-side external power MOSFET, connect to gate
12	BTS	**Buck Driver Supply Input** Connect the bootstrap capacitor between this pin and pin BUO
13	sense low	**Current sensing (low-side) input** For Shunt-configuration connect a shunt resistor from senselow to input/battery voltage, for Rdson-configuration connect to source of the high-side MOSFET
14	sense high	**Current sensing (high-side) input** Connect a resistor between battery and this pin to adjust the current threshold for both Rdson and Shunt configurations
Exposed Pad		Connect to heatsink area and GND by low inductance wiring

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings[1)]

T_j = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Synchronization Input	V_{SYNC}	-0.3	5.5	V	–
4.1.2				6.2	V	t < 10s[2)]
4.1.3	Compensation Input	V_{COMP}	-0.3	5.5	V	–
4.1.4				6.2	V	t < 10s[2)]
4.1.5	Feedback Input	V_{FB}	-0.3	5.5	V	
4.1.6	Buck Driver Supply Input	V_{BTS}	V_{BUO} - 0.3	V_{BUO} + 5.0	V	
4.1.7	Buck Switch Output	V_{BUO}	-2.0	45	V	
4.1.8	Enable Input	V_{EN}	-20	45	V	
4.1.9	Supply Voltage Input	V_S	-0.3	45	V	
4.1.10	Sensehigh	$V_{sensehigh}$	-0.3	45	V	
4.1.11	Senselow	$V_{senselow}$	-2.0	$V_{sensehigh}$ + 0.3	V	
4.1.12	IVCC	V_{IVCC}	-0.3	6.0	V	
4.1.13	Upper Transistor Gate	V_{UG}	V_{BUO} - 0.3	V_{BTS} + 0.3	V	
4.1.14	Lower Transistor Gate	V_{LG}	-0.3	6.5	V	
Temperatures						
4.1.15	Junction Temperature	T_j	-40	150	°C	–
4.1.16	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.17	ESD Resistivity	V_{ESD}	-2	2	kV	HBM [2)]
4.1.18	ESD Resistivity to GND	V_{ESD}	-500	500	V	CDM [3)]
4.1.19	ESD Resistivity corner pins to GND	V_{ESD}	-750	750	V	CDM [3)]

1) Not subject to production test, specified by design

2) ESD susceptibility HBM according to ANSI/ESDA/JEDEC JS-001.

3) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage	V_S	4.75	45	V	–
4.2.2	Max. Duty Cycle	D_{max}	–	>99	%	–
4.2.3	Output Voltage adjust range	V_{CC}	1.20	D_{max} x V_S	V	–
4.2.4	Junction Temperature	T_j	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case[1)]	R_{thJC}	–	10	–	K/W	–
4.3.2	Junction to Ambient[1) 2)]	R_{thJA}	–	47	–	K/W	2s2p
4.3.3		R_{thJA}	–	54	–	K/W	1s0p + 600 mm^2
4.3.4		R_{thJA}	–	64	–	K/W	1s0p + 300 mm^2

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board;

5 Regulator

5.1 Description

The TLF51801ELV is a synchronous step down controller for output currents up to 10 Amps. The power stage consists of two external MOSFETs with logic level gate signal. The switching frequency can be adjusted between 100 and 700 kHz by connecting an external resistor between pin SYNC/FREQ and GND (FREQ-mode). By connecting this pin to a frequency source the TLF51801ELV might be synchronized to a frequency between 350 and 700 kHz (SYNC-mode).

A valid high signal at pin EN will start the regulator. Then it will ramp up with a soft start ramp, which is derived from the switching frequency (i.e.: the soft start ramp will last around 1 msec at a switching frequency of 500 kHz).

The regulator is working in voltage mode, there is no feedforward function included and it operates in continuous conduction mode only.

An external compensation network connected to pin COMP is necessary to compensate the switching ripple on the feedback line. The compensation network must be adapted to the application.

The regulator can withstand a short circuit at the output. The current limitation can be implemented measuring the drop across the Rdson of the external high-side MOSFET (Rdson-configuration), or by shunt resistor located in series with the drain of high-side MOSFET (Shunt-configuration).

The output voltage is monitored using pin FB. If the output voltage exceeds the overvoltage threshold (10% higher than the regulated output voltage), the low-side external MOSFET is turned on in order to discharge the output capacitor and lower the output voltage to the nominal value.

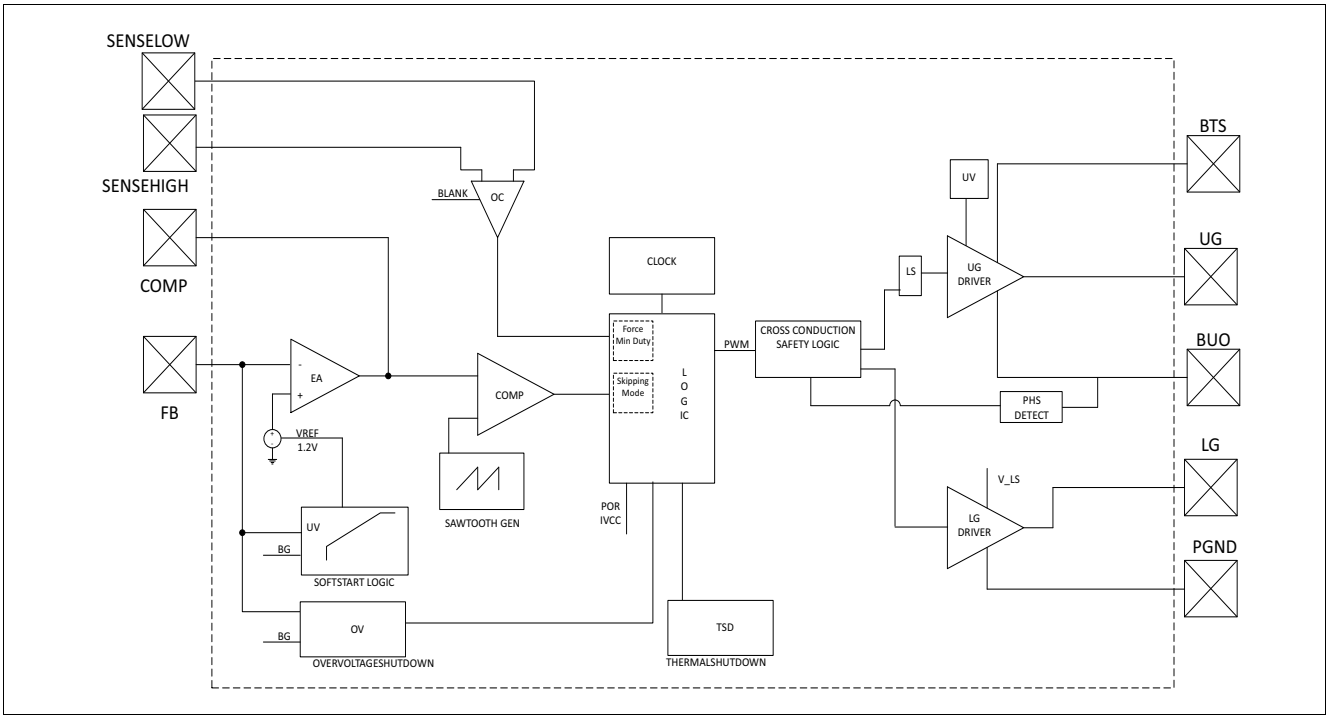


Figure 3 Block Diagram Buck Regulator

5.2 The Soft start

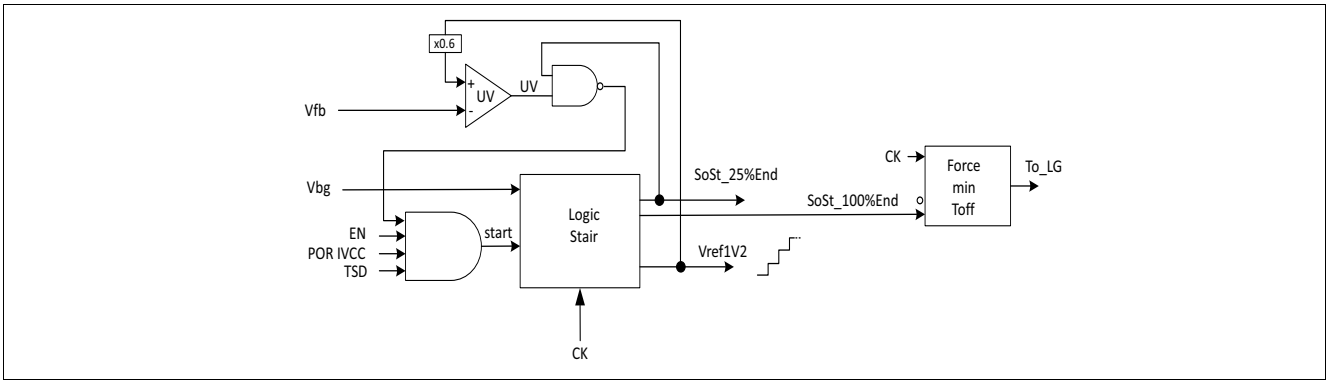


Figure 4 Soft start block diagram

An integrated Soft start function (of duration 512 clock cycles, where a clock cycle is derived from the switching frequency) ensures that the inrush current will be limited and prevents from output voltage overshoots.

When the regulator starts from OFF state (EN pin forced from low to high), an additional pre-charging function is triggered before Soft start: for a time slot of 64 clock cycles, low-side MOSFET is switched ON and OFF at fixed frequency of 1.5 MHz and 50% duty cycle, in order to charge in advance the bootstrap capacitor.

If an under voltage appears during Soft start, it is recognized only after 25% of the Soft start stair, this is realized by the signal SoSt_25%End. In case 1) the UV is permanent fault (i.e. the BTS cap is not charged or shorted, or the output cap is shorted). In case 2) the UV failure is removed before the 25% of the Soft start procedure is reached (i.e. the output cap is too large and the system is not able to charge it fast enough). In case 1), a permanent UV, the soft start begins again the procedure after a delay of 512 clock cycles.

In case of pre-charged output condition, the system recognizes it and keeps the external switches in high impedance in order not to discharge the output capacitance.

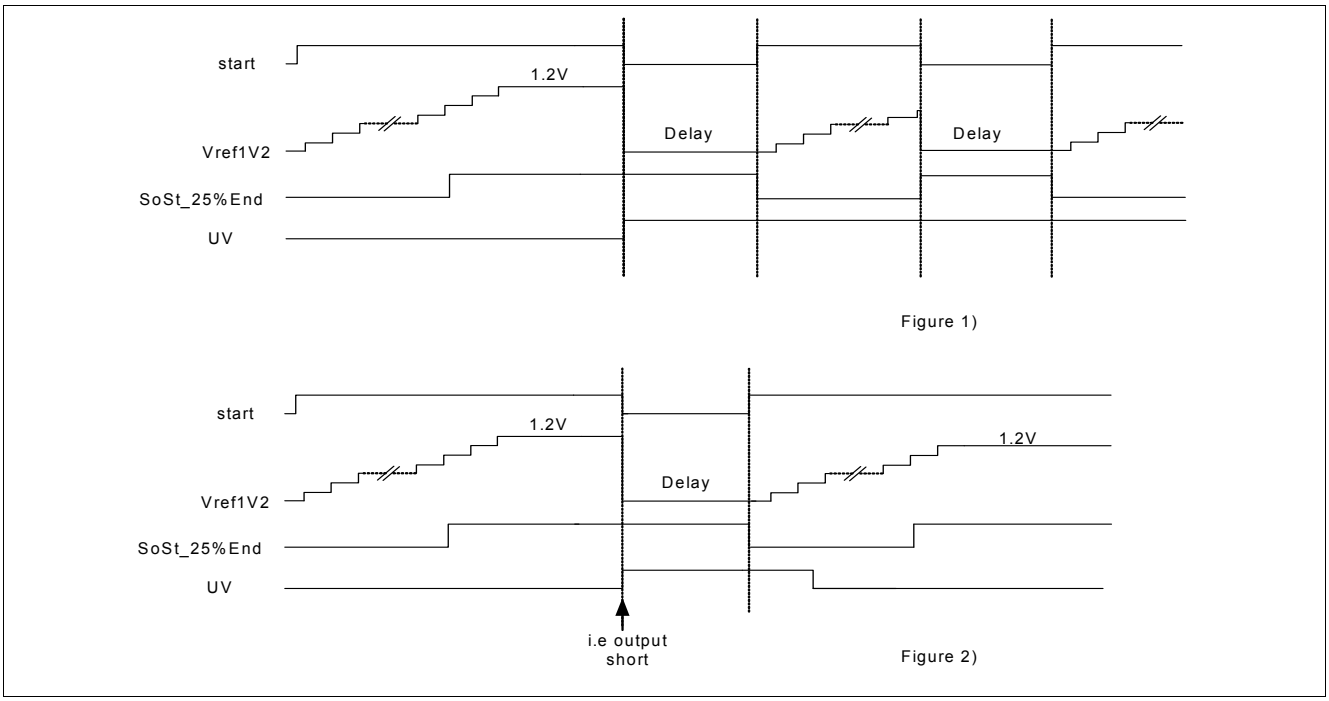


Figure 5 Soft start timing

5.3 Operation Mode

The PWM pulses are voltage controlled. The error amplifier and the PWM comparator are creating the PWM pulses using the oscillator saw-tooth signal and the feedback voltage. The pulse-width modulation is done so that the feedback voltage is similar to the reference voltage (1.2 V). To achieve a stable output voltage even under very low or very high duty cycle conditions a pulse skipping mode is implemented. When the minimum off time for the up-side gate is reached (boundary between dark grey area and light grey area in **Figure 6**), the TLF51801ELV operates in pulse skipping mode for high duty cycle. This operation mode is typically used with low supply voltages for very low dropout operation. If the minimum on time for the up-side gate is reached (boundary between dark grey area and light grey area in **Figure 6**) the TLF51801ELV operates in pulse skipping mode for low duty cycle.

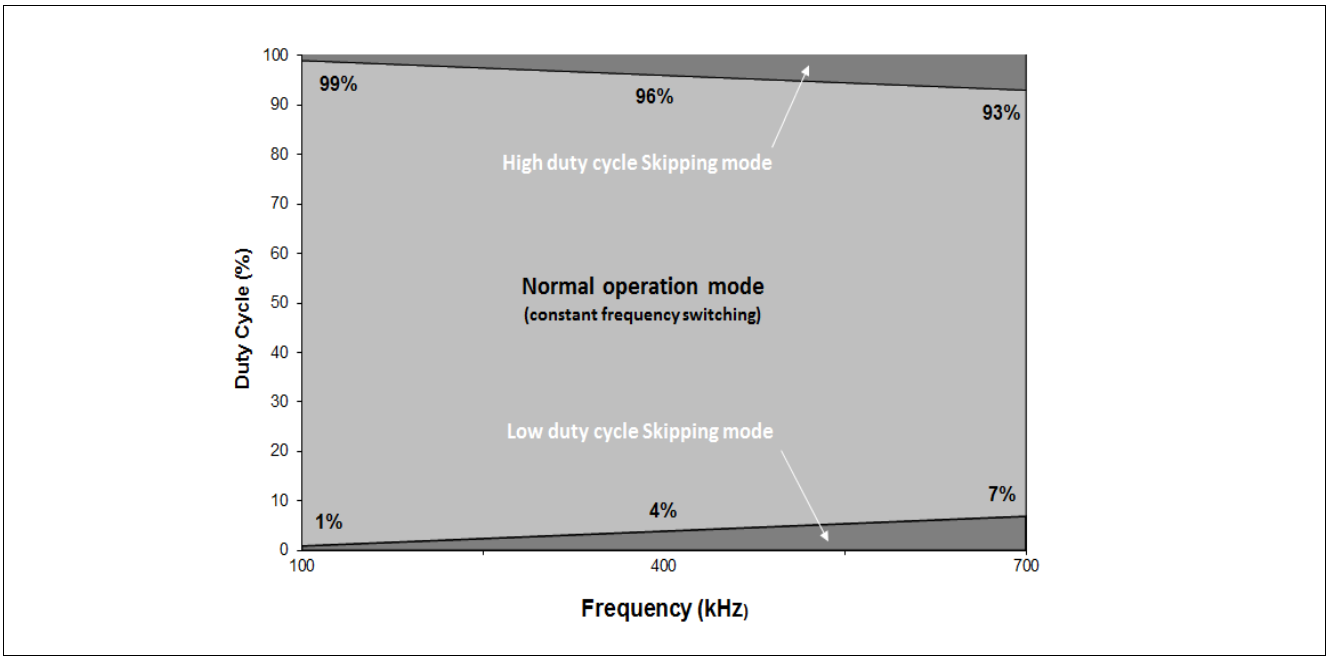


Figure 6 Operation Mode

5.4 Bootstrap concept

The high-side MOSFET driver is supplied by the bootstrap concept. The capacitor at pin BTS and BUO must be switched to GND to be charged by the internal LDO. A monitoring circuit controls the charge of the bootstrap capacitor. If the charge is sufficient the driver will trigger the external high-side MOSFET. If a recharge is necessary, the capacitor will be loaded using the integrated bootstrap diode by switching pin BUO to ground forcing a proper PWM signal.

For very high duty-cycle and high input capacitance of the MOSFET, it may be necessary to consider use of an external diode placed in parallel with the internal bootstrap diode to speed up the recharge of the bootstrap capacitor. In addition, the small voltage drop across the external diode improves the overdrive of the gate of the high-side MOSFET.

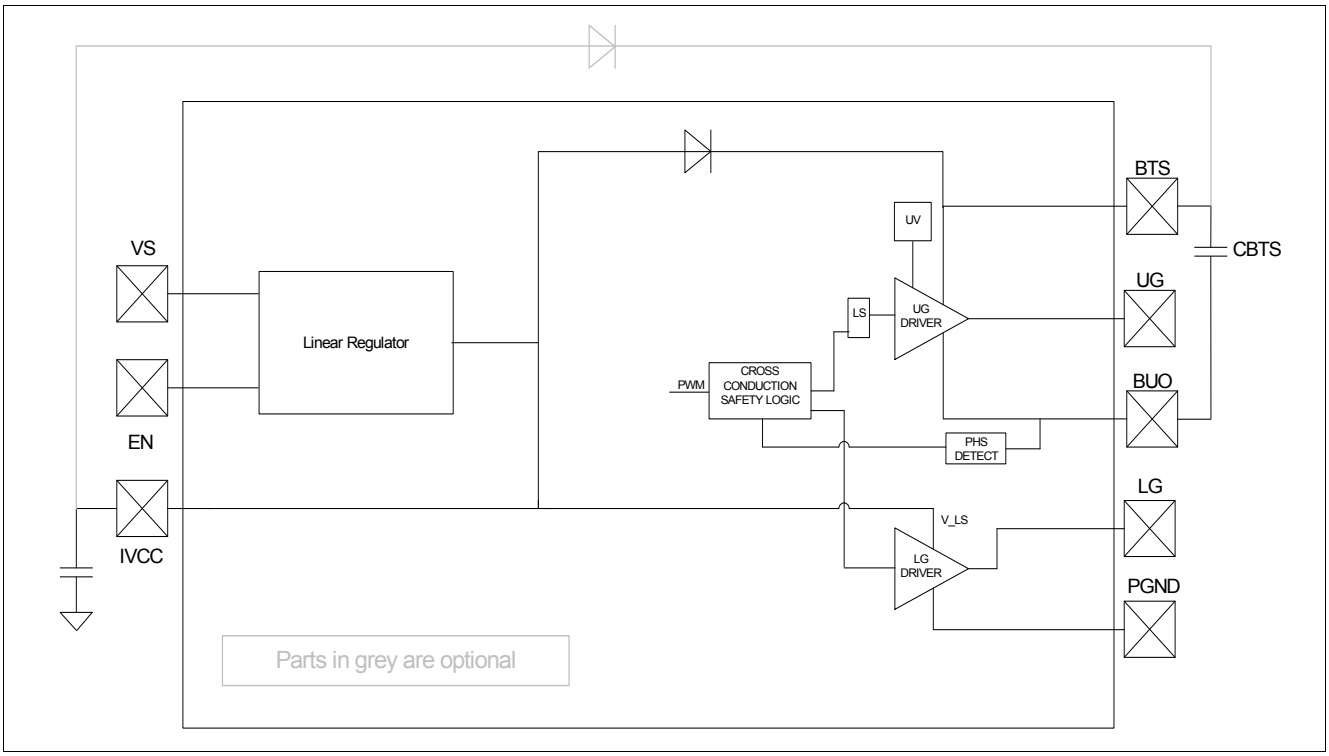


Figure 7 Bootstrap concept

5.5 Current Limitation

5.5.1 Rdson-configuration

To optimize the efficiency, the regulator is measuring the voltage (which is the current through the MOSFET multiplied by the Rdson) over the high-side switch, if it should be too high the pulse will be cut off. By varying the sense resistor between the pin sensehigh and the drain of the high-side MOSFET the current limit can be adjusted. Senselow is connected to the source of the MOSFET.

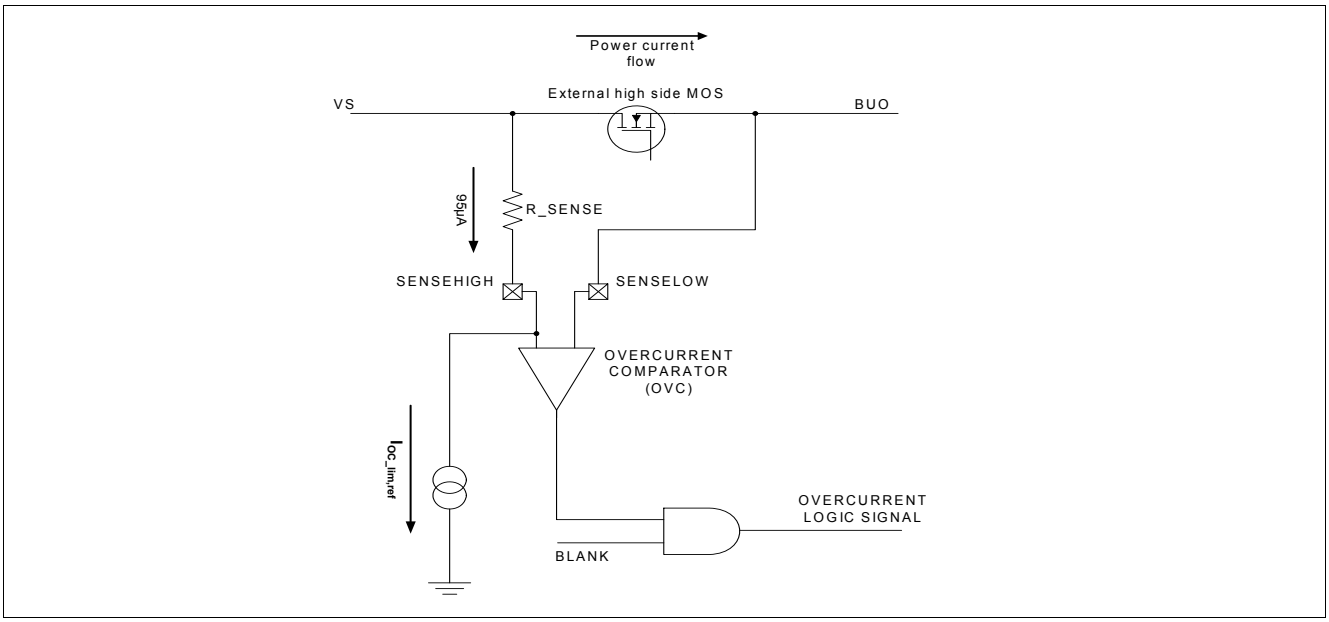


Figure 8 Rdson-configuration for current limitation

The figure above shows the concept of the Rdson configuration for current limitation. The characteristics of the external high-side MOSFET must be known, especially its thermal behavior. The current limitation might be calculated with the following equation:

$$I_{limit} = I_{OC\_lim,\,ref} \cdot \frac{R\_SENSE}{Rdson\_EXT\_MOS}$$

5.5.2 Shunt-configuration

The regulator is offering a second possibility to do a more accurate current measurement by shunt resistor located in series with the drain of the high-side MOSFET. The shunt resistor will be placed in the input current path and be connected to the overcurrent comparator with pin senselow and through a sense resistor to pin sensehigh. By varying the sense resistor the current limit can be adjusted.

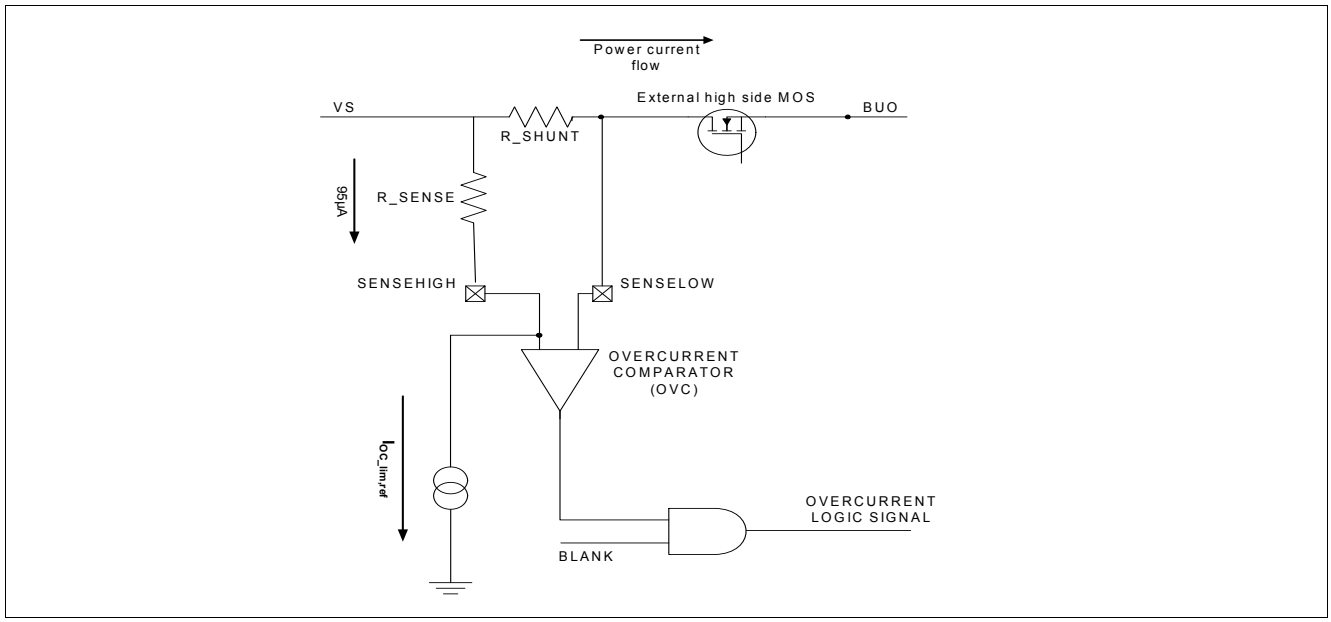


Figure 9 Shunt-configuration for current limitation

The Shunt-configuration works similar to the Rdson-configuration, it uses also pins Sensehigh and Senselow. The current limitation might be calculated with the following equation:

$$I_{limit} = I_{OC\_lim,ref} \cdot \frac{R\_SENSE}{R\_SHUNT}$$

5.6 Electrical Characteristics

Electrical Characteristics:

V_S = 6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.6.1	Output voltage	V_{FB}	1.176	1.200	1.224	V	V_{EN} = 12V; I_{CC} < 10A
5.6.2	Output overvoltage threshold	$V_{FB,OV}$	1.05 x V_{FB}	1.1 x V_{FB}	1.15 x V_{FB}	V	V_{FB} increasing; V_{COMP} = 3V; Monitor LG low to high
5.6.3	Output overvoltage threshold hysteresis	$V_{FB,OV,hyst}$	0.02 x V_{FB}	0.05 x V_{FB}	0.08 x V_{FB}	V	–
5.6.4	FB input current	I_{FB}	-1	-0.1	0	µA	V_{FB} = 1.2V
5.6.5	Error amplifier, gain	gm_{EA}	0.8	1.2	1.6	mS	V_{FB} = 1.2V
5.6.6	Error amplifier, output resistance	$R_{EA,OUT}$	1.0	–	–	MΩ	V_{FB} = 1.2V; V_{COMP} = 1.2V
5.6.7	Error amplifier, ramp amplitude, FREQ-mode	$V_{Comp,peak\ to\ peak,FREQ}$	1.0	–	1.6	V	V_{FB} = 1.2V; FREQ-mode; f_{FREQ} = 100 -700kHz; Monitor LG
5.6.8	Error amplifier, ramp amplitude, SYNC-mode	$V_{Comp,peak\ to\ peak,SYNC}$	0.6	–	2.6	V	V_{FB} = 1.2V; SYNC-mode; f_{SYNC} = 350 -700kHz; Monitor LG
5.6.9	Error amplifier output, source and sink current	$I_{Comp,max}$	150	280	450	µA	Source current: V_{FB} = 0.8V, V_{COMP}= 2.5V; Sink current: V_{FB} = 2.4V, V_{COMP}= 2.5V
5.6.10	Comp pin, minimum voltage	$V_{Comp,min}$	0.8	–	–	V	V_{COMP} increasing; Monitor UG
5.6.11	Bootstrap under voltage lockout threshold for UG turn-off	$V_{BTS,off}$	V_{BUO} + 3.0	–	–	V	V_{BTS_BUO} voltage decreasing
5.6.12	Bootstrap under voltage lockout, hysteresis	$V_{BTS,hyst}$	–	300	–	mV	–
5.6.13	Bootstrap capacitor discharge current	I_{BTS_BUO}	–	150	–	µA	V_{BTS_BUO} = 4.5V
5.6.14	Bootstrap diode forward voltage	$V_{DBTS,fwd}$	–	0.8	–	V	I_{DBTS} = 20mA
5.6.15	Minimum on time Upper Gate	$T_{UGON,min}$	–	100	–	ns	1)
5.6.16	Minimum off time Upper Gate	$T_{UGOFF,min}$	–	100	–	ns	1)
5.6.17	Soft start ramp	t_{start}	–	512 x 1/f	–	µs	f = f_{FREQ}, FREQ-mode; f = f_{SYNC}, SYNC-mode
5.6.18	Input under voltage shutdown threshold	$V_{S,off}$	3.7	–	–	V	V_S decreasing

Electrical Characteristics:

V_S = 6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.6.19	Input voltage startup threshold	$V_{S,on}$	–	–	4.75	V	V_S increasing
5.6.20	Input under voltage shutdown hysteresis	$V_{S,hyst}$	–	300	–	mV	–
Gate Driver for upper Switch							
5.6.21	Upper Gate Driver Peak Sourcing Current	$I_{UG,SRC}$	–	-380	–	mA	V_{UG} = 3.5V; 1)
5.6.22	Upper Gate Driver Peak Sinking Current	$I_{UG,SNK}$	–	550	–	mA	V_{UG} = 1.5V; 1)
5.6.23	Upper Gate Driver Output Rise Time	$t_{R,UG}$	–	30	60	ns	$C_{L,UG}$ = 3.3nF; V_{UG} = 1V to 4V
5.6.24	Upper Gate Driver Output Fall Time	$t_{F,UG}$	–	20	40	ns	$C_{L,UG}$ = 3.3nF; V_{UG} = 1V to 4V
5.6.25	Upper Gate Driver Output Voltage	V_{UG}	–	4.4	5.2	V	$C_{L,UG}$ = 3.3nF
Gate Driver for lower Switch							
5.6.26	Lower Gate Driver Peak Sourcing Current	$I_{LG,SRC}$	–	-380	–	mA	V_{LG} = 3.5V; 1)
5.6.27	Lower Gate Driver Peak Sinking Current	$I_{LG,SNK}$	–	550	–	mA	V_{LG} = 1.5V; 1)
5.6.28	Lower Gate Driver Output Rise Time	$t_{R,LG}$	–	30	60	ns	$C_{L,LG}$ = 3.3nF; V_{LG} = 1V to 4V
5.6.29	Lower Gate Driver Output Fall Time	$t_{F,LG}$	–	20	40	ns	$C_{L,LG}$ = 3.3nF; V_{LG} = 1V to 4V
5.6.30	Lower Gate Driver Output Voltage	V_{LG}	5.05	5.40	5.75	V	$C_{L,LG}$ = 3.3nF; $V_S \geq$ 7V
5.6.31	Overcurrent limitation	$I_{OC\_lim,ref}$	89	95	101	µA	V_{COMP} = 3V sensehigh-senselow decreasing; monitor max current on sensehigh
5.6.32	Overcurrent comparator offset voltage	$V_{OCComp,Offset}$	-15	–	+15	mV	V_{FB} = 1V; V_{COMP} = 4V; sensehigh-senselow increasing

1) Not subject to production test, specified by design.

6 Module Oscillator

6.1 Description

The oscillator supplies the device with a constant frequency. When the device is not operating in pulse skipping mode, the external MOSFETs are switched on and off with the same constant frequency. Some safety functions are synchronized also to this frequency.

The internal oscillator is used to determine the switching frequency of the buck regulator. The switching frequency can be selected from 100 kHz to 700 kHz with an external resistor connected at pin SYNC/FREQ to GND. To set the switching frequency with an external resistor the following formula can be applied

$$R_{FREQ} = \frac{1}{\left(149 \times 10^{-12}\left[\frac{s}{\Omega}\right]\right) \times \left(f_{FREQ}\left[\frac{1}{s}\right]\right)} - \left(2.0 \times 10^{3}\left[\Omega\right]\right)\left[\Omega\right]$$

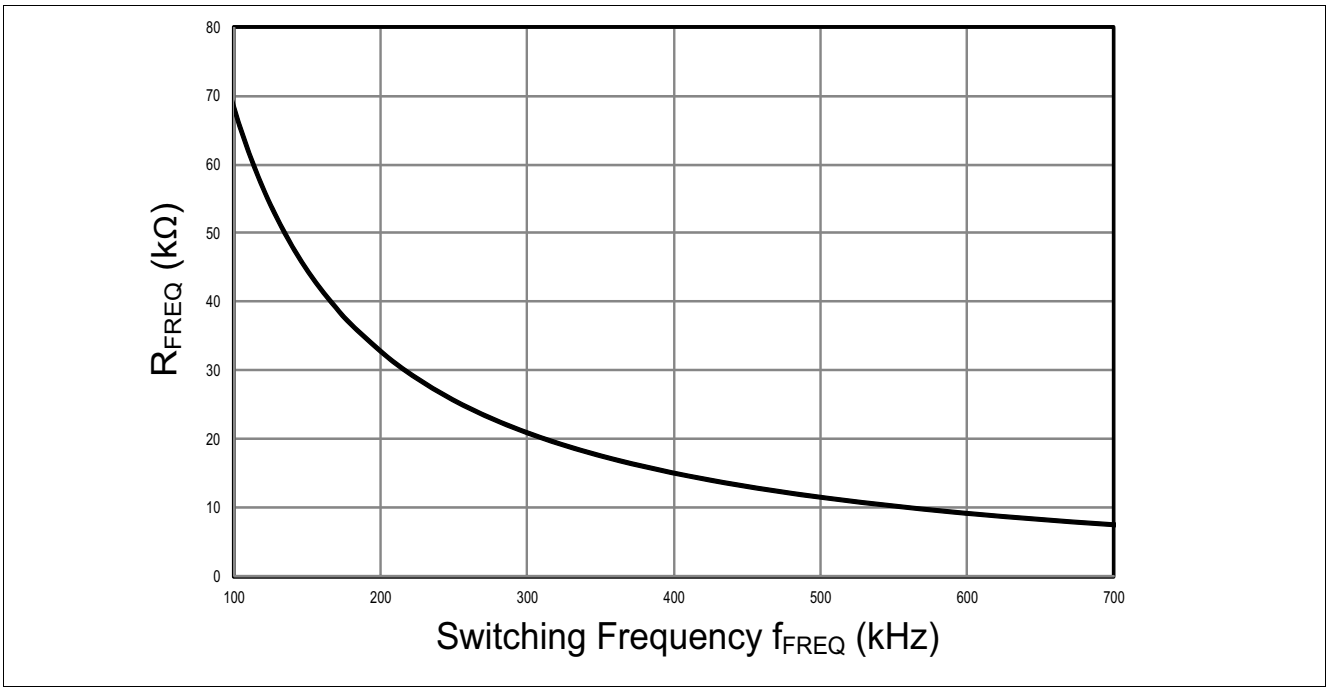


Figure 10 Resistor R_{FREQ} versus Switching Frequency f_{FREQ}

The turn-on frequency can optionally be set externally via the pin SYNC/FREQ. In this case the synchronization of the PWM-on signal refers to the falling edge of the pin SYNC/FREQ input signal.

6.2 Electrical Characteristics Module Oscillator

Electrical Characteristics: Module Oscillator

V_S = 6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Oscillator:							
6.2.1	Oscillator Frequency	f_{FREQ}	250	300	350	kHz	R_{FREQ} = 20kΩ
6.2.2	Oscillator Frequency Adjustment Range	f_{FREQ}	100	–	700	kHz	17% internal tolerance + external resistor tolerance
6.2.3	FREQ Supply Current	I_{FREQ}	–	–	800	µA	V_{FREQ} = 0 V
Synchronization							
6.2.4	Synchronization Frequency Capture Range	f_{SYNC}	350	–	700	kHz	1)
6.2.5	Synchronization Signal Duty cycle	D_{SYNC}	20		80	%	
6.2.6	Synchronization Signal High Logic Level Valid	$V_{SYNC,H}$	3.0	–	–	V	2)
6.2.7	Synchronization Signal Low Logic Level Valid	$V_{SYNC,L}$	–	–	0.8	V	2)

1) Synchronization frequency out of the specified range leads to complete malfunction of the device

2) Synchronization of external UG ON signal to falling edge

7 Linear Regulator

7.1 Description

The internal linear voltage regulator supplies the low-side gate driver directly (typical voltage 5.4 V) and through a diode the high-side gate driver. The current capability is up to 50 mA. An external output capacitor with low ESR is required on pin IVCC for stability and buffering transient load currents. During normal operation the gate drivers will draw transient currents from the linear regulator and its output capacitor. Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFETs. An integrated power-on reset circuit monitors the linear regulator output voltage and resets the device in case the output voltage falls below the power-on reset threshold. The power-on reset helps protect the external MOSFETs from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of an external logic level n-channel MOSFET. For IVCC voltage lower than 5V the proper charging of the bootstrap capacitor is not guaranteed.

The internal linear voltage regulator is implemented to supply the gate drivers, therefore a large voltage ripple may be present on this output due to the pulsed current sinked by internal drivers and bootstrap diode. This output should not be used to supply loads than the internal ones.

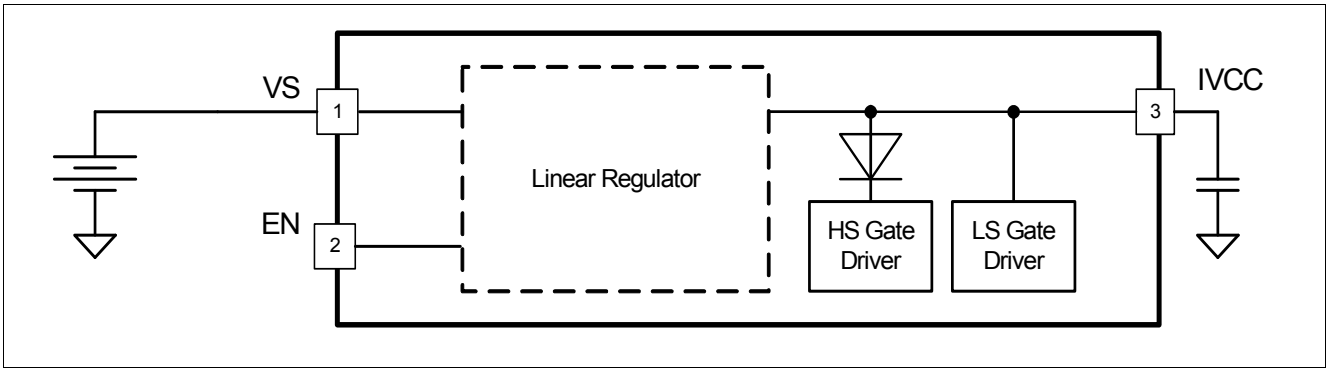


Figure 11 Linear Regulator Block Diagram and Simplified Application Circuit

7.2 Electrical Characteristics

Electrical Characteristics: Linear Regulator

V_S = 6V to 40V; T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
7.2.1	Output Voltage	V_{IVCC}	5.05	5.4	5.75	V	7 V ≤ V_S ≤ 40 V; 0.1 mA ≤ I_{IVCC} ≤ 50 mA
7.2.2	Output Current Limitation	I_{LIM}	51		110	mA	V_S = 13.5 V; V_{IVCC} = 5.1V
7.2.3	Drop out Voltage	V_{DR}			800	mV	I_{IVCC} = 50mA [1]
7.2.4	Output Capacitor	C_{IVCC}	0.47		3	µF	[2]
7.2.5	Output Capacitor ESR	$R_{IVCC,ESR}$			0.5	Ω	f = 10kHz
7.2.6	Undervoltage Reset Headroom	$V_{IVCC,HDRM}$	100	–	–	mV	V_{IVCC} decreasing; V_{IVCC} - $V_{IVCC,RTH,d}$
7.2.7	Undervoltage Reset Threshold	$V_{IVCC,RTH,d}$	4.0	–	–	V	V_{IVCC} decreasing
7.2.8	Undervoltage Reset Threshold	$V_{IVCC,RTH,i}$	–	–	4.5	V	V_{IVCC} increasing

1) Measured when the output voltage V_{IVCC} has dropped 100 mV from its nominal value.

2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum.

8 Module Enable and Thermal Shutdown

8.1 Description

With the enable pin the device can be set in off-state reducing the current consumption to less than 2µA.

The enable function features an integrated pull down resistor which ensures that the IC is shut down and the external MOSFETs are off in case the pin EN is left open.

The integrated thermal shutdown function turns the external MOSFETs off in case of overtemperature. The typical junction shutdown temperature is 175°C, with a minimum of 160°C. After cooling down, the IC will automatically restart with soft start. The thermal shutdown is an integrated protection function designed to prevent IC destruction when operating under fault conditions.

8.2 Electrical Characteristics Module Enable, Bias and Thermal Shutdown

Electrical Characteristics: Enable, Bias and Thermal Shutdown

V_S = 6.0 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.2.1	Current Consumption, shut down mode	$I_{q,OFF}$	–	0.1	2	µA	V_{EN} = 0.8V; T_j < 105°C; V_s = 16V
8.2.2	Current Consumption, active mode	$I_{q,ON}$	–	3	10	mA	V_{EN} = 5.0V; I_{IVCC}= 0mA; V_S = 16V
8.2.3	Enable high signal valid	$V_{EN,lo}$	3.0	–	–	V	–
8.2.4	Enable low signal valid	$V_{EN,hi}$	–	–	0.8	V	–
8.2.5	Enable hysteresis	$V_{EN,HY}$	200	300	400	mV	
8.2.6	Enable high input current	$I_{EN,hi}$	–	–	30	µA	V_{EN} = 16V
8.2.7	Enable low input current	$I_{EN,lo}$	–	0.1	1	µA	V_{EN} = 0.5V
8.2.8	Over temperature shutdown	$T_{j,sd}$	160	175	190	°C	1)
8.2.9	Over temperature shutdown hysteresis	T_{j,sd_hyst}	–	15	–	K	1)

1) Not subject to production test, specified by design.

9 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

9.1 Application Diagram

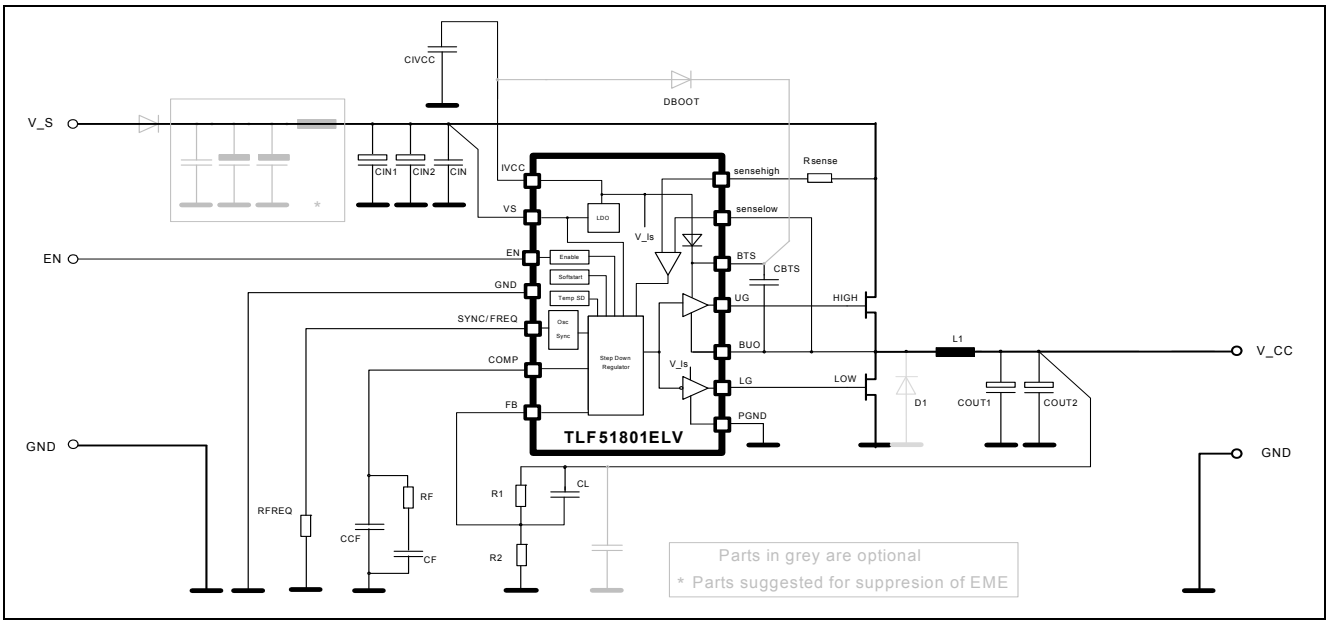


Figure 12 Application Diagram (Current limitation with Rdson-configuration)

Note: This is a very simplified example of an application circuit. The function must be verified in the real application

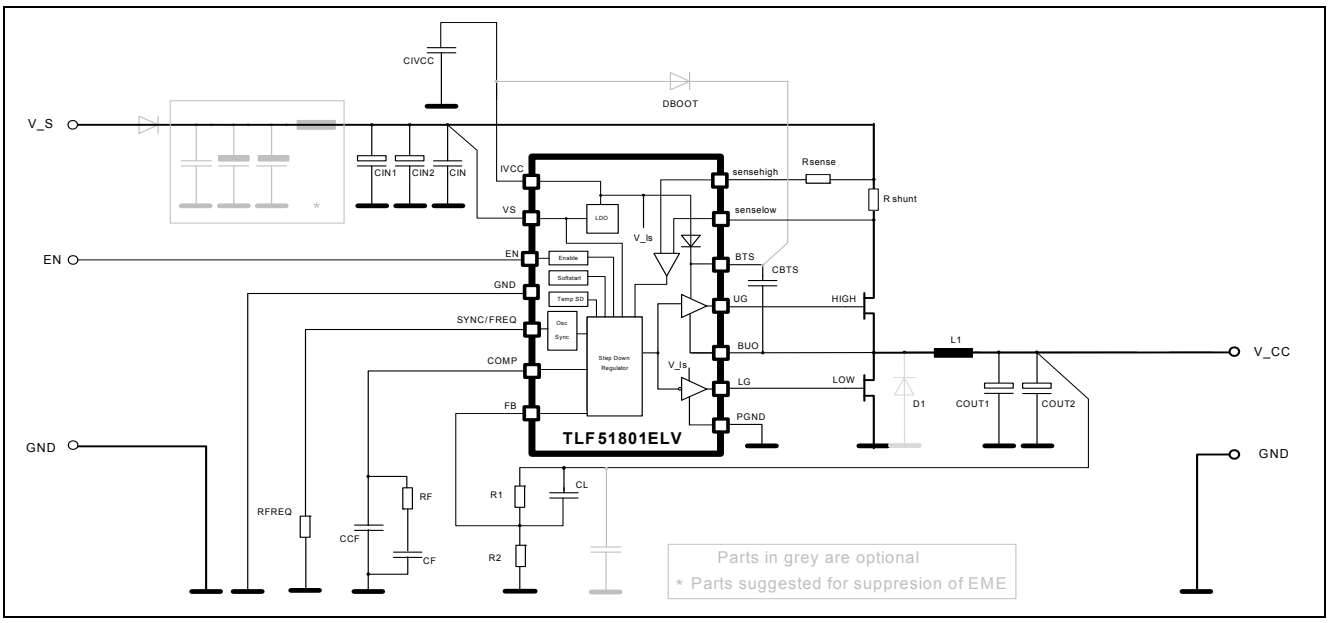


Figure 13 Application Diagram (Current limitation with Shunt-configuration)

Note: This is a very simplified example of an application circuit. The function must be verified in the real application

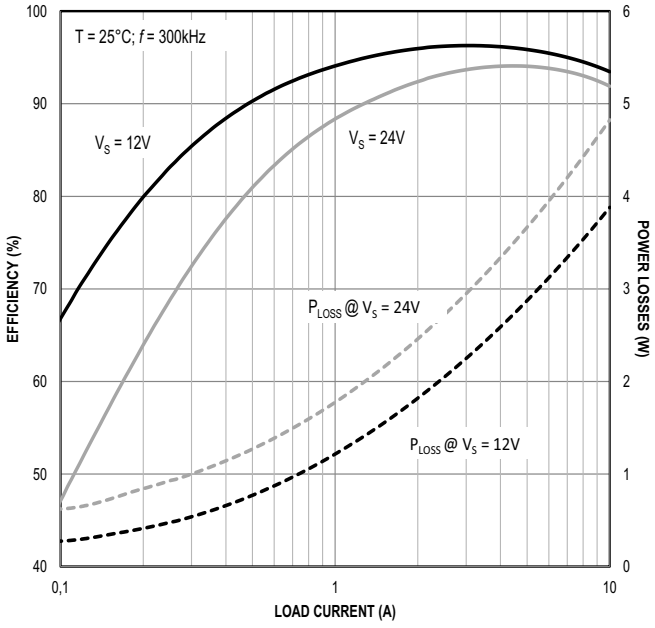
Ref	Value	Manufacturer	Part number	Type	Qty
L_1	5.6µH	Coilcraft	MSS1278T-562ML_	Inductor	1
LOW, HIGH	N-ch, 60 V, 12 mΩ	Infineon	IPD50N06S4L-12	Transistor	2
C_{OUT1}, C_{OUT2}	100µF - 10mΩ ESR	Rubycon	6SW100M	Capacitor, Poly Al, 6.3V	2
C_{IN2}	22µF	Kemet	C2220C226M5R2CTU	Capacitor, X7R, 50V	1
C_{IN1}	470µF	Panasonic	EEEFK1H471AM	Capacitor, Al, 50V	1
R_{FREQ}	20kΩ	Panasonic	ERJ3EKF2002V	Resistor, ±1%, 0.1W	1
R_1	100kΩ	Panasonic	ERJ3EKF1003V	Resistor, ±1%, 0.1W	1
R_2	27.3kΩ	Panasonic	ERJ3EKF2742V	Resistor, ±1%, 0.1W	1
R_F	6.65kΩ	Panasonic	ERJ3EKF6651V	Resistor, ±1%, 0.1W	1
R_{sense}	1.1kΩ	Panasonic	ERJ3EKF1101V	Resistor, ±1%, 0.1W	1
R_{shunt}	10mΩ	Vishay Dale	WSL3637R0100FEB	Resistor, ±1%, 3W	1
C_{CF}	12pF	Kemet	C0603C120J5GACTU	Capacitor, C0G	1
C_L	120pF	Kemet	C0603C121J5GACTU	Capacitor, C0G	1
C_F	15nF	Kemet	C0603C153K5RACTU	Capacitor, X7R, 50V	1
C_{IVCC}	1µF	Kemet	C1206C105K4RACTU	Capacitor, X7R, 16V	1
C_{IN}	1µF	Kemet	C1206C105K5RACTU	Capacitor, X7R, 50V	1
C_{BTS}	270nF	Kemet	C1206C273K5RACTU	Capacitor, X7R, 50V	1

Figure 14 Bill of Material for Application Diagram

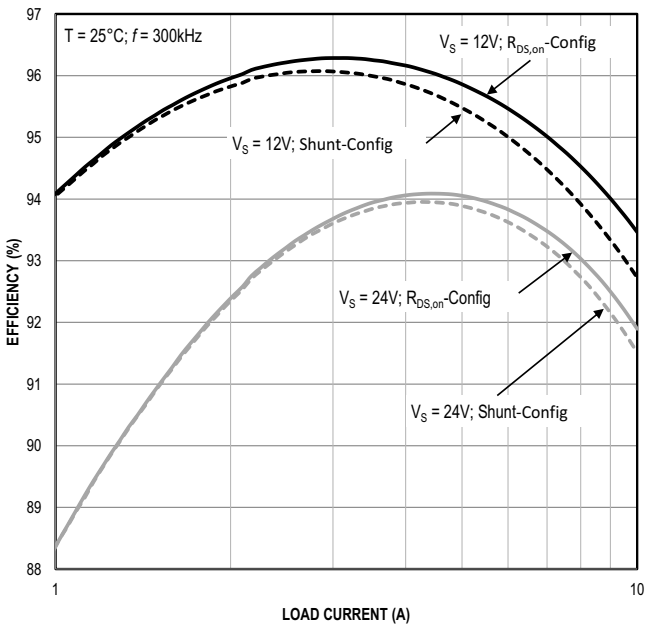
10 Performance Graphs

Typical Performance Characteristics

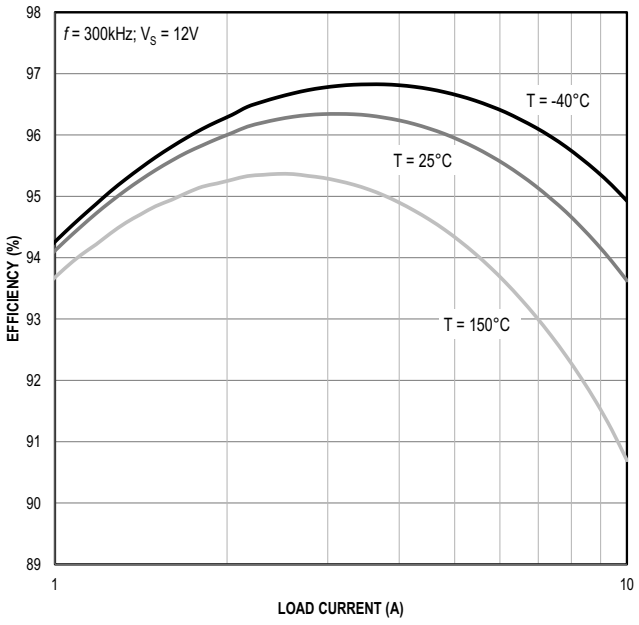
Efficiency and Power Losses versus Load Current



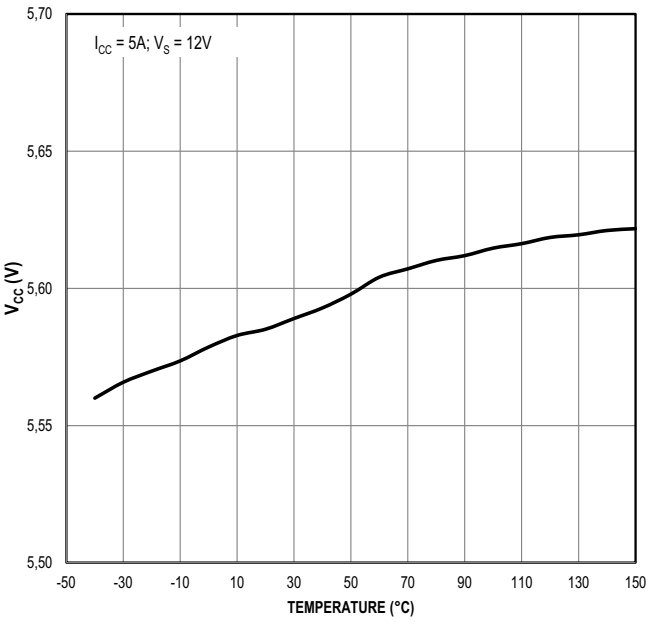
Efficiency versus Load Current



Efficiency versus Load Current

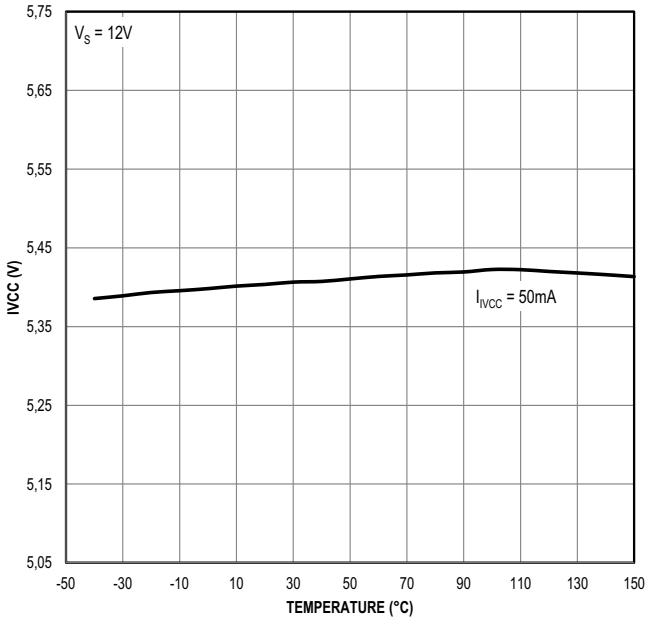


V_{CC} versus Temperature

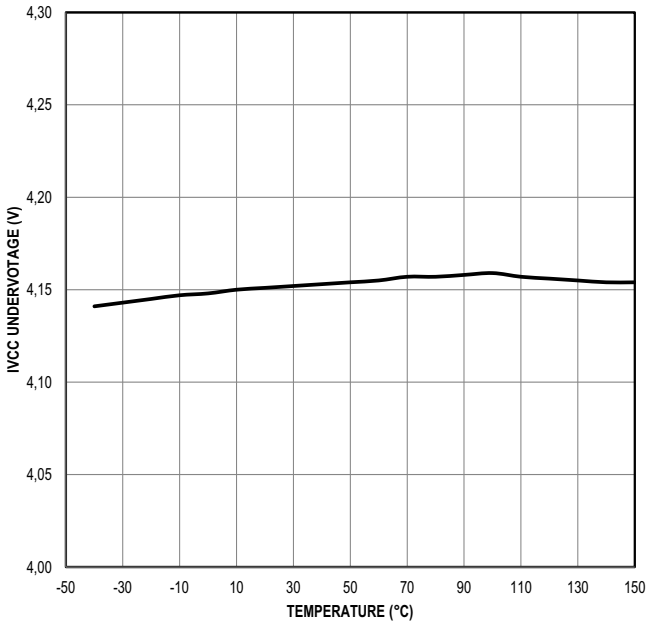


Typical Performance Characteristics

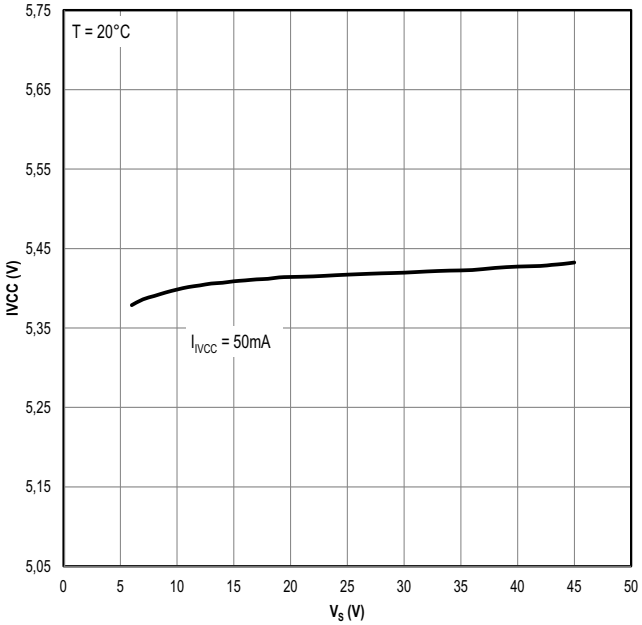
IVCC versus Temperature



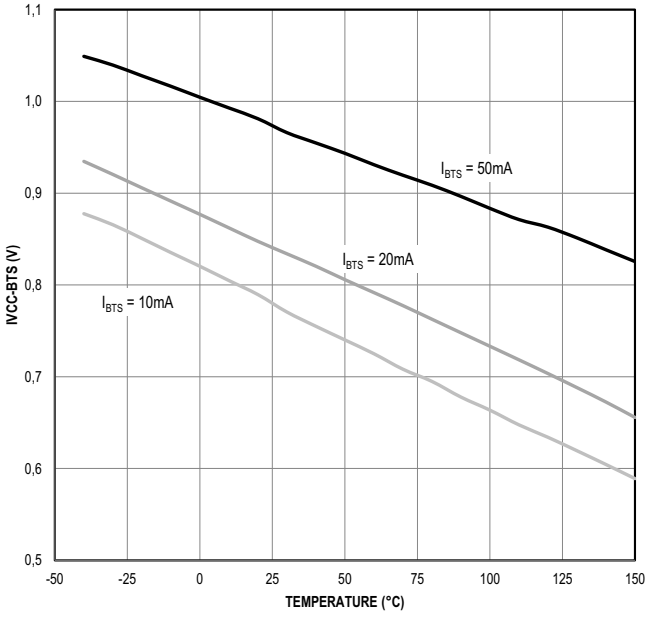
IVCC Undervoltage versus Temperature



IVCC versus V_S

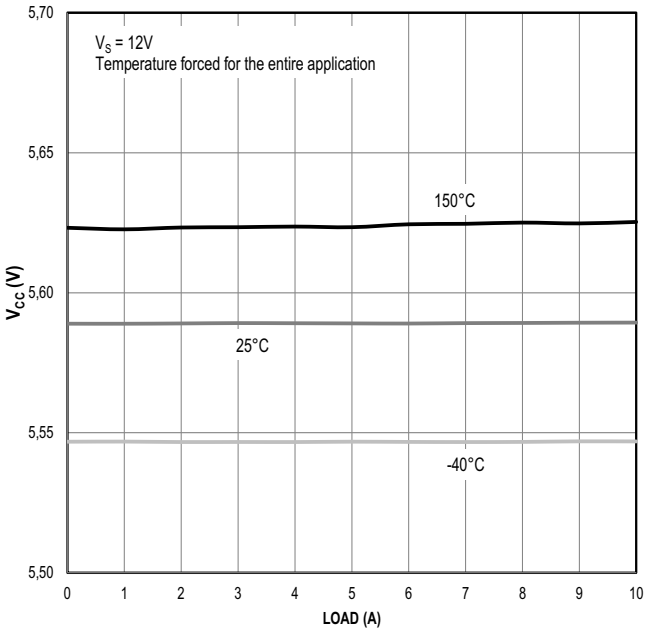


Bootstrap Diode drop versus Temperature

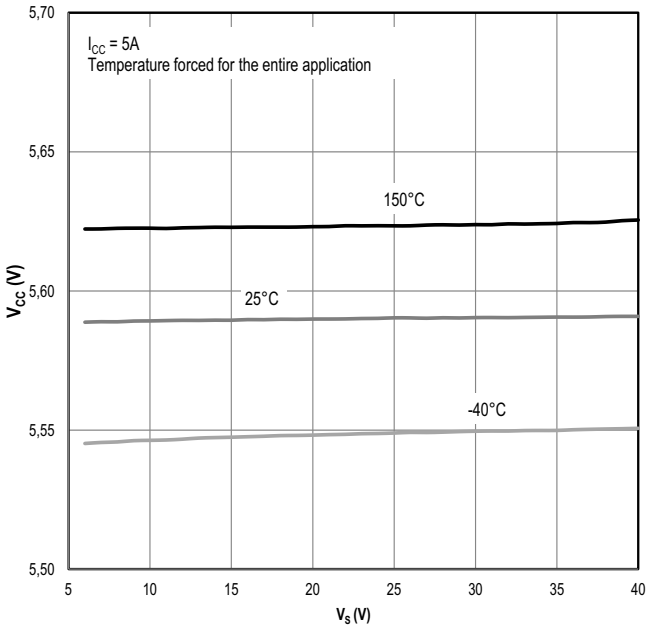


Typical Performance Characteristics

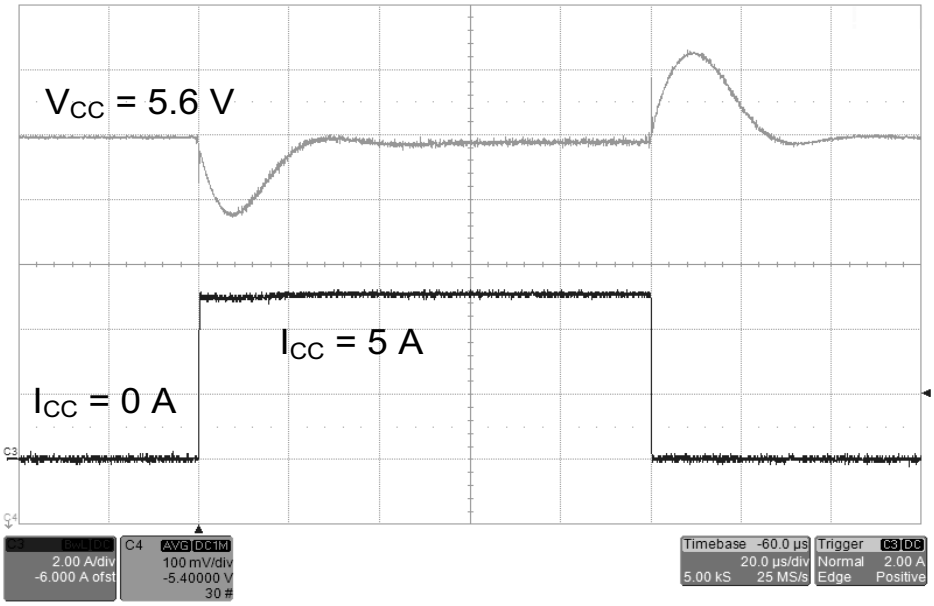
Load Regulation
V_S = 12 V



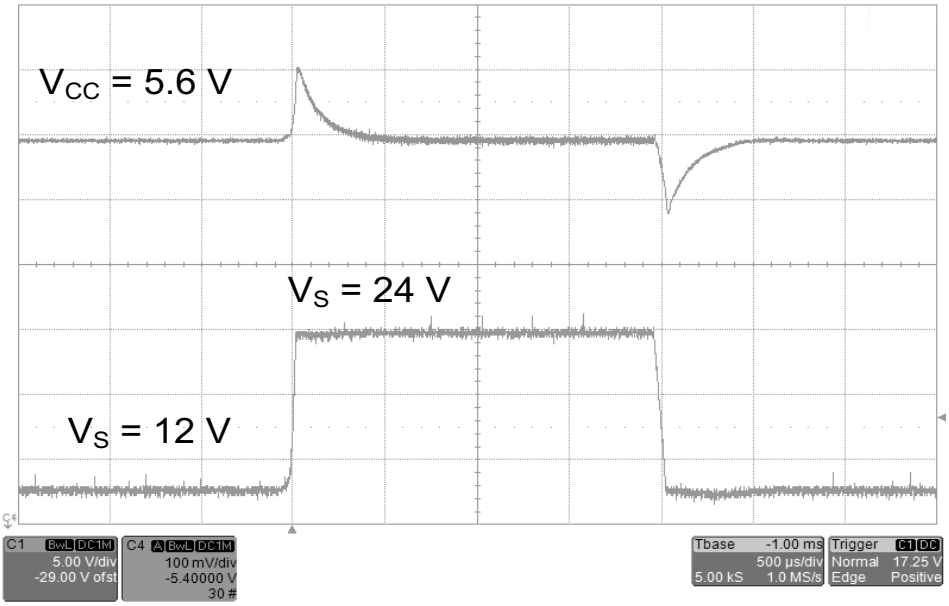
Line Regulation
I_{CC} = 5 A



Load Step
V_S = 12 V



Line Step
I_{CC} = 5 A



11 Package Outlines

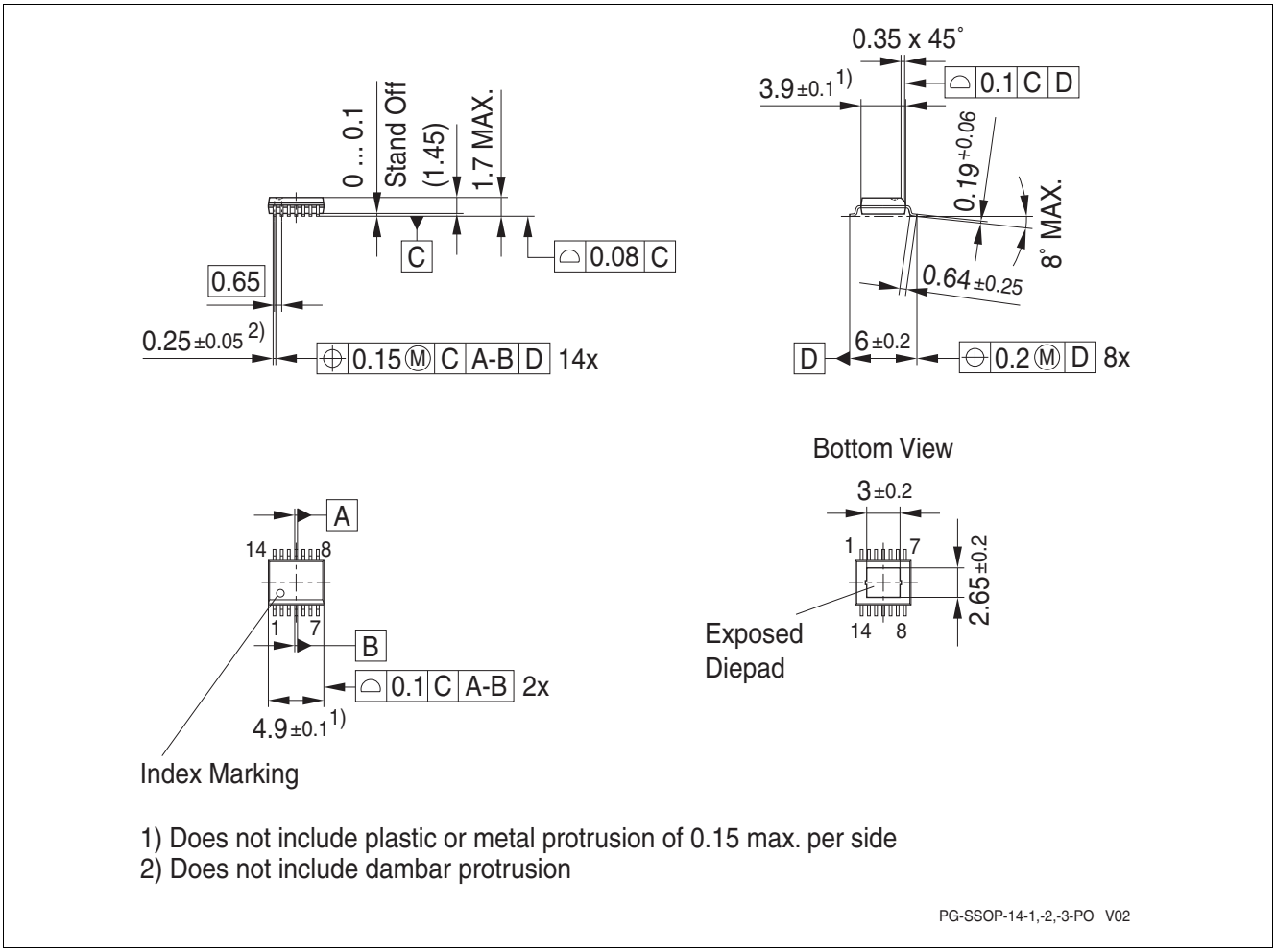


Figure 15 Package Drawing

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further package information, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

12 Revision History

Version	Date	Changes
Rev 1.0.1	2013-04-15	Page 21: Editorial change
Rev 1.0	2013-02-25	Initial data sheet

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