PCA9955B

16-channel Fm+ I²C-bus 57 mA/20 V constant current LED driver

Rev. 2.1 — 2 May 2017 Product data sheet

1. General description

The PCA9955B is an I²C-bus controlled 16-channel constant current LED driver optimized for dimming and blinking 57 mA Red/Green/Blue/Amber (RGBA) LEDs in amusement products. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 31.25 kHz with a duty cycle that is adjustable from 0 % to 100 % to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 122 Hz and an adjustable frequency between 15 Hz to every 16.8 seconds with a duty cycle that is adjustable from 0 % to 99.6 % that is used to either dim or blink all LEDs with the same value.

Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The PCA9955B operates with a supply voltage range of 3 V to 5.5 V and the constant current sink LED outputs allow up to 20 V for the LED supply. The output peak current is adjustable with an 8-bit linear DAC from 225 μA to 57 mA.

Gradation control for all current sources is achieved via the I²C-bus serial interface and allows user to ramp current automatically without MCU intervention. 8-bit DACs are available to adjust brightness levels for each LED current source. There are four selectable gradation control groups and each group has independently four registers to control ramp-up and ramp-down rate, step time, hold ON/OFF time and final hold ON output current. Two gradation operation modes are available for each group, one is single shot mode (output pattern once) and the other is continuous mode (output pattern repeat). Each channel can be set to either gradation mode or normal mode and assigned to any one of these four gradation control groups.

This device has built-in open, short load and overtemperature detection circuitry. The error information from the corresponding register can be read via the I²C-bus. Additionally, a thermal shutdown feature protects the device when internal junction temperature exceeds the limit allowed for the process.

The PCA9955B device has a Fast-mode Plus (Fm+) I²C-bus interface. Fm+ devices offer higher frequency (up to 1 MHz) or more densely populated bus operation (up to 4000 pF).

The active LOW output enable input pin ($\overline{OE}$) blinks all the LED outputs and can be used to externally PWM the outputs, which is useful when multiple devices need to be dimmed or blinked together without using software control.

Software programmable LED Group and three Sub Call I²C-bus addresses allow all or defined groups of PCA9955B devices to respond to a common I²C-bus address, allowing for example, all red LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I²C-bus commands. On power-up, PCA9955B has a unique

Sub Call address to identify it as a 16-channel LED driver. This unique address allows mixing of devices with different channel widths. Three hardware address pins on PCA9955B allow up to 125 devices on the same bus.

The Software Reset (SWRST) function allows the master to perform a reset of the PCA9955B through the I²C-bus, identical to the Power-On Reset (POR) that initializes the registers to their default state causing the output current switches to be OFF (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

2. Features and benefits

- 16 LED drivers. Each output programmable at:
  - Off
  - On
  - Programmable LED brightness
  - Programmable group dimming/blinking mixed with individual LED brightness
  - Programmable LED output delay to reduce EMI and surge currents
- Gradation control for all channels
  - Each channel can assign to one of four gradation control groups
  - Programmable gradation time and rate for ramp-up and/or ramp-down operations
  - Programmable step time (6-bit) from 0.5 ms (minimum) to 512 ms (maximum)
  - Programmable hold-on time after ramp-up and hold-off time after ramp-down (3-bit) from 0 s to 6 s
  - Programmable final ramp-up and hold-on current
  - Programmable brightness current output adjustment, either linear or exponential curve
- 16 constant current output channels can sink up to 57 mA, tolerate up to 20 V when OFF
- Output current adjusted through an external resistor (REXT input)
- Output current accuracy
  - ±4 % between output channels
  - ±6 % between PCA9955B devices
- Open/short load/overtemperature detection mode to detect individual LED errors
- 1 MHz Fast-mode Plus compatible I²C-bus interface with 30 mA high drive capability on SDA output for driving high capacitive buses
- 256-step (8-bit) linear programmable brightness per LED output varying from fully off (default) to maximum brightness fully ON using a 31.25 kHz PWM signal
- 256-step group brightness control allows general dimming (using a 122 Hz PWM signal) from fully off to maximum brightness (default)
- 256-step group blinking with frequency programmable from 15 Hz to 16.8 s and duty cycle from 0 % to 99.6 %
- Output state change programmable on the Acknowledge or the STOP condition to update outputs byte-by-byte or all at the same time (default to ‘Change on STOP’).
- Active LOW Output Enable ($\overline{OE}$) input pin allows for hardware blinking and dimming of the LEDs

- Three quinary hardware address pins allow 125 PCA9955B devices to be connected to the same I²C-bus and to be individually programmed
- 4 software programmable I²C-bus addresses (one LED Group Call address and three LED Sub Call addresses) allow groups of devices to be addressed at the same time in any combination (for example, one register used for 'All Call' so that all the PCA9955Bs on the I²C-bus can be addressed at the same time and the second register used for three different addresses so that 1⁄3 of all devices on the bus can be addressed at the same time in a group). Software enable and disable for each programmable I²C-bus address.
- Unique power-up default Sub Call address allows mixing of devices with different channel widths
- Software Reset feature (SWRST Call) allows the device to be reset through the I²C-bus
- 8 MHz internal oscillator requires no external components
- Internal power-on reset
- Noise filter on SDA/SCL inputs
- No glitch on LEDn outputs on power-up
- Low standby current
- Operating power supply voltage (V_{DD}) range of 3 V to 5.5 V
- 5.5 V tolerant inputs on non-LED pins
- −40 °C to +105 °C operation
- ESD protection exceeds 4000 V HBM per JESD22-A114
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: HTSSOP28

3. Applications

- Amusement products
- RGB or RGBA LED drivers
- LED status information
- LED displays
- LCD backlights
- Keypad backlights for cellular phones or handheld devices
- Fade-in and fade-out for breathlight control
- Automotive lighting (PCA9955BTW/Q900)

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9955BTW	PCA9955BTW	HTSSOP28	plastic thermal enhanced thin shrink small outline package; 28 leads; body width 4.4 mm; lead pitch 0.65 mm; exposed die pad	SOT1172-3
PCA9955BTW/Q900[1]	PCA9955BTW	HTSSOP28	plastic thermal enhanced thin shrink small outline package; 28 leads; body width 4.4 mm; lead pitch 0.65 mm; exposed die pad	SOT1172-3

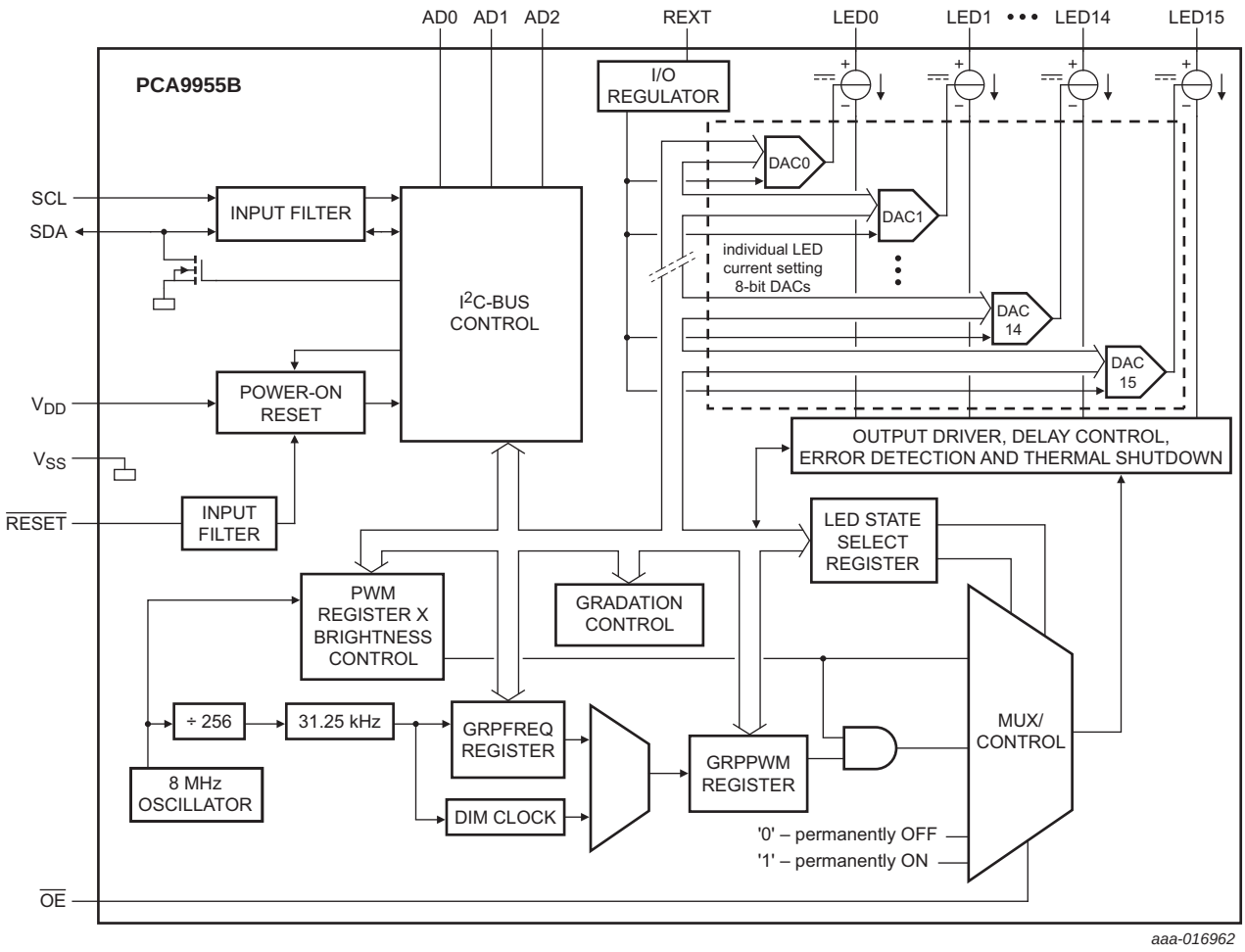
[1] PCA9955BTW/Q900 is AEC-Q100 compliant.

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9955BTW	PCA9955BTWJ	HTSSOP28	Reel 13” Q1/T1 *Standard mark SMD	2500	T_{amb} = –40 °C to +105 °C
PCA9955BTW/Q900	PCA9955BTW/Q900J	HTSSOP28	Reel 13” Q1/T1 *Standard mark SMD	2500	T_{amb} = –40 °C to +105 °C

5. Block diagram



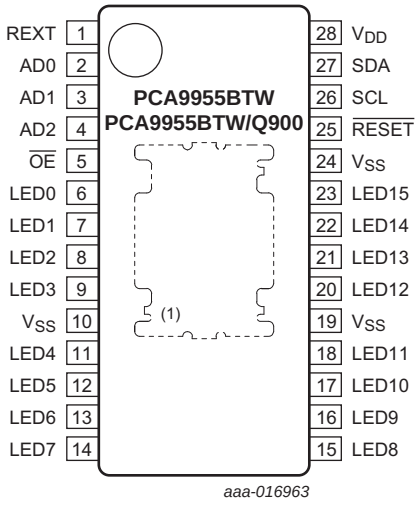
Dim repetition rate = 122 Hz

Blink repetition rate = 15 Hz to every 16.8 seconds

Fig 1. Block diagram of PCA9955B

6. Pinning information

6.1 Pinning



(1) Thermal pad; connected to V_{SS}

Fig 2. Pin configuration for HTSSOP28

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
REXT	1	I	current set resistor input; resistor to ground
AD0	2	I	address input 0
AD1	3	I	address input 1
AD2	4	I	address input 2
$\overline{OE}$	5	I	active LOW output enable for LEDs
LED0	6	O	LED driver 0
LED1	7	O	LED driver 1
LED2	8	O	LED driver 2
LED3	9	O	LED driver 3
LED4	11	O	LED driver 4
LED5	12	O	LED driver 5
LED6	13	O	LED driver 6
LED7	14	O	LED driver 7
LED8	15	O	LED driver 8
LED9	16	O	LED driver 9
LED10	17	O	LED driver 10
LED11	18	O	LED driver 11
LED12	20	O	LED driver 12
LED13	21	O	LED driver 13
LED14	22	O	LED driver 14
LED15	23	O	LED driver 15
$\overline{RESET}$	25	I	active LOW reset input with external 10 kΩ pull-up resistor
SCL	26	I	serial clock line
SDA	27	I/O	serial data line
V_{SS}	10, 19, 24 [1]	ground	supply ground
V_{DD}	28	power supply	supply voltage

[1] HTSSOP28 package supply ground is connected to both V_{SS} pins and exposed center pad. V_{SS} pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad must be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias must be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

Refer to Figure 1 “Block diagram of PCA9955B”.

7.1 Device addresses

Following a START condition, the bus master must output the address of the slave it is accessing.

For PCA9955B there are a maximum of 125 possible programmable addresses using the three quinary hardware address pins.

7.1.1 Regular I²C-bus slave address

The I²C-bus slave address of the PCA9955B is shown in Figure 3. The 7-bit slave address is determined by the quinary input pads AD0, AD1 and AD2. Each pad can have one of five states (GND, pull-up, floating, pull-down, and V_{DD}) based on how the input pad is connected on the board. At power-up or hardware/software reset, the quinary input pads are sampled and set the slave address of the device internally. To conserve power, once the slave address is determined, the quinary input pads are turned off and will not be sampled until the next time the device is power cycled. Table 4 lists the five possible connections for the quinary input pads along with the external resistor values that must be used.

Table 4. Quinary input pad connection

Pad connection (pins AD2, AD1, AD0)[1]	Mnemonic	External resistor (kΩ)	
		Min.	Max.
tie to ground	GND	0	17.9
resistor pull-down to ground	PD	34.8	270
open (floating)	FLT	503	∞
resistor pull-up to V_{DD}	PU	31.7	340
tie to V_{DD}	V_{DD}	0	22.1

[1] These AD[2:0] inputs must be stable before the supply V_{DD} to the chip.

Table 5 lists all 125 possible slave addresses of the device based on all combinations of the five states connected to three address input pins AD0, AD1 and AD2.

Table 5. I²C-bus slave address

Hardware selectable input pins			I²C-bus slave address for PCA9955B			
AD2	AD1	AD0	Decimal	Hexadecimal	Binary (A[6:0])	Address (R/$\overline{W}$ = 0)
GND	GND	GND	1	01	0000001[1]	02h
GND	GND	PD	2	02	0000010[1]	04h
GND	GND	FLT	3	03	0000011[1]	06h
GND	GND	PU	4	04	0000100[1]	08h
GND	GND	V_{DD}	5	05	0000101[1]	0Ah
GND	PD	GND	6	06	0000110[1]	0Ch
GND	PD	PD	7	07	0000111[1]	0Eh

Table 5. I²C-bus slave address *…continued*

Hardware selectable input pins			I²C-bus slave address for PCA9955B			
AD2	**AD1**	**AD0**	**Decimal**	**Hexadecimal**	**Binary (A[6:0])**	**Address (R/$\overline{W}$ = 0)**
GND	PD	FLT	8	08	0001000	10h
GND	PD	PU	9	09	0001001	12h
GND	PD	V_{DD}	10	0A	0001010	14h
GND	FLT	GND	11	0B	0001011	16h
GND	FLT	PD	12	0C	0001100	18h
GND	FLT	FLT	13	0D	0001101	1Ah
GND	FLT	PU	14	0E	0001110	1Ch
GND	FLT	V_{DD}	15	0F	0001111	1Eh
GND	PU	GND	16	10	0010000	20h
GND	PU	PD	17	11	0010001	22h
GND	PU	FLT	18	12	0010010	24h
GND	PU	PU	19	13	0010011	26h
GND	PU	V_{DD}	20	14	0010100	28h
GND	V_{DD}	GND	21	15	0010101	2Ah
GND	V_{DD}	PD	22	16	0010110	2Ch
GND	V_{DD}	FLT	23	17	0010111	2Eh
GND	V_{DD}	PU	24	18	0011000	30h
GND	V_{DD}	V_{DD}	25	19	0011001	32h
PD	GND	GND	26	1A	0011010	34h
PD	GND	PD	27	1B	0011011	36h
PD	GND	FLT	28	1C	0011100	38h
PD	GND	PU	29	1D	0011101	3Ah
PD	GND	V_{DD}	30	1E	0011110	3Ch
PD	PD	GND	31	1F	0011111	3Eh
PD	PD	PD	32	20	0100000	40h
PD	PD	FLT	33	21	0100001	42h
PD	PD	PU	34	22	0100010	44h
PD	PD	V_{DD}	35	23	0100011	46h
PD	FLT	GND	36	24	0100100	48h
PD	FLT	PD	37	25	0100101	4Ah
PD	FLT	FLT	38	26	0100110	4Ch
PD	FLT	PU	39	27	0100111	4Eh
PD	FLT	V_{DD}	40	28	0101000	50h
PD	PU	GND	41	29	0101001	52h
PD	PU	PD	42	2A	0101010	54h
PD	PU	FLT	43	2B	0101011	56h
PD	PU	PU	44	2C	0101100	58h
PD	PU	V_{DD}	45	2D	0101101	5Ah
PD	V_{DD}	GND	46	2E	0101110	5Ch
PD	V_{DD}	PD	47	2F	0101111	5Eh

Table 5. I²C-bus slave address *…continued*

Hardware selectable input pins			I²C-bus slave address for PCA9955B			
AD2	**AD1**	**AD0**	**Decimal**	**Hexadecimal**	**Binary (A[6:0])**	**Address (R/$\overline{W}$ = 0)**
PD	V_{DD}	FLT	48	30	0110000	60h
PD	V_{DD}	PU	49	31	0110001	62h
PD	V_{DD}	V_{DD}	50	32	0110010	64h
FLT	GND	GND	51	33	0110011	66h
FLT	GND	PD	52	34	0110100	68h
FLT	GND	FLT	53	35	0110101	6Ah
FLT	GND	PU	54	36	0110110	6Ch
FLT	GND	V_{DD}	55	37	0110111	6Eh
FLT	PD	GND	56	38	0111000	70h
FLT	PD	PD	57	39	0111001	72h
FLT	PD	FLT	58	3A	0111010	74h
FLT	PD	PU	59	3B	0111011	76h
FLT	PD	V_{DD}	60	3C	0111100	78h
FLT	FLT	GND	61	3D	0111101	7Ah
FLT	FLT	PD	62	3E	0111110	7Ch
FLT	FLT	FLT	63	3F	0111111	7Eh
FLT	FLT	PU	64	40	1000000	80h
FLT	FLT	V_{DD}	65	41	1000001	82h
FLT	PU	GND	66	42	1000010	84h
FLT	PU	PD	67	43	1000011	86h
FLT	PU	FLT	68	44	1000100	88h
FLT	PU	PU	69	45	1000101	8Ah
FLT	PU	V_{DD}	70	46	1000110	8Ch
FLT	V_{DD}	GND	71	47	1000111	8Eh
FLT	V_{DD}	PD	72	48	1001000	90h
FLT	V_{DD}	FLT	73	49	1001001	92h
FLT	V_{DD}	PU	74	4A	1001010	94h
FLT	V_{DD}	V_{DD}	75	4B	1001011	96h
PU	GND	GND	76	4C	1001100	98h
PU	GND	PD	77	4D	1001101	9Ah
PU	GND	FLT	78	4E	1001110	9Ch
PU	GND	PU	79	4F	1001111	9Eh
PU	GND	V_{DD}	80	50	1010000	A0h
PU	PD	GND	81	51	1010001	A2h
PU	PD	PD	82	52	1010010	A4h
PU	PD	FLT	83	53	1010011	A6h
PU	PD	PU	84	54	1010100	A8h
PU	PD	V_{DD}	85	55	1010101	AAh
PU	FLT	GND	86	56	1010110	ACh
PU	FLT	PD	87	57	1010111	AEh

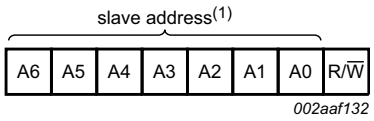
Table 5. I²C-bus slave address *…continued*

Hardware selectable input pins			I²C-bus slave address for PCA9955B			
AD2	**AD1**	**AD0**	**Decimal**	**Hexadecimal**	**Binary (A[6:0])**	**Address (R/$\overline{W}$ = 0)**
PU	FLT	FLT	88	58	1011000	B0h
PU	FLT	PU	89	59	1011001	B2h
PU	FLT	V_{DD}	90	5A	1011010	B4h
PU	PU	GND	91	5B	1011011	B6h
PU	PU	PD	92	5C	1011100	B8h
PU	PU	FLT	93	5D	1011101	BAh
PU	PU	PU	94	5E	1011110	BCh
PU	PU	V_{DD}	95	5F	1011111	BEh
PU	V_{DD}	GND	96	60	1100000	C0h
PU	V_{DD}	PD	97	61	1100001	C2h
PU	V_{DD}	FLT	98	62	1100010	C4h
PU	V_{DD}	PU	99	63	1100011	C6h
PU	V_{DD}	V_{DD}	100	64	1100100	C8h
V_{DD}	GND	GND	101	65	1100101	CAh
V_{DD}	GND	PD	102	66	1100110	CCh
V_{DD}	GND	FLT	103	67	1100111	CEh
V_{DD}	GND	PU	104	68	1101000	D0h
V_{DD}	GND	V_{DD}	105	69	1101001	D2h
V_{DD}	PD	GND	106	6A	1101010	D4h
V_{DD}	PD	PD	107	6B	1101011	D6h
V_{DD}	PD	FLT	108	6C	1101100	D8h
V_{DD}	PD	PU	109	6D	1101101	DAh
V_{DD}	PD	V_{DD}	110	6E	1101110	DCh
V_{DD}	FLT	GND	111	6F	1101111	DEh
V_{DD}	FLT	PD	112	70	1110000	E0h
V_{DD}	FLT	FLT	113	71	1110001	E2h
V_{DD}	FLT	PU	114	72	1110010	E4h
V_{DD}	FLT	V_{DD}	115	73	1110011	E6h
V_{DD}	PU	GND	116	74	1110100	E8h
V_{DD}	PU	PD	117	75	1110101	EAh
V_{DD}	PU	FLT	118	76	1110110	ECh
V_{DD}	PU	PU	119	77	1110111	EEh
V_{DD}	PU	V_{DD}	120	78	1111000[1]	F0h
V_{DD}	V_{DD}	GND	121	79	1111001[1]	F2h
V_{DD}	V_{DD}	PD	122	7A	1111010[1]	F4h
V_{DD}	V_{DD}	FLT	123	7B	1111011[1]	F6h
V_{DD}	V_{DD}	PU	124	7C	1111100[1]	F8h
V_{DD}	V_{DD}	V_{DD}	125	7D	1111101[1]	FAh

[1] See ‘Remark’ below.

Remark: Reserved I²C-bus addresses must be used with caution since they can interfere with:

- 'reserved for future use' I²C-bus addresses (0000 011, 1111 1XX)
- slave devices that use the 10-bit addressing scheme (1111 0XX)
- slave devices that are designed to respond to the General Call address (0000 000)
- High-speed mode (Hs-mode) master code (0000 1XX)



(1) This slave address must match one of the 125 internal addresses as shown in Table 5

Fig 3. PCA9955B slave address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

7.1.2 LED All Call I²C-bus address

- Default power-up value (ALLCALLADR register): E0h or 1110 000X
- Programmable through I²C-bus (volatile programming)
- At power-up, LED All Call I²C-bus address is enabled. PCA9955B sends an ACK when E0h (R/$\overline{W}$ = 0) or E1h (R/$\overline{W}$ = 1) is sent by the master.

See Section 7.3.11 "ALLCALLADR, LED All Call I²C-bus address" for more detail.

Remark: The default LED All Call I²C-bus address (E0h or 1110 000X) must not be used as a regular I²C-bus slave address since this address is enabled at power-up. All of the PCA9955Bs on the I²C-bus acknowledge the address if sent by the I²C-bus master.

7.1.3 LED Sub Call I²C-bus addresses

- 3 different I²C-bus addresses can be used
- Default power-up values:
  - SUBADR1 register: ECh or 1110 110X
  - SUBADR2 register: ECh or 1110 110X
  - SUBADR3 register: ECh or 1110 110X
- Programmable through I²C-bus (volatile programming)
- At power-up, SUBADR1 is enabled while SUBADR2 and SUBADR3 I²C-bus addresses are disabled.

Remark: At power-up SUBADR1 identifies this device as a 16-channel driver.

See Section 7.3.10 "LED Sub Call I²C-bus addresses for PCA9955B" for more detail.

Remark: The default LED Sub Call I²C-bus addresses may be used as regular I²C-bus slave addresses as long as they are disabled.

7.2 Control register

Following the successful acknowledgement of the slave address, LED All Call address or LED Sub Call address, the bus master sends a byte to the PCA9955B, which is stored in the Control register.

The lowest 7 bits are used as a pointer to determine which register is accessed (D[6:0]). The highest bit is used as Auto-Increment Flag (AIF).

This bit along with the MODE1 register bit 5 and bit 6 provide the Auto-Increment feature.

reset state = 80h

Remark: The Control register does not apply to the Software Reset I²C-bus address

Fig 4. Control register

When the Auto-Increment Flag is set (AIF = logic 1), the seven low-order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values of MODE1 register.

Table 6. Auto-Increment options

AIF	AI1[1]	AI0[1]	Function
0	0	0	no Auto-Increment
1	0	0	Auto-Increment for registers (00h to 43h). D[6:0] roll over to 00h after the last register 43h is accessed.
1	0	1	Auto-Increment for individual brightness registers only (08h to 17h). D[6:0] roll over to 08h after the last register (17h) is accessed.
1	1	0	Auto-Increment for MODE1 to IREF15 control registers (00h to 27h). D[6:0] roll over to 00h after the last register (27h) is accessed.
1	1	1	Auto-Increment for global control registers and individual brightness registers (06h to 17h). D[6:0] roll over to 06h after the last register (17h) is accessed.

[1] AI1 and AI0 come from MODE1 register.

Remark: Other combinations not shown in Table 6 (AIF + AI[1:0] = 001b, 010b and 011b) are reserved and must not be used for proper device operation.

AIF + AI[1:0] = 000b is used when the same register must be accessed several times during a single I²C-bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AIF + AI[1:0] = 100b is used when all the registers must be sequentially accessed, for example, power-up programming.

AIF + AI[1:0] = 101b is used when the 16 LED drivers must be individually programmed with different values during the same I²C-bus communication, for example, changing color setting to another color setting.

AIF + AI[1:0] = 110b is used when MODE1 to IREF15 registers must be programmed with different settings during the same I²C-bus communication.

AIF + AI[1:0] = 111b is used when the 16 LED drivers must be individually programmed with different values in addition to global programming.

Only the 7 least significant bits D[6:0] are affected by the AIF, AI1 and AI0 bits.

When the Control register is written, the register entry point determined by D[6:0] is the first register that will be addressed (read or write operation), and can be anywhere between 00h and 49h (as defined in Table 7). When AIF = 1, the Auto-Increment Flag is set and the rollover value at which the register increment stops and goes to the next one is determined by AIF, AI1 and AI0. See Table 6 for rollover values. For example, if MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1001 0000, then the register addressing sequence is (in hexadecimal):
10 → 11 → … → 17 → 08 → 09 → … → 17 → 08 → 09 → … as long as the master keeps sending or reading data.

If MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1010 0010, then the register addressing sequence is (in hexadecimal):
22 → 23 → … → 43 → 00 → 01 → … → 17 → 08 → 09 → … as long as the master keeps sending or reading data.

If MODE1 register bit AI1 = 0 and AI0 = 1 and if the Control register = 1000 0101, then the register addressing sequence is (in hexadecimal):
05 → 06 → … → 17 → 08 → 09 → … → 17 → 08 → 09 → … as long as the master keeps sending or reading data.

Remark: Writing to registers marked ‘not used’ returns NACK.

7.3 Register definitions

Table 7. Register summary

Register number (hex)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
00h	0	0	0	0	0	0	0	MODE1	read/write	Mode register 1
01h	0	0	0	0	0	0	1	MODE2	read/write	Mode register 2
02h	0	0	0	0	0	1	0	LEDOUT0	read/write	LED output state 0
03h	0	0	0	0	0	1	1	LEDOUT1	read/write	LED output state 1
04h	0	0	0	0	1	0	0	LEDOUT2	read/write	LED output state 2
05h	0	0	0	0	1	0	1	LEDOUT3	read/write	LED output state 3
06h	0	0	0	0	1	1	0	GRPPWM	read/write	group duty cycle control
07h	0	0	0	0	1	1	1	GRPFREQ	read/write	group frequency
08h	0	0	0	1	0	0	0	PWM0	read/write	brightness control LED0
09h	0	0	0	1	0	0	1	PWM1	read/write	brightness control LED1
0Ah	0	0	0	1	0	1	0	PWM2	read/write	brightness control LED2
0Bh	0	0	0	1	0	1	1	PWM3	read/write	brightness control LED3
0Ch	0	0	0	1	1	0	0	PWM4	read/write	brightness control LED4
0Dh	0	0	0	1	1	0	1	PWM5	read/write	brightness control LED5
0Eh	0	0	0	1	1	1	0	PWM6	read/write	brightness control LED6

Table 7. Register summary *…continued*

Register number (hex)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
0Fh	0	0	0	1	1	1	1	PWM7	read/write	brightness control LED7
10h	0	0	1	0	0	0	0	PWM8	read/write	brightness control LED8
11h	0	0	1	0	0	0	1	PWM9	read/write	brightness control LED9
12h	0	0	1	0	0	1	0	PWM10	read/write	brightness control LED10
13h	0	0	1	0	0	1	1	PWM11	read/write	brightness control LED11
14h	0	0	1	0	1	0	0	PWM12	read/write	brightness control LED12
15h	0	0	1	0	1	0	1	PWM13	read/write	brightness control LED13
16h	0	0	1	0	1	1	0	PWM14	read/write	brightness control LED14
17h	0	0	1	0	1	1	1	PWM15	read/write	brightness control LED15
18h	0	0	1	1	0	0	0	IREF0	read/write	output gain control register 0
19h	0	0	1	1	0	0	1	IREF1	read/write	output gain control register 1
1Ah	0	0	1	1	0	1	0	IREF2	read/write	output gain control register 2
1Bh	0	0	1	1	0	1	1	IREF3	read/write	output gain control register 3
1Ch	0	0	1	1	1	0	0	IREF4	read/write	output gain control register 4
1Dh	0	0	1	1	1	0	1	IREF5	read/write	output gain control register 5
1Eh	0	0	1	1	1	1	0	IREF6	read/write	output gain control register 6
1Fh	0	0	1	1	1	1	1	IREF7	read/write	output gain control register 7
20h	0	1	0	0	0	0	0	IREF8	read/write	output gain control register 8
21h	0	1	0	0	0	0	1	IREF9	read/write	output gain control register 9
22h	0	1	0	0	0	1	0	IREF10	read/write	output gain control register 10
23h	0	1	0	0	0	1	1	IREF11	read/write	output gain control register 11
24h	0	1	0	0	1	0	0	IREF12	read/write	output gain control register 12
25h	0	1	0	0	1	0	1	IREF13	read/write	output gain control register 13
26h	0	1	0	0	1	1	0	IREF14	read/write	output gain control register 14
27h	0	1	0	0	1	1	1	IREF15	read/write	output gain control register 15
28h	0	1	0	1	0	0	0	RAMP_RATE_GRP0	read/write	ramp enable and rate control for group 0
29h	0	1	0	1	0	0	1	STEP_TIME_GRP0	read/write	step time control for group 0
2Ah	0	1	0	1	0	1	0	HOLD_CNTL_GRP0	read/write	hold ON/OFF time control for group 0
2Bh	0	1	0	1	0	1	1	IREF_GRP0	read/write	output gain control for group 0
2Ch	0	1	0	1	1	0	0	RAMP_RATE_GRP1	read/write	ramp enable and rate control for group 1
2Dh	0	1	0	1	1	0	1	STEP_TIME_GRP1	read/write	step time control for group 1
2Eh	0	1	0	1	1	1	0	HOLD_CNTL_GRP1	read/write	hold ON/OFF time control for group 1
2Fh	0	1	0	1	1	1	1	IREF_GRP1	read/write	output gain control for group 1
30h	0	1	1	0	0	0	0	RAMP_RATE_GRP2	read/write	ramp enable and rate control for group 2
31h	0	1	1	0	0	0	1	STEP_TIME_GRP2	read/write	step time control for group 2
32h	0	1	1	0	0	1	0	HOLD_CNTL_GRP2	read/write	hold ON/OFF time control for group 2

Table 7. Register summary *…continued*

Register number (hex)	D6	D5	D4	D3	D2	D1	D0	Name	Type	Function
33h	0	1	1	0	0	1	1	IREF_GRP2	read/write	output gain control for group 2
34h	0	1	1	0	1	0	0	RAMP_RATE_GRP3	read/write	ramp enable and rate control for group 3
35h	0	1	1	0	1	0	1	STEP_TIME_GRP3	read/write	step time control for group 3
36h	0	1	1	0	1	1	0	HOLD_CNTL_GRP3	read/write	hold ON/OFF time control for group 3
37h	0	1	1	0	1	1	1	IREF_GRP3	read/write	output gain control for group 3
38h	0	1	1	1	0	0	0	GRAD_MODE_SEL0	read/write	gradation mode select register for channel 7 to channel 0
39h	0	1	1	1	0	0	1	GRAD_MODE_SEL1	read/write	gradation mode select register for channel 15 to channel 8
3Ah	0	1	1	1	0	1	0	GRAD_GRP_SEL0	read/write	gradation group select for channel 3 to channel 0
3Bh	0	1	1	1	0	1	1	GRAD_GRP_SEL1	read/write	gradation group select for channel 7 to channel 4
3Ch	0	1	1	1	1	0	0	GRAD_GRP_SEL2	read/write	gradation group select for channel 11 to channel 8
3Dh	0	1	1	1	1	0	1	GRAD_GRP_SEL3	read/write	gradation group select for channel 15 to channel 12
3Eh	0	1	1	1	1	1	0	GRAD_CNTL	read/write	gradation control register for all four groups
3Fh	0	1	1	1	1	1	1	OFFSET	read/write	Offset/delay on LEDn outputs
40h	1	0	0	0	0	0	0	SUBADR1	read/write	I²C-bus subaddress 1
41h	1	0	0	0	0	0	1	SUBADR2	read/write	I²C-bus subaddress 2
42h	1	0	0	0	0	1	0	SUBADR3	read/write	I²C-bus subaddress 3
43h	1	0	0	0	0	1	1	ALLCALLADR	read/write	All Call I²C-bus address
44h	1	0	0	0	1	0	0	PWMALL	write only	brightness control for all LEDn
45h	1	0	0	0	1	0	1	IREFALL	write only	output gain control for all registers IREF0 to IREF15
46h	1	0	0	0	1	1	0	EFLAG0	read only	output error flag 0
47h	1	0	0	0	1	1	1	EFLAG1	read only	output error flag 1
48h	1	0	0	1	0	0	0	EFLAG2	read only	output error flag 2
49h	1	0	0	1	0	0	1	EFLAG3	read only	output error flag 3
4Ah to 7Fh	-	-	-	-	-	-	-	reserved	read only	not used[1]

[1] Reserved registers should not be written to and will always read back as zeros.

7.3.1 MODE1 — Mode register 1

Table 8. MODE1 - Mode register 1 (address 00h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	AIF	read only	0	Register Auto-Increment disabled.
			1*	Register Auto-Increment enabled.
6	AI1	R/W	0*	Auto-Increment bit 1 = 0. Auto-increment range as defined in Table 6.
			1	Auto-Increment bit 1 = 1. Auto-increment range as defined in Table 6.
5	AI0	R/W	0*	Auto-Increment bit 0 = 0. Auto-increment range as defined in Table 6.
			1	Auto-Increment bit 0 = 1. Auto-increment range as defined in Table 6.
4	SLEEP	R/W	0*	Normal mode[1].
			1	Low power mode. Oscillator off[2][3].
3	SUB1	R/W	0	PCA9955B does not respond to I²C-bus subaddress 1.
			1*	PCA9955B responds to I²C-bus subaddress 1.
2	SUB2	R/W	0*	PCA9955B does not respond to I²C-bus subaddress 2.
			1	PCA9955B responds to I²C-bus subaddress 2.
1	SUB3	R/W	0*	PCA9955B does not respond to I²C-bus subaddress 3.
			1	PCA9955B responds to I²C-bus subaddress 3.
0	ALLCALL	R/W	0	PCA9955B does not respond to LED All Call I²C-bus address.
			1*	PCA9955B responds to LED All Call I²C-bus address.

[1] It takes 500 μs max. for the oscillator to be up and running once SLEEP bit has been set to logic 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM or GRPFREQ registers are accessed within the 500 μs window.

[2] No blinking, dimming or gradation control is possible when the oscillator is off.

[3] The device must be reset if the LED driver output state is set to LDRx=11 after the device is set back to Normal mode.

7.3.2 MODE2 — Mode register 2

Table 9. MODE2 - Mode register 2 (address 01h) bit description

*Legend: * default value.*

Bit	Symbol	Access	Value	Description
7	OVERTEMP	read only	0*	O.K.
			1	overtemperature condition
6	ERROR	read only	0*	no error at LED outputs
			1	any open or short-circuit detected in error flag registers (EFLAGn)
5	DMBLNK	R/W	0*	group control = dimming
			1	group control = blinking
4	CLRERR	write only	0*	self clear after write '1'
			1	Write '1' to clear all error status bits in EFLAGn register and ERROR (bit 6). The EFLAGn and ERROR bit sets to '1' if open or short-circuit is detected again.
3	OCH	R/W	0*	outputs change on STOP condition
			1	outputs change on ACK
2	EXP_EN	R/W	0*	linear adjustment for gradation control
			1	exponential adjustment for gradation control
1	-	read only	0*	reserved
0	-	read only	1*	reserved

Brightness adjustment for gradation control is either linear or exponential by setting the EXP_EN bit as shown in Figure 5. When EXP_EN = 0, linear adjustment scale is used. When EXP_EN = 1, exponential scale is used.

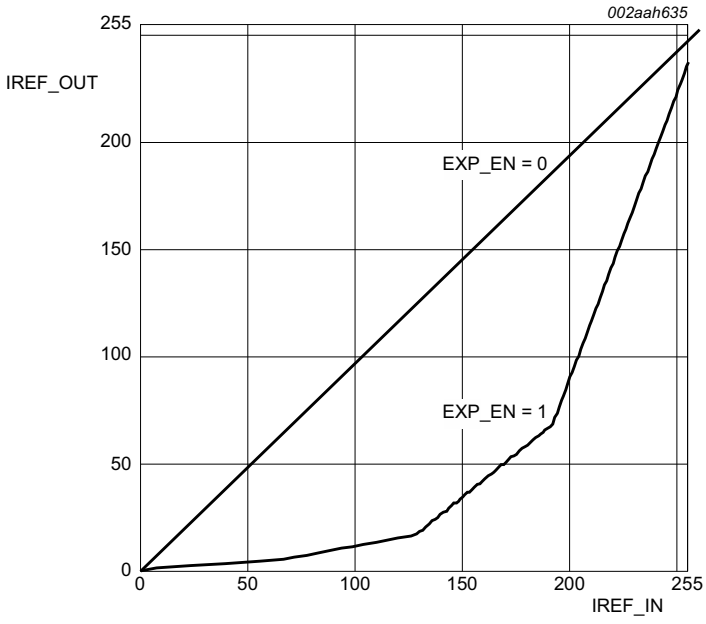


Fig 5. Linear and exponential adjustment curves

7.3.3 LEDOUT0 to LEDOUT3, LED driver output state

Table 10. LEDOUT0 to LEDOUT3 - LED driver output state registers (address 02h to 05h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
02h	LEDOUT0	7:6	LDR3	R/W	10*	LED3 output state control
		5:4	LDR2	R/W	10*	LED2 output state control
		3:2	LDR1	R/W	10*	LED1 output state control
		1:0	LDR0	R/W	10*	LED0 output state control
03h	LEDOUT1	7:6	LDR7	R/W	10*	LED7 output state control
		5:4	LDR6	R/W	10*	LED6 output state control
		3:2	LDR5	R/W	10*	LED5 output state control
		1:0	LDR4	R/W	10*	LED4 output state control
04h	LEDOUT2	7:6	LDR11	R/W	10*	LED11 output state control
		5:4	LDR10	R/W	10*	LED10 output state control
		3:2	LDR9	R/W	10*	LED9 output state control
		1:0	LDR8	R/W	10*	LED8 output state control
05h	LEDOUT3	7:6	LDR15	R/W	10*	LED15 output state control
		5:4	LDR14	R/W	10*	LED14 output state control
		3:2	LDR13	R/W	10*	LED13 output state control
		1:0	LDR12	R/W	10*	LED12 output state control

LDRx = 00 — LED driver x is off (x = 0 to 15).

LDRx = 01 — LED driver x is fully on (individual brightness and group dimming/blinking not controlled). The $\overline{OE}$ pin can be used as external dimming/blinking control in this state.

LDRx = 10 — LED driver x individual brightness can be controlled through its PWMx register (default power-up state) or PWMALL register for all LEDn outputs.

LDRx = 11 — LED driver x individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

Remark: Setting the device in low power mode while being on group dimming/blinking mode may cause the LED output state to be in an unknown state after the device is set back to normal mode. The device must be reset and all register values reprogrammed.

7.3.4 GRPPWM, group duty cycle control

Table 11. GRPPWM - Group brightness control register (address 06h) bit description

*Legend: * default value*

Address	Register	Bit	Symbol	Access	Value	Description
06h	GRPPWM	7:0	GDC[7:0]	R/W	1111 1111*	GRPPWM register

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 122 Hz fixed frequency signal is superimposed with the 31.25 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a ‘Don’t care’.

General brightness for the 16 outputs is controlled through 255 linear steps from 00h (0 % duty cycle = LED output off) to FFh (99.6 % duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 67 ms to 16.8 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$duty\ cycle = \frac{GDC[7:0]}{256} \quad (1)$$

7.3.5 GRPFREQ, group frequency

Table 12. GRPFREQ - Group frequency register (address 07h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
07h	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000*	GRPFREQ register

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a ‘Don’t care’ when DMBLNK = 0. Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

Blinking period is controlled through 256 linear steps from 00h (67 ms, frequency 15 Hz) to FFh (16.8 s).

$$global\ blinking\ period = \frac{GFRQ[7:0] + 1}{15.26}(s) \quad (2)$$

7.3.6 PWM0 to PWM15, individual brightness control

Table 13. PWM0 to PWM15 - PWM registers 0 to 15 (address 08h to 17h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
08h	PWM0	7:0	IDC0[7:0]	R/W	0000 0000*	PWM0 Individual Duty Cycle
09h	PWM1	7:0	IDC1[7:0]	R/W	0000 0000*	PWM1 Individual Duty Cycle
0Ah	PWM2	7:0	IDC2[7:0]	R/W	0000 0000*	PWM2 Individual Duty Cycle
0Bh	PWM3	7:0	IDC3[7:0]	R/W	0000 0000*	PWM3 Individual Duty Cycle
0Ch	PWM4	7:0	IDC4[7:0]	R/W	0000 0000*	PWM4 Individual Duty Cycle
0Dh	PWM5	7:0	IDC5[7:0]	R/W	0000 0000*	PWM5 Individual Duty Cycle
0Eh	PWM6	7:0	IDC6[7:0]	R/W	0000 0000*	PWM6 Individual Duty Cycle
0Fh	PWM7	7:0	IDC7[7:0]	R/W	0000 0000*	PWM7 Individual Duty Cycle
10h	PWM8	7:0	IDC8[7:0]	R/W	0000 0000*	PWM8 Individual Duty Cycle
11h	PWM9	7:0	IDC9[7:0]	R/W	0000 0000*	PWM9 Individual Duty Cycle
12h	PWM10	7:0	IDC10[7:0]	R/W	0000 0000*	PWM10 Individual Duty Cycle
13h	PWM11	7:0	IDC11[7:0]	R/W	0000 0000*	PWM11 Individual Duty Cycle
14h	PWM12	7:0	IDC12[7:0]	R/W	0000 0000*	PWM12 Individual Duty Cycle

Table 13. PWM0 to PWM15 - PWM registers 0 to 15 (address 08h to 17h) bit description
…continued

Address	Register	Bit	Symbol	Access	Value	Description
15h	PWM13	7:0	IDC13[7:0]	R/W	0000 0000*	PWM13 Individual Duty Cycle
16h	PWM14	7:0	IDC14[7:0]	R/W	0000 0000*	PWM14 Individual Duty Cycle
17h	PWM15	7:0	IDC15[7:0]	R/W	0000 0000*	PWM15 Individual Duty Cycle

A 31.25 kHz fixed frequency signal is used for each output. Duty cycle is controlled through 255 linear steps from 00h (0 % duty cycle = LED output off) to FEh (99.2 % duty cycle = LED output at maximum brightness) and FFh (100 % duty cycle = LED output completed ON). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 to LEDOUT3 registers).

$$duty\ cycle = \frac{IDCx[7:0]}{256} \quad (3)$$

Remark: The first lower end 8 steps of PWM and the last (higher end) steps of PWM will not have effective brightness control of LEDs due to edge rate control of LED output pins.

7.3.7 IREF0 to IREF15, LED output current value registers

These registers reflect the gain settings for output current for LED0 to LED15.

Table 14. IREF0 to IREF15 - LED output gain control registers (address 18h to 27h) bit description
*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
18h	IREF0	7:0	R/W	00h*	LED0 output current setting
19h	IREF1	7:0	R/W	00h*	LED1 output current setting
1Ah	IREF2	7:0	R/W	00h*	LED2 output current setting
1Bh	IREF3	7:0	R/W	00h*	LED3 output current setting
1Ch	IREF4	7:0	R/W	00h*	LED4 output current setting
1Dh	IREF5	7:0	R/W	00h*	LED5 output current setting
1Eh	IREF6	7:0	R/W	00h*	LED6 output current setting
1Fh	IREF7	7:0	R/W	00h*	LED7 output current setting
20h	IREF8	7:0	R/W	00h*	LED8 output current setting
21h	IREF9	7:0	R/W	00h*	LED9 output current setting
22h	IREF10	7:0	R/W	00h*	LED10 output current setting
23h	IREF11	7:0	R/W	00h*	LED11 output current setting
24h	IREF12	7:0	R/W	00h*	LED12 output current setting
25h	IREF13	7:0	R/W	00h*	LED13 output current setting
26h	IREF14	7:0	R/W	00h*	LED14 output current setting
27h	IREF15	7:0	R/W	00h*	LED15 output current setting

7.3.8 Gradation control

Gradation control is designed to use four independent groups of registers to program the full cycle of the gradation timing to implement on each selected channel. Each group has four registers to define the ramp rate, step time, hold ON/OFF time, and final hold ON current, as shown in Figure 6.

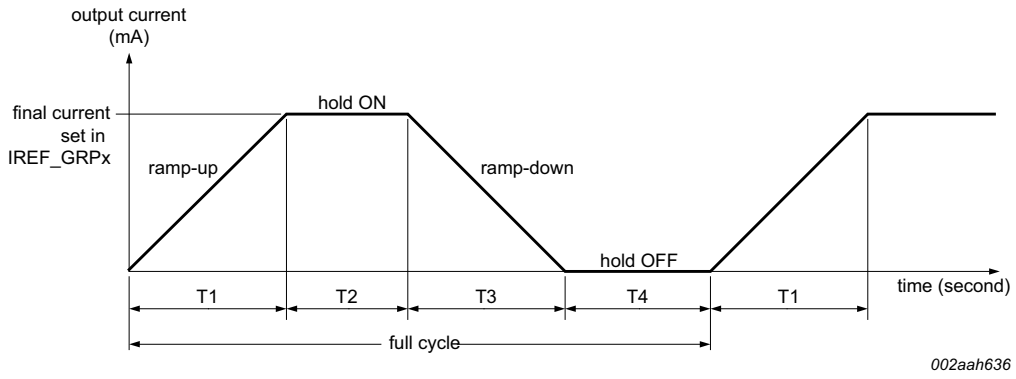


Fig 6. Gradation timing

- The 'final' and 'hold ON' current is defined in IREF_GRPx register value × (225 μA if REXT = 1 kΩ, or 112.5 μA if REXT = 2 kΩ).
- Ramp rate value and enable/disable ramp operation is defined in RAMP_RATE_GRPx register.
- Total number of ramp steps (or level changes) is calculated as 'IREF_GRPx value' ÷ 'ramp rate value in RAMP_RATE_GRPx'. Rounds a number up to the next integer if the total number is not an integer.
- Time for each step is calculated as 'cycle time' × 'multiple factor' bits in STEP_TIME_GRPx register. Minimum time for one step is 0.5 ms (0.5 ms × 1) and maximum time is 512 ms (8 ms × 64).
- The ramp-up or ramp-down time (T1 or T3) is calculated as '(total steps + 1)' × 'step time'.
- Hold ON or OFF time (T2 or T4) is defined in HOLD_CNTL_GRPx register in the range of 0/0.25/0.5/0.75/1/2/4/6 seconds.
- Gradation start or stop with single shot mode (one full cycle only) or continuous mode (repeat full cycle) is defined in the GRAD_CNTL register for all groups.
- Each channel can be assigned to one of these four groups in the GRAD_GRP_SELx register.
- Each channel can set either normal mode or gradation mode operation in the GRAD_MODE_SELx register.

To enable the gradation operation, the following steps are required:

1. Program all gradation control registers except the gradation start bit in GRAD_CNTL register.
2. Program either LDRx = 01 (LED fully ON mode) only, or LDRx = 10 or 11 (PWM control mode) with individual brightness control PWMx register for duty cycle.

3. Program output current value IREFx register to non-zero, which will enable LED output.
4. Set the gradation start bit in GRAD_CNTL register for enabling gradation operation.

7.3.8.1 RAMP_RATE_GRP0 to RAMP_RATE_GRP3, ramp rate control registers

Table 15. RAMP_RATE_GRP[0:3] - Ramp enable and rate control registers (address 28h, 2Ch, 30h, 34h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
28h	RAMP_RATE_GRP0	7	R/W	0*	Ramp-up disable
2Ch	RAMP_RATE_GRP1			1	Ramp-up enable
30h	RAMP_RATE_GRP2	6	R/W	0*	Ramp-down disable
34h	RAMP_RATE_GRP3			1	Ramp-down enable
		5:0	R/W	0x00*	Ramp rate value per step is defined from 1 (00h) to 64 (3Fh)[1][2]

[1] Total number of ramp steps is defined as 'IREF_GRP[7:0]' ÷ 'ramp_rate[5:0]'. (Round up to next integer if it is not an integer number.)

[2] Per step current increment or decrement is calculated by the (ramp_rate × I_{ref}), where the I_{ref} reference current is 112.5 μA (REXT = 2 kΩ) or 225 μA (REXT = 1 kΩ).

7.3.8.2 STEP_TIME_GRP0 to STEP_TIME_GRP3, step time control registers

Table 16. STEP_TIME_GRP[0:3] - Step time control registers (address 29h, 2Dh, 31h, 35h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
29h	STEP_TIME_GRP0	7	read only	0*	reserved
2Dh	STEP_TIME_GRP1	6	R/W	0*	Cycle time is set to 0.5 ms
31h	STEP_TIME_GRP2			1	Cycle time is set to 8 ms
35h	STEP_TIME_GRP3	5:0	R/W	0x00*	Multiple factor per step, the multiple factor is defined from 1 (00h) to 64 (3Fh)[1]

[1] Step time = cycle time (0.5 ms or 8 ms) × multiple factor (1 ~ 64); minimum step time is 0.5 ms and maximum step time is 512 ms.

7.3.8.3 HOLD_CNTL_GRP0 to HOLD_CNTL_GRP3, hold ON and OFF control registers

Table 17. HOLD_CNTL_GRP[0:3] - Hold ON and OFF enable and time control registers (address 2Ah, 2Eh, 32h, 36h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
2Ah 2Eh 32h 36h	HOLD_CNTL_GRP0 HOLD_CNTL_GRP1 HOLD_CNTL_GRP2 HOLD_CNTL_GRP3	7	R/W	0*	Hold ON disable
				1	Hold ON enable
		6	R/W	0*	Hold OFF disable
				1	Hold OFF enable
		5:3	R/W	000*	Hold ON time select:[1] 000: 0 s 001: 0.25 s 010: 0.5 s 011: 0.75 s 100: 1 s 101: 2 s 110: 4 s 111: 6 s
		2:0	R/W	000*	Hold OFF time select:[1] 000: 0 s 001: 0.25 s 010: 0.5 s 011: 0.75 s 100: 1 s 101: 2 s 110: 4 s 111: 6 s

[1] Hold ON or OFF minimum time is 0 s and maximum time is 6 s

7.3.8.4 IREF_GRP0 to IREF_GRP3, output gain control

Table 18. IREF_GRP[0:3] - Final and hold ON output gain setting registers (address 2Bh, 2Fh, 33h, 37h) for each group bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
2Bh 2Fh 33h 37h	IREF_GRP0 IREF_GRP1 IREF_GRP2 IREF_GRP3	7:0	R/W	00h*	Final ramp-up and hold ON output current gain setting[1]

[1] Output current = I_{ref} × IREF_GRPx[7:0], where I_{ref} is reference current. I_{ref} = 112.5 μA if REXT = 2 kΩ, or I_{ref} = 225 μA if REXT = 1 kΩ

7.3.8.5 GRAD_MODE_SEL0 to GRAD_MODE_SEL1, Gradation mode select registers

Table 19. GRAD_MODE_SEL[0:1] - Gradation mode select register for channel 15 to channel 0 (address 38h, 39h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description[1][2]
38h	GRAD_MODE_SEL0	7:0	R/W	00*	Normal operation mode for channel 7 to channel 0
				FFh	Gradation operation mode for channel 7 to channel 0
39h	GRAD_MODE_SEL1	7:0	R/W	00*	Normal operation mode for channel 15 to channel 8
				FFh	Gradation operation mode for channel 15 to channel 8

[1] Each bit represents one channel that can set either 0 for normal mode (use IREFx to set individual LED output current), or 1 for gradation mode (use IREF_GRPx to set group LEDs output current.).

[2] In gradation mode, it only affects the source of the IREF current level and does not affect the PWMx operation or LEDOUTx registers' function. It is possible to use the gradation feature, individual PWMx and group PWM simultaneously.

7.3.8.6 GRAD_GRP_SEL0 to GRAD_GRP_SEL3, Gradation group select registers

Table 20. GRAD_GRP_SEL[0:3] - Gradation group select register for channel 15 to channel 0 (address 3Ah, 3Bh, 3Ch, 3Dh) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description[1]
3Ah	GRAD_GRP_SEL0	7:6	R/W	00*	Gradation group select for LED3 output
		5:4	R/W	00*	Gradation group select for LED2 output
		3:2	R/W	00*	Gradation group select for LED1 output
		1:0	R/W	00*	Gradation group select for LED0 output
3Bh	GRAD_GRP_SEL1	7:6	R/W	01*	Gradation group select for LED7 output
		5:4	R/W	01*	Gradation group select for LED6 output
		3:2	R/W	01*	Gradation group select for LED5 output
		1:0	R/W	01*	Gradation group select for LED4 output
3Ch	GRAD_GRP_SEL2	7:6	R/W	10*	Gradation group select for LED11 output
		5:4	R/W	10*	Gradation group select for LED10 output
		3:2	R/W	10*	Gradation group select for LED9 output
		1:0	R/W	10*	Gradation group select for LED8 output
3Dh	GRAD_GRP_SEL3	7:6	R/W	11*	Gradation group select for LED15 output
		5:4	R/W	11*	Gradation group select for LED14 output
		3:2	R/W	11*	Gradation group select for LED13 output
		1:0	R/W	11*	Gradation group select for LED12 output

[1] LED[3:0] outputs default assigned to group 0; LED[7:4] outputs default assigned to group 1; LED[11:8] outputs default assigned to group 2; LED[15:12] outputs default assigned to group 3.

7.3.8.7 GRAD_CNTL, Gradation control register

Table 21. GRAD_CNTL - Gradation control register for group 3 to group 0 (address 3Eh) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
3Eh	GRAD_CNTL	7	R/W	0*	Gradation stop or done for group 3[1]
				1	Gradation start for group 3[2]
		6	R/W	0*	Single shot operation for group 3
				1	Continuous operation for group 3
		5	R/W	0*	Gradation stop or done for group 2[1]
				1	Gradation start for group 2[2]
		4	R/W	0*	Single shot operation for group 2
				1	Continuous operation for group 2
		3	R/W	0*	Gradation stop or done for group 1[1]
				1	Gradation start for group 1[2]
		2	R/W	0*	Single shot operation for group 1
				1	Continuous operation for group 1
		1	R/W	0*	Gradation stop or done for group 0[1]
				1	Gradation start for group 0[2]
		0	R/W	0*	Single shot operation for group 0
				1	Continuous operation for group 0

[1] When the gradation operation is forced to stop, the output current stops immediately and is frozen at the last output level.

[2] This bit will be self-cleared when single mode is completed, and writing 0 to this bit will force to stop the gradation operation when single mode is not completed or continuous mode is running.

7.3.8.8 Ramp control — equation and calculation example

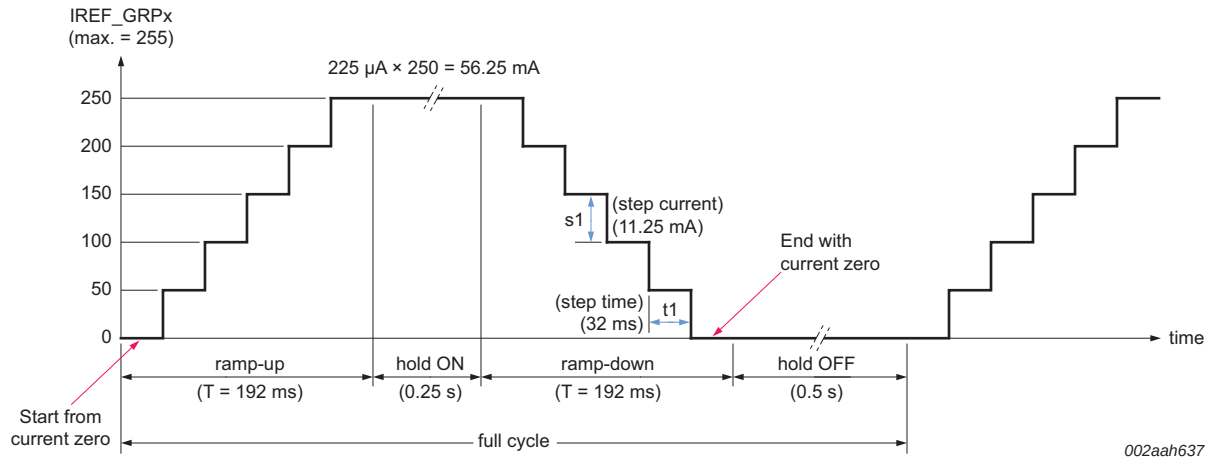


Fig 7. Ramp calculation example 1

- t1 (step time) = cycle time × multiple factor, where:
  - Cycle time = 0.5 ms (fast ramp) or 8 ms (slow ramp) in STEP_TIME_GRPx[6]
  - Multiple factor = 6-bit, from 1 (00h) to 64 (3Fh) counts in STEP_TIME_GRPx[5:0]
- s1 (step current) = ramp_rate × I_{ref}, where:
  - ramp_rate = 6-bit, from 1 (00h) to 64 (3Fh) counts in RAMP_RATE_GRPx[5:0]
  - I_{ref} = reference current either 112.5 µA if REXT = 2 kΩ, or 225 µA if REXT = 1 kΩ
- S (total steps) = (IREF_GRPx / ramp_rate), where:
  - IREF_GRPx = output current gain setting, 8-bit, up to 255 counts
  - ramp_rate = 6-bit, up to 64 counts in RAMP_RATE_GRPx[5:0]
  - If it is not an integer, then round up to next integer number.
- T (ramp time) = (S (total steps) + 1) × t1 (step time)
  - Ramp-up time starts from zero current and ends at the maximum current
  - Ramp-down time starts from the maximum current and ends at the zero current

Calculation example 1 (Figure 7):

- Assumption:
  - I_{ref} = 225 µA if REXT = 1 kΩ
  - Output hold ON current = 225 µA × 250 = 56.25 mA (IREF_GRPx[7:0] = FAh)
  - Cycle time = 0.5 ms (STEP_TIME_GRPx[6] = 0)
  - Multiple factor = 64 (STEP_TIME_GRPx[5:0] = 3Fh)
  - Ramp rate = 50 (RAMP_RATE_GRPx[5:0] = 31h)
  - Hold ON = 0.25 s (HOLD_CNTL_GRPx[5:3] = 001)
  - Hold OFF = 0.5 s (HOLD_CNTL_GRPx[2:0] = 010)
- t1 (step time) = cycle time (0.5 ms) × multiple (64) = 32 ms
- Step current = ramp_rate × I_{ref} = 50 × 225 µA = 11.25 mA

- S (total steps) = (IREF_GRPx ÷ ramp_rate) = (250 ÷ 50) = 5 steps
- T (ramp time) = (S + 1) × t1 = 6 × 32 ms = 192 ms

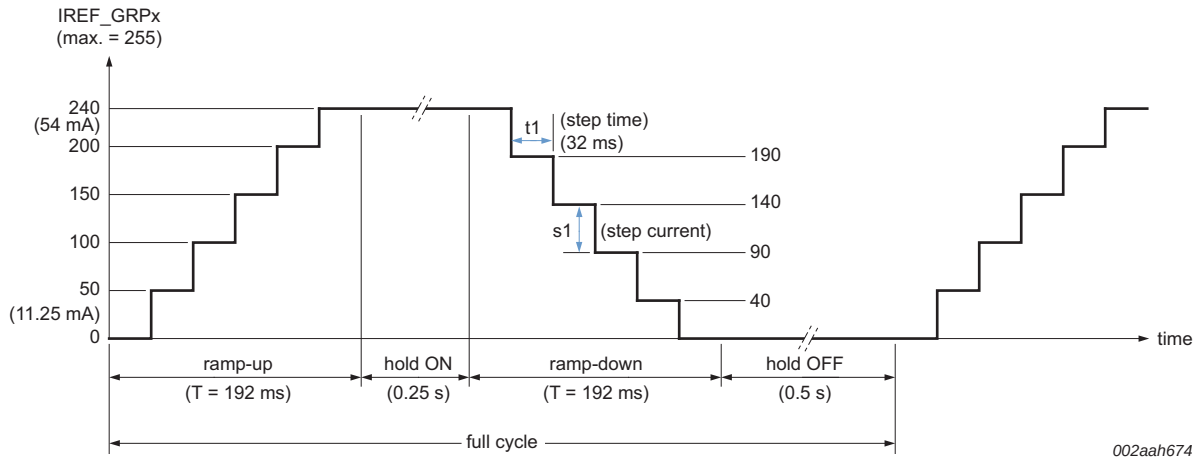


Fig 8. Ramp calculation example 2

Calculation example 2:

- Assumption:
  - I_{ref} = 225 μA if REXT = 1 kΩ
  - Output hold ON current = 225 μA × 240 = 54 mA (IREF_GRPx[7:0] = F0h)
  - Cycle time = 0.5 ms (STEP_TIME_GRPx[6] = 0)
  - Multiple factor = 64 (STEP_TIME_GRPx[5:0] = 3Fh)
  - Ramp rate = 50 (RAMP_RATE_GRPx[5:0] = 31h)
  - Hold ON = 0.25 s (HOLD_CNTL_GRPx[5:3] = 001)
  - Hold OFF = 0.5 s (HOLD_CNTL_GRPx[2:0] = 010)
- t1 (step time) = cycle time (0.5 ms) × multiple (64) = 32 ms
- Step current = ramp_rate × I_{ref} = 50 × 225 μA = 11.25 mA (except the last one)
- S (total steps) = IREF_GRPx ÷ ramp_rate = 240 ÷ 50 = 4.8 steps (round up to next integer) = 5 steps
- T (ramp time) = (S + 1) × t1 = 6 × 32 ms = 192 ms

	(enable bit) Ramp UP	(enable bit) Hold ON	(enable bit) Ramp DOWN	(enable bit) Hold OFF	Single shot waveform	Continuous waveform
1	0	0	0	0		
2	1	0	0	0		
3	0	1	0	0		
4	1	1	0	0		
5	0	0	1	0		
6	1	0	1	0		
7	0	1	1	0		
8	1	1	1	0		
9	0	0	0	1		
10	1	0	0	1		
11	0	1	0	1		
12	1	1	0	1		
13	0	0	1	1		
14	1	0	1	1		
15	0	1	1	1		
16	1	1	1	1		

Fig 9. Gradation output waveform in single shot or continuous mode

7.3.9 OFFSET — LEDn output delay offset register

Table 22. OFFSET - LEDn output delay offset register (address 3Fh) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
3Fh	OFFSET	7:4	read only	0000*	not used
		3:0	R/W	1000*	LEDn output delay offset factor

The PCA9955B can be programmed to have turn-on delay between LED outputs. This helps to reduce peak current for the V_{DD} supply and reduces EMI.

The order in which the LED outputs are enabled will always be the same (channel 0 will enable first and channel 15 will enable last).

OFFSET control register bits [3:0] determine the delay used between the turn-on times as follows:

0000 = no delay between outputs (all on, all off at the same time)

0001 = delay of 1 clock cycle (125 ns) between successive outputs

0010 = delay of 2 clock cycles (250 ns) between successive outputs

0011 = delay of 3 clock cycles (375 ns) between successive outputs

:

1111 = delay of 15 clock cycles (1.875 μs) between successive outputs

Example: If the value in the OFFSET register is 1000 the corresponding delay = 8 × 125 ns = 1 μs delay between successive outputs.

channel 0 turns on at time 0 μs

channel 1 turns on at time 1 μs

channel 2 turns on at time 2 μs

channel 3 turns on at time 3 μs

channel 4 turns on at time 4 μs

channel 5 turns on at time 5 μs

channel 6 turns on at time 6 μs

channel 7 turns on at time 7 μs

channel 8 turns on at time 8 μs

channel 9 turns on at time 9 μs

channel 10 turns on at time 10 μs

channel 11 turns on at time 11 μs

channel 12 turns on at time 12 μs

channel 13 turns on at time 13 μs

channel 14 turns on at time 14 μs

channel 15 turns on at time 15 μs

7.3.10 LED Sub Call I²C-bus addresses for PCA9955B

Table 23. SUBADR1 to SUBADR3 - I²C-bus subaddress registers 1 to 3 (address 40h to 42h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
40h	SUBADR1	7:1	A1[7:1]	R/W	1110 110*	I²C-bus subaddress 1
		0	A1[0]	R only	0*	reserved
41h	SUBADR2	7:1	A2[7:1]	R/W	1110 110*	I²C-bus subaddress 2
		0	A2[0]	R only	0*	reserved
42h	SUBADR3	7:1	A3[7:1]	R/W	1110 110*	I²C-bus subaddress 3
		0	A3[0]	R only	0*	reserved

Default power-up values are ECh, ECh, ECh. At power-up, SUBADR1 is enabled while SUBADR2 and SUBADR3 are disabled. The power-up default bit subaddress of ECh indicates that this device is a 16-channel LED driver.

All three subaddresses are programmable. Once subaddresses have been programmed to their right values, SUBx bits need to be set to logic 1 in order to have the device acknowledging these addresses (MODE1 register) (0). When SUBx is set to logic 1, the corresponding I²C-bus subaddress can be used during either an I²C-bus read or write sequence.

7.3.11 ALLCALLADR, LED All Call I²C-bus address

Table 24. ALLCALLADR - LED All Call I²C-bus address register (address 43h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
43h	ALLCALLADR	7:1	AC[7:1]	R/W	1110 000*	ALLCALL I²C-bus address register
		0	AC[0]	R only	0*	reserved

The LED All Call I²C-bus address allows all the PCA9955Bs on the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to logic 1 [power-up default state]). This address is programmable through the I²C-bus and can be used during either an I²C-bus read or write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I²C-bus address are valid. The LSB in ALLCALLADR register is a read-only bit (0).

If ALLCALL bit = 0 in MODE1 register, the device does not acknowledge the address programmed in register ALLCALLADR.

7.3.12 PWMALL — brightness control for all LEDn outputs

When programmed, the value in this register will be used for PWM duty cycle for all the LEDn outputs and will be reflected in PWM0 through PWM15 registers.

Table 25. PWMALL - brightness control for all LEDn outputs register (address 44h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
44h	PWMALL	7:0	write only	0000 0000*	duty cycle for all LEDn outputs

Remark: Write to any of the PWM0 to PWM15 registers will overwrite the value in corresponding PWMn register programmed by PWMALL.

7.3.13 IREFALL register: output current value for all LED outputs

The output current setting for all outputs is held in this register. When this register is written to or updated, all LED outputs will be set to a current corresponding to this register value.

Writes to IREF0 to IREF15 will overwrite the output current settings.

Table 26. IREFALL - Output gain control for all LED outputs (address 45h) bit description

*Legend: * default value.*

Address	Register	Bit	Access	Value	Description
45h	IREFALL	7:0	write only	00h*	Current gain setting for all LED outputs.

7.3.14 LED driver constant current outputs

In LED display applications, PCA9955B provides nearly no current variations from channel to channel and from device to device. The maximum current skew between channels is less than ±4 % and less than ±6 % between devices.

7.3.14.1 Adjusting output current

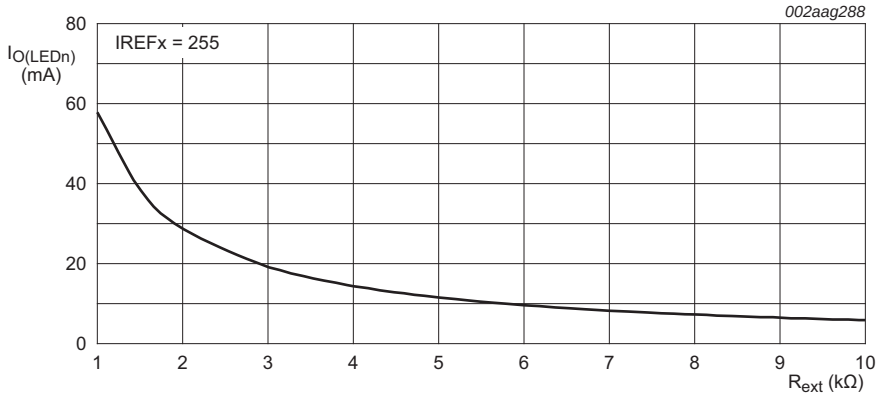
The PCA9955B scales up the reference current (I_{ref}) set by the external resistor (R_{ext}) to sink the output current (I_O) at each output port. The maximum output current for the outputs can be set using R_{ext}. In addition, the constant value for current drive at each of the outputs is independently programmable using command registers IREF0 to IREF15. Alternatively, programming the IREFALL register allows all outputs to be set at one current value determined by the value in IREFALL register.

Equation 4 and Equation 5 can be used to calculate the minimum and maximum constant current values that can be programmed for the outputs for a chosen R_{ext}.

$$I_O\_LED\_MIN = \frac{900\ mV}{R_{ext}} \times \frac{1}{4}\ (\text{minimum constant current}) \quad (4)$$

$$I_O\_LED\_MAX = (255 \times I_O\_LED\_MIN) = \left(\frac{900\ mV}{R_{ext}} \times \frac{255}{4}\right) \quad (5)$$

For a given IREFx setting, $I_O\_LED = IREFx \times \frac{900\ mV}{R_{ext}} \times \frac{1}{4}$.



$I_{O(LEDn)}$ (mA) = IREFx × (0.9 / 4) / R_{ext} (kΩ)

maximum $I_{O(LEDn)}$ (mA) = 255 × (0.9 / 4) / R_{ext} (kΩ)

Remark: Default IREFx at power-up = 0

Fig 10. Maximum I_{LED} versus R_{ext}

Example 1: If R_{ext} = 1 kΩ, I_O_LED_MIN = 225 μA, I_O_LED_MAX = 57.375 mA (as shown in Figure 11).

So each channel can be programmed with its individual IREFx in 256 steps and in 225 μA increments to a maximum output current of 57.375 mA independently.

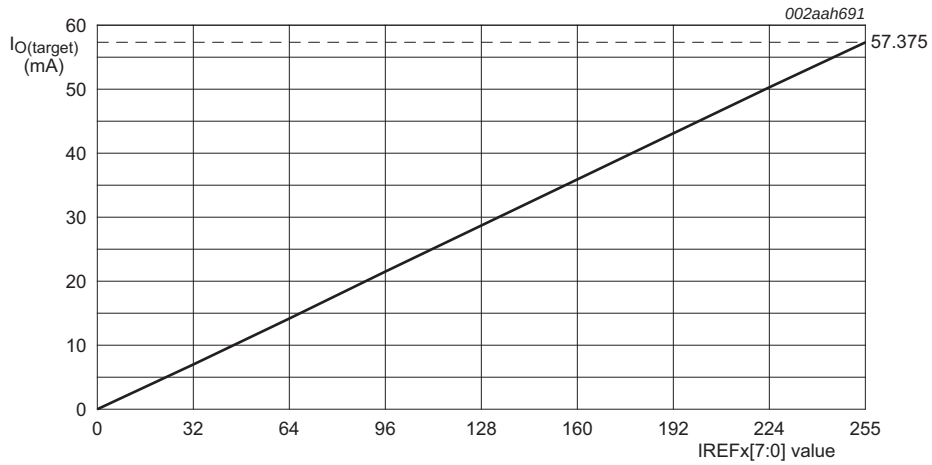


Fig 11. $I_{O(target)}$ versus IREFx value with R_{ext} = 1 kΩ

Example 2: If R_{ext} = 2 kΩ, I_O_LED_MIN = 112.5 μA, I_O_LED_MAX = 28.687 mA (as shown in Figure 12).

So each channel can be programmed with its individual IREFx in 256 steps and in 112.5 μA increments to a maximum output channel of 28.687 mA independently.

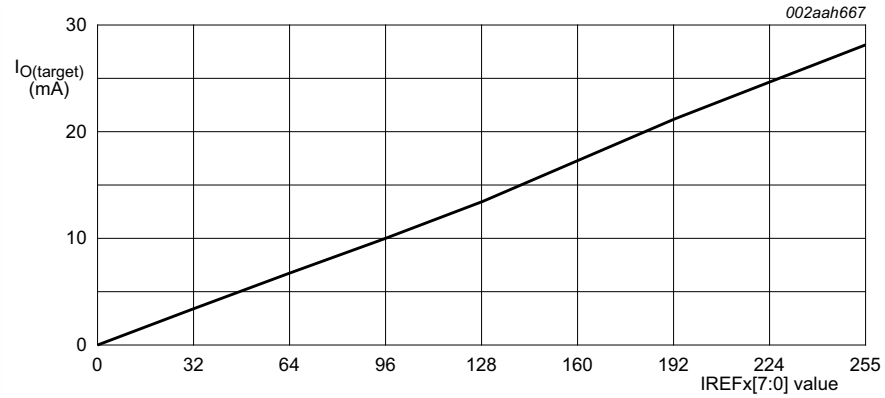


Fig 12. $I_{O(target)}$ versus IREFx value with R_{ext} = 2 kΩ

7.3.15 LED error detection

The PCA9955B is capable of detecting an LED open or a short condition at its open-drain LED outputs. Users will recognize these faults by reading the status of a pair of error bits (ERRx) in error flag registers (EFLAGn) for each channel. Both LDRx value in LEDOUTx registers and IREFx value must be set to '00' for those unused LED output channels. If the output is selected to be fully on, individual dim, or individual and group dim, that channel will be tested.

The user can poll the ERROR status bit (bit 6 in MODE2 register) to check if there is a fault condition in any of the 16 channels. The EFLAGn registers can then be read to determine which channels are at fault and the type of fault in those channels. The error status reported by the EFLAGn register is real time information that will get self cleared once the error is fixed and write '1' to CLRERR bit (bit 4 in MODE2 register).

Remark: When LED outputs programmed with LDRx = 10 or 11 in LEDOUT[3:0] registers, checks for open and short-circuit will not occur if the PWM value in PWM0 to PWM15 registers is less than 8 or 255 (100 % duty cycle).

Table 27. EFLAG0 to EFLAG3 - Error flag registers (address 46h to 49h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
46h	EFLAG0	7:6	ERR3	R only	00*	Error status for LED3 output
		5:4	ERR2	R only	00*	Error status for LED2 output
		3:2	ERR1	R only	00*	Error status for LED1 output
		1:0	ERR0	R only	00*	Error status for LED0 output
47h	EFLAG1	7:6	ERR7	R only	00*	Error status for LED7 output
		5:4	ERR6	R only	00*	Error status for LED6 output
		3:2	ERR5	R only	00*	Error status for LED5 output
		1:0	ERR4	R only	00*	Error status for LED4 output
48h	EFLAG2	7:6	ERR11	R only	00*	Error status for LED11 output
		5:4	ERR10	R only	00*	Error status for LED10 output
		3:2	ERR9	R only	00*	Error status for LED9 output
		1:0	ERR8	R only	00*	Error status for LED8 output
49h	EFLAG3	7:6	ERR15	R only	00*	Error status for LED15 output
		5:4	ERR14	R only	00*	Error status for LED14 output
		3:2	ERR13	R only	00*	Error status for LED13 output
		1:0	ERR12	R only	00*	Error status for LED12 output

Table 28. ERRx bit description

LED error detection status	ERRx		Description
	Bit 1	Bit 0	
No error	0	0	In normal operation and no error
Short-circuit	0	1	Detected LED short-circuit condition
Open-circuit	1	0	Detected LED open-circuit condition
DNE (Do Not Exist)	1	1	This condition does not exist

7.3.15.1 Open-circuit detection principle

The PCA9955B LED open-circuit detection compares the effective current level I_O with the open load detection threshold current $I_{th(det)}$. If I_O is below the threshold $I_{th(det)}$, the PCA9955B detects an open load condition. This error status can be read out as an error flag through the EFLAGn registers. For open-circuit error detection of an output channel, that channel must be ON.

Table 29. Open-circuit detection

State of output port	Condition of output current	Error status code	Description
OFF	I_O = 0 mA	0	detection not possible
ON	$I_O < I_{th(det)}$[1]	1	open-circuit
	$I_O \geq I_{th(det)}$[1]	this channel open error status bit is 0	normal

[1] $I_{th(det)} = 0.5 \times I_{O(target)}$ (typical). This threshold may be different for each I/O and only depends on IREFx and R_{ext}.

7.3.15.2 Short-circuit detection principle

The LED short-circuit detection compares the effective output voltage level (V_O) with the shorted-load detection threshold voltages $V_{th(trig)}$. If V_O is above the $V_{th(trig)}$ threshold, the PCA9955B detects a shorted-load condition. If V_O is below the $V_{th(trig)}$ threshold, no error is detected and error bit is set to '0'. This error status can be read out as an error flag through the EFLAGn registers. For short-circuit error detection of an output channel, that channel must be ON.

Table 30. Short-circuit detection

State of output port	Condition of output voltage	Error status code	Description
OFF	-	0	detection not possible
ON	$V_O \geq V_{th(trig)}$[1]	1	short-circuit
	$V_O < V_{th(trig)}$[1]	this channel short error status bit is 0	normal

[1] $V_{th} \approx 2.85$ V.

Remark: The error status distinguishes between an LED short condition and an LED open condition. Upon detecting an LED short or open, the corresponding LED outputs should be turned OFF to prevent heat dissipation for a short in the chip. Although an open event will not be harmful, the outputs should be turned OFF for both occasions to repair the LED string.

7.3.16 Overtemperature protection

If the PCA9955B chip temperature exceeds its limit ($T_{th(otp)}$ rising, see Table 33), all output channels will be disabled until the temperature drops below its limit minus a small hysteresis ($T_{th(otp)}$ hysteresis, see Table 33). When an overtemperature situation is encountered, the OVERTEMP flag (bit 7) is set in the MODE2 register. Once the die temperature reduces below the $T_{th(otp)}$ rising − $T_{th(otp)}$ hysteresis, the chip will return to the same condition it was prior to the overtemperature event and the OVERTEMP flag will be cleared.

7.4 Active LOW output enable input

The active LOW output enable ($\overline{OE}$) pin on PCA9955B allows to enable or disable all the LED outputs at the same time.

- When a LOW level is applied to $\overline{OE}$ pin, all the LED outputs are enabled.
- When a HIGH level is applied to $\overline{OE}$ pin, all the LED outputs are high-impedance.

The $\overline{OE}$ pin can be used as a synchronization signal to switch on/off several PCA9955B devices at the same time when LED drive output state is set fully ON (LDRx = 01 in LEDOUTx register) in these devices. This requires an external clock reference that provides blinking period and the duty cycle.

The $\overline{OE}$ pin can also be used as an external dimming control signal. The frequency of the external clock must be high enough not to be seen by the human eye, and the duty cycle value determines the brightness of the LEDs.

Remark: Do not use $\overline{OE}$ as an external blinking control signal when internal global blinking is selected (DMBLNK = 1, MODE2 register) since it will result in an undefined blinking pattern. Do not use $\overline{OE}$ as an external dimming control signal when internal global dimming is selected (DMBLNK = 0, MODE2 register) since it will result in an undefined dimming pattern.

7.5 Power-on reset

When power is applied to V_{DD}, an internal power-on reset holds the PCA9955B in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9955B registers and I²C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, V_{DD} must be pulled lower than 1 V and stay LOW for longer than 20 μs. The device will reset itself, and allow 2 ms for the device to fully wake up.

7.6 Hardware reset recovery

When a reset of PCA9955B is activated using an active LOW input on the $\overline{RESET}$ pin, a reset pulse width of 2.5 μs minimum is required. The maximum wait time after $\overline{RESET}$ pin is released is 1.5 ms.

7.7 Software reset

The Software Reset Call (SWRST Call) allows all the devices in the I²C-bus to be reset to the power-up state value through a specific formatted I²C-bus command. To be performed correctly, it implies that the I²C-bus is functional and that there is no device hanging the bus.

The maximum wait time after software reset is 1 ms.

The SWRST Call function is defined as the following:

1. A START command is sent by the I²C-bus master.
2. The reserved General Call address '0000 000' with the R/$\overline{W}$ bit set to '0' (write) is sent by the I²C-bus master.
3. The PCA9955B device(s) acknowledge(s) after seeing the General Call address '0000 0000' (00h) only. If the R/$\overline{W}$ bit is set to '1' (read), no acknowledge is returned to the I²C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte with 1 specific value (SWRST data byte 1):
   a. Byte 1 = 06h: the PCA9955B acknowledges this value only. If byte 1 is not equal to 06h, the PCA9955B does not acknowledge it.

   If more than 1 byte of data is sent, the PCA9955B does not acknowledge any more.
5. Once the correct byte (SWRST data byte 1) has been sent and correctly acknowledged, the master sends a STOP condition to end the SWRST function: the PCA9955B then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

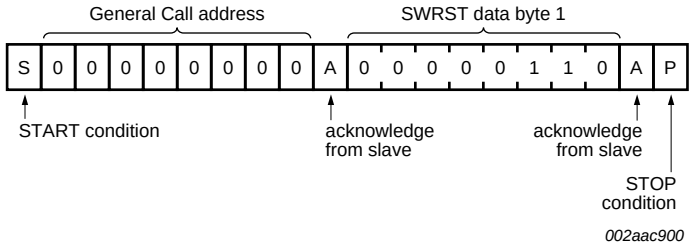


Fig 13. SWRST Call

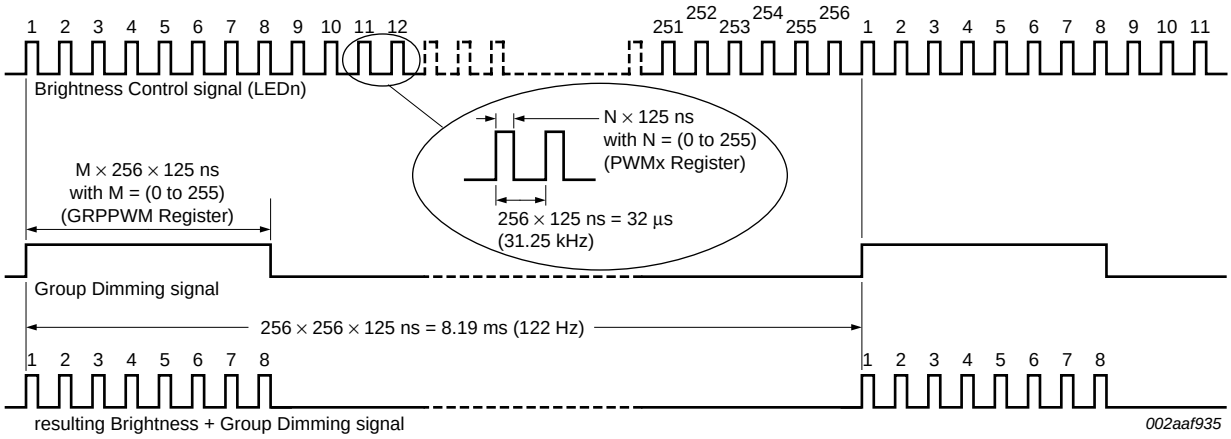
The I²C-bus master must interpret a non-acknowledge from the PCA9955B (at any time) as a 'SWRST Call Abort'. The PCA9955B does not initiate a reset of its registers. This happens only when the format of the SWRST Call sequence is not correct.

7.8 Individual brightness control with group dimming/blinking

A 31.25 kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 16 LED outputs LED0 to LED15).

- A lower 122 Hz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 15 Hz to every 16.8 seconds (8 bits, 256 steps) with programmable duty cycle (8 bits, 256 steps) is used to provide a global blinking control.



Minimum pulse width for LEDn Brightness Control is 125 ns

Minimum pulse width for Group Dimming is 32 µs

When M = 1 (GRPPWM register value), the resulting LEDn Brightness Control + Group Dimming signal will have 1 pulse of the LED Brightness Control signal (pulse width = N × 125 ns, with 'N' defined in PWMx register)

This resulting Brightness + Group Dimming signal above shows a resulting Control signal with M = 8

Fig 14. Brightness + Group Dimming signals

8. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 15).

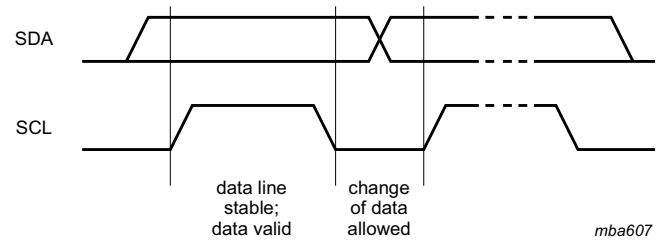


Fig 15. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 16).

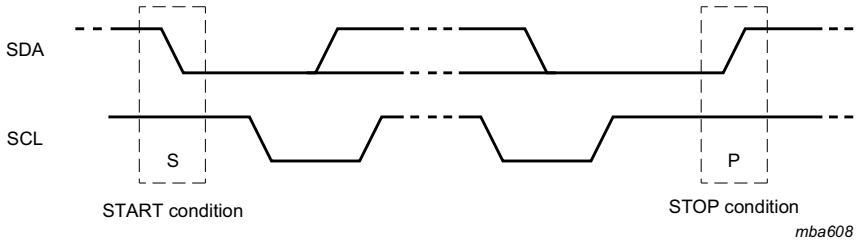


Fig 16. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 17).

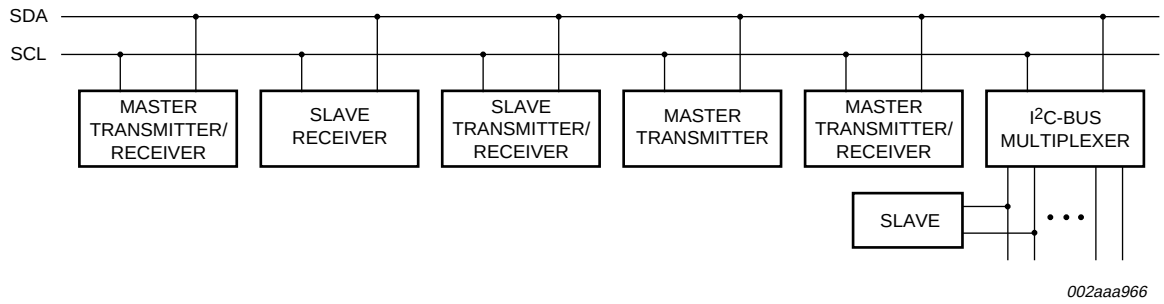


Fig 17. System configuration

8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

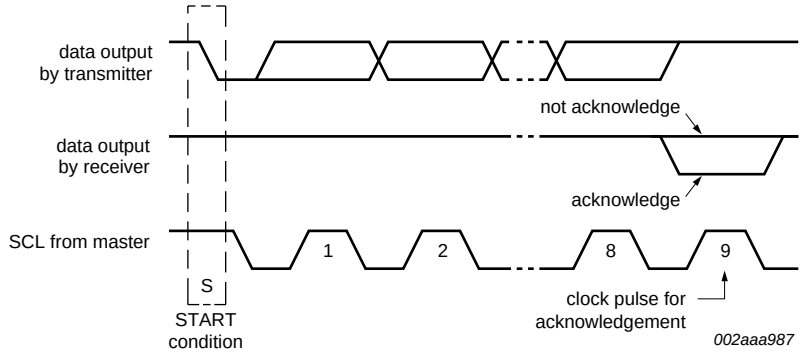
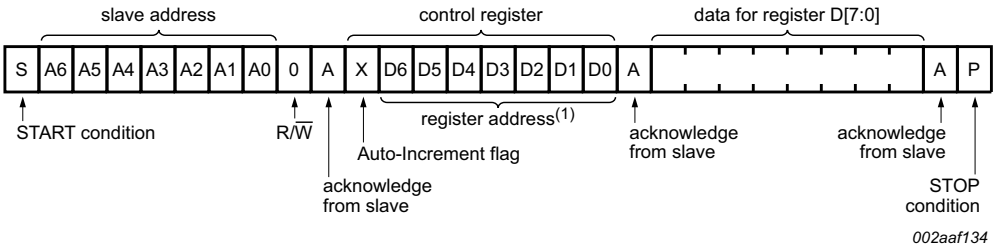


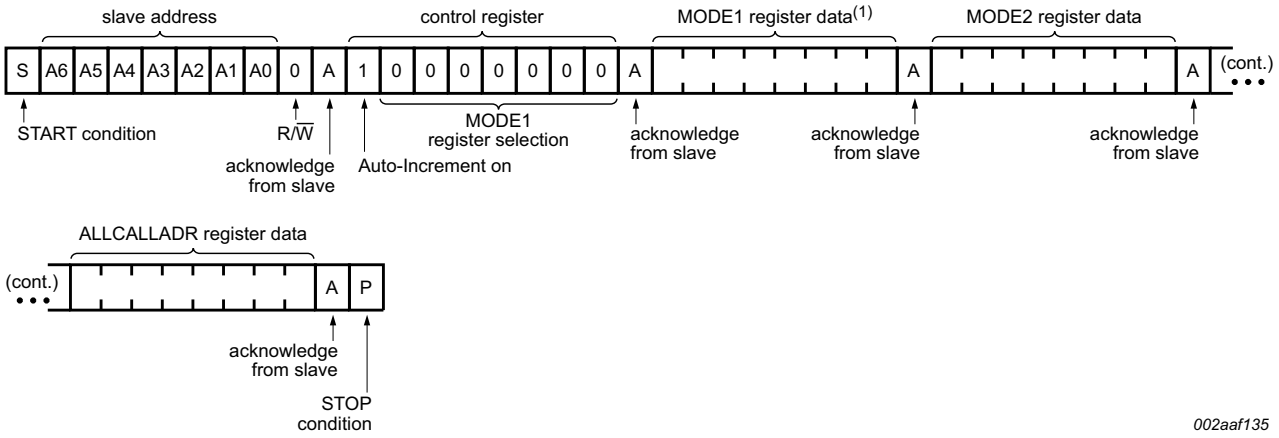
Fig 18. Acknowledgement on the I²C-bus

9. Bus transactions



(1) See Table 7 for register definition

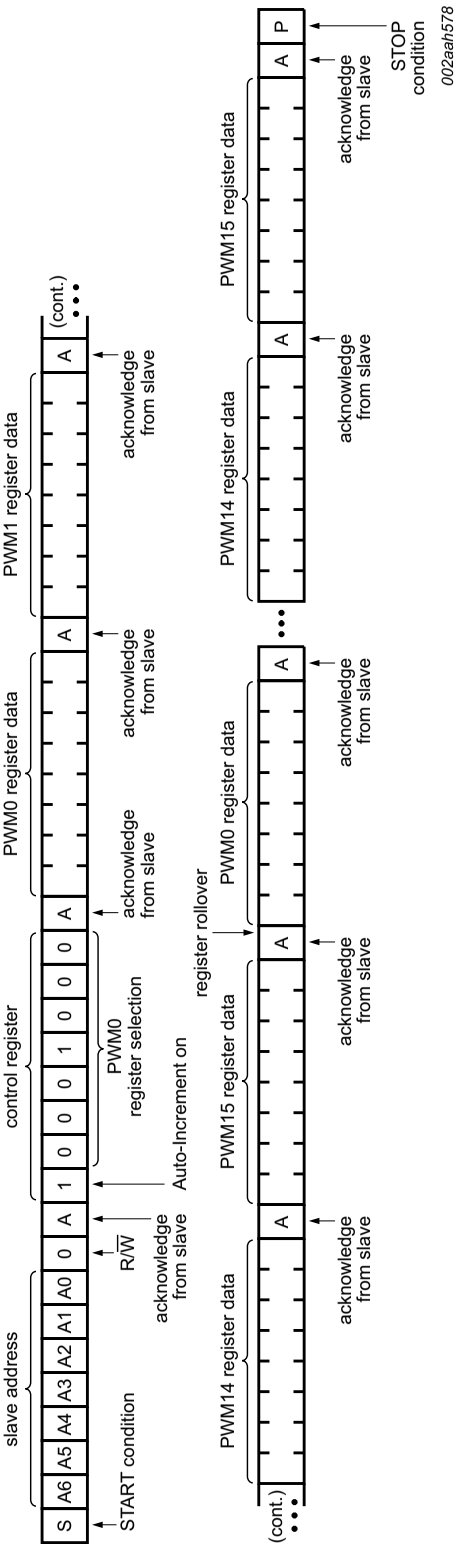
Fig 19. Write to a specific register



(1) AI1, AI0 = 00. See Table 6 for Auto-Increment options

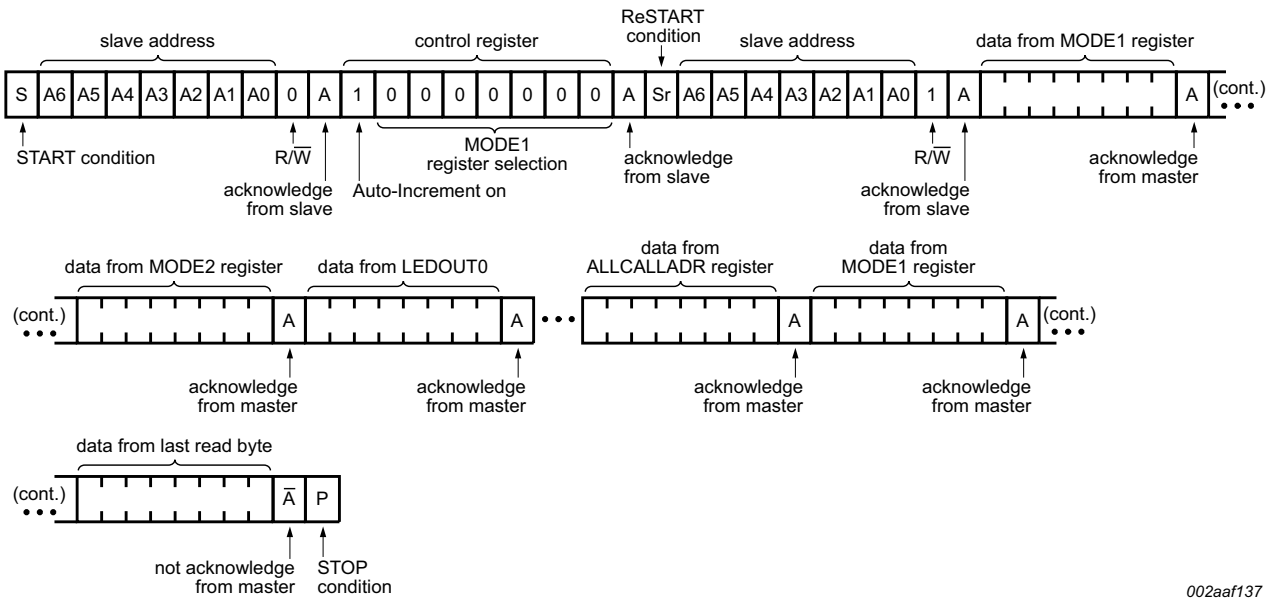
Remark: Care should be taken to load the appropriate value here in the AI1 and AI0 bits of the MODE1 register for programming the part with the required Auto-Increment options

Fig 20. Write to all registers using the Auto-Increment feature



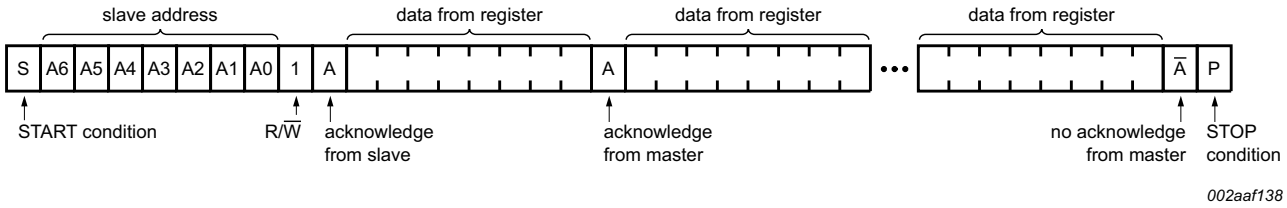
This example assumes that AIF + AI[1:0] = 101b

Fig 21. Multiple writes to Individual Brightness registers only using the Auto-Increment feature



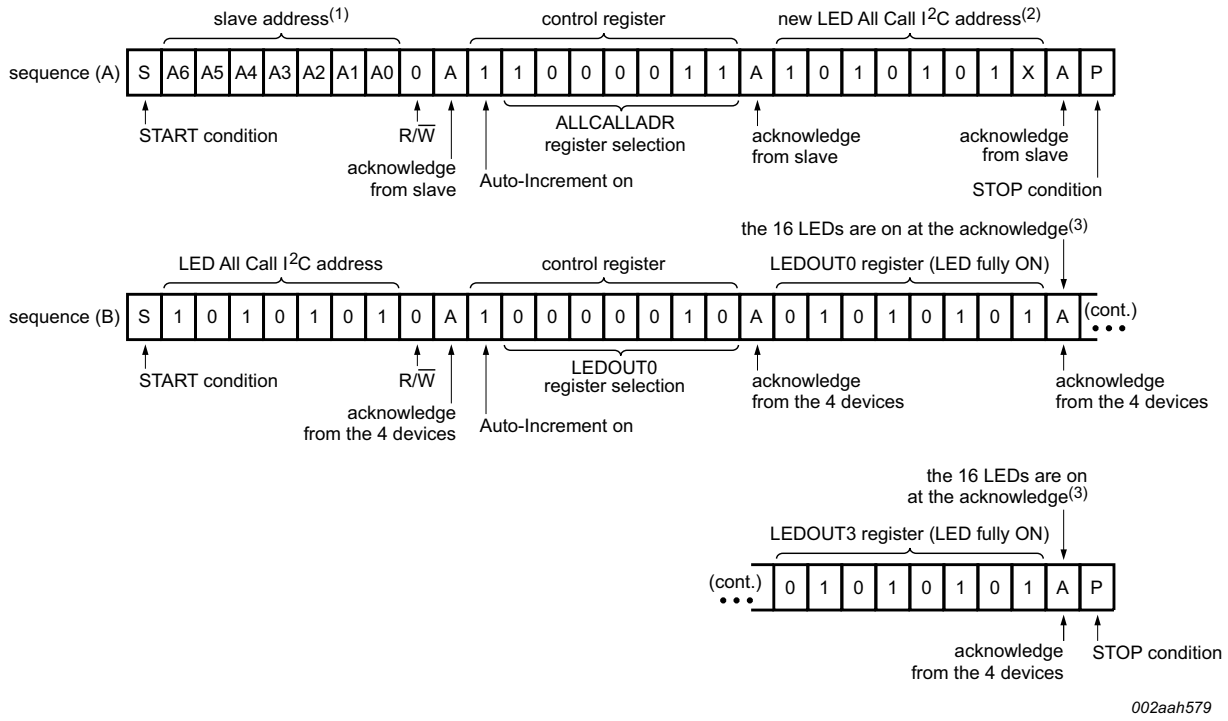
This example assumes that the MODE1[5] = 0 and MODE1[6] = 0

Fig 22. Read all registers using the Auto-Increment feature



Remark: A read operation can be done without doing a write operation before it. In this case, the data sent out is from the register pointed to by the control register (written to during the last write operation) with the Auto-Increment options in the MODE1 register (written to during the last write operation)

Fig 23. Read of registers



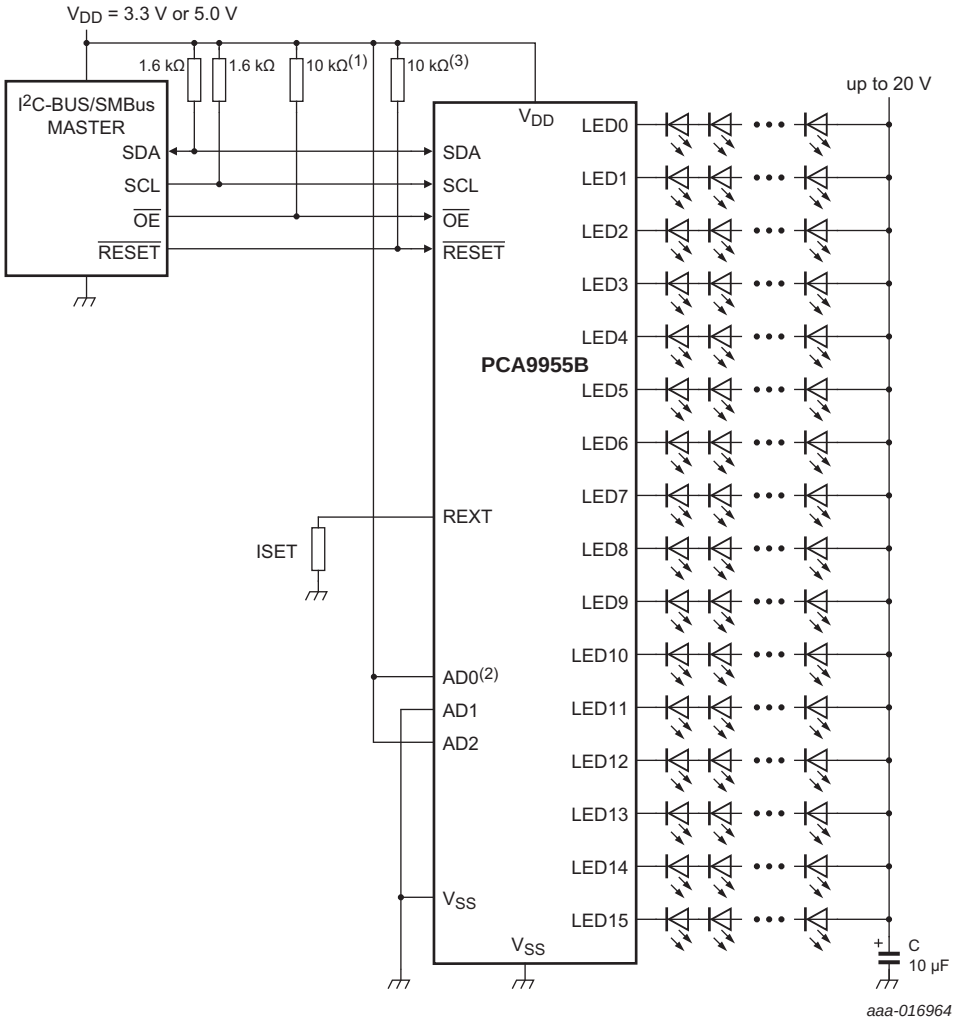
(1) In this example, several PCA9955Bs are used and the same sequence (A) (above) is sent to each of them

(2) ALLCALL bit in MODE1 register is previously set to 1 for this example

(3) OCH bit in MODE2 register is previously set to 1 for this example

Fig 24. LED All Call I²C-bus address programming and LED All Call sequence example

10. Application design-in information



(1) $\overline{OE}$ requires pull-up resistor if control signal from the master is open-drain

(2) I²C-bus address = 1101001 when AD0, AD2 tied to V_{DD} and AD1 tied to V_{SS} (see Table 5)

(3) $\overline{RESET}$ requires a pull-up resistor of <100 kΩ if not used or connected to open-drain output

Fig 25. Typical application

10.1 Thermal considerations

Since the PCA9955B device integrates 16 linear current sources, thermal considerations should be taken into account to prevent overheating, which can cause the device to go into thermal shutdown.

Perhaps the major contributor for device's overheating is the LED forward voltage mismatch. This is because it can cause significant voltage differences between the LED strings of the same type (for example, 2 V to 3 V), which ultimately translates into higher power dissipation in the device. The voltage drop across the LED channels of the device is given by the difference between the supply voltage and the LED forward voltage of each

LED string. Reducing this to a minimum (for example, 0.8 V) helps to keep the power dissipation down. Therefore LEDs binning is recommended to minimize LED voltage forward variation and reduce power dissipation in the device.

In order to ensure that the device will not go into thermal shutdown when operating under certain application conditions, its junction temperature (T_j) should be calculated to ensure that is below the overtemperature threshold limit (130 °C). The T_j of the device depends on the ambient temperature (T_{amb}), device's total power dissipation (P_{tot}), and thermal resistance.

The device junction temperature can be calculated by using the following equation:

$$T_j = T_{amb} + R_{th(j-a)} \times P_{tot} \quad (6)$$

where:

T_j = junction temperature

T_{amb} = ambient temperature

$R_{th(j-a)}$ = junction to ambient thermal resistance

P_{tot} = (device) total power dissipation

An example of this calculation is show below:

Conditions:

T_{amb} = 50 °C

$R_{th(j-a)}$ = 39 °C/W (per JEDEC 51 standard for multilayer PCB)

I_{LED} = 30 mA / channel

$I_{DD(max)}$ = 20 mA

V_{DD} = 5 V

LEDs per channel = 5 LEDs / channel

LED $V_{F(typ)}$ = 3 V per LED (15 V total for 5 LEDs in series)

LED V_F mismatch = 0.2 V per LED (1 V total for 5 LEDs in series)

$V_{reg(drv)}$ = 0.8 V (This will be present only in the LED string with the highest LED forward voltage.)

V_{sup} = LED $V_{F(typ)}$ + LED V_F mismatch + $V_{reg(drv)}$ = 15 V + 1 V + 0.8 V = 16.8 V

P_{tot} calculation:

P_{tot} = IC_power + LED drivers_power;

IC_power = ($I_{DD} \times V_{DD}$) + (SDA_$V_{OL} \times I_{OL}$)

IC_power = (0.02 A × 5 V) + (0.4 V × 0.03 A) = 0.112 W

LED drivers_power = [(16 − 1) × (I_{LED}) × (LED V_F mismatch + $V_{reg(drv)}$)] + ($I_{LED} \times V_{reg(drv)}$)

LED drivers_power = [15 × 0.03 A × (1 V + 0.8 V)] + (0.03 A × 0.8 V) = 0.834 W

P_{tot} = 0.112 W + 0.834 W = 0.946 W

T_j calculation:

$T_j = T_{amb} + R_{th(j-a)} \times P_{tot}$

$T_j = 50\ °C + (39\ °C/W \times 0.946\ W) = 86.894\ °C$

This confirms that the junction temperature is below the minimum overtemperature threshold of 130 °C, which ensures the device will not go into thermal shutdown under these conditions.

It is important to mention that the value of the thermal resistance junction-to-ambient ($R_{th(j-a)}$) strongly depends in the PCB design. Therefore, the thermal pad of the device should be attached to a big enough PCB copper area to ensure proper thermal dissipation (similar to JEDEC 51 standard). Several thermal vias in the PCB thermal pad should be used as well to increase the effectiveness of the heat dissipation (for example, 15 thermal vias). The thermal vias should be distributed evenly in the PCB thermal pad.

Finally, it is important to point out that this calculation should be taken as a reference only and therefore evaluations should still be performed under the application environment and conditions to confirm proper system operation.

11. Limiting values

Table 31. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin		V_{SS} – 0.5	5.5	V
$V_{drv(LED)}$	LED driver voltage		V_{SS} – 0.5	20	V
$I_{O(LEDn)}$	output current on pin LEDn		-	65	mA
I_{SS}	ground supply current		-	1.0	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	-	2.56	W
		T_{amb} = 85 °C	-	1.03	W
		T_{amb} = 105 °C	-	0.513	W
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature	operating for non AEC-Q100 or AEC-Q100	–40	+105	°C
T_j	junction temperature		–40	+125	°C

12. Thermal characteristics

Table 32. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	HTSSOP28 [1]	39	°C/W

[1] Per JEDEC 51 standard for multilayer PCB and Wind Speed (m/s) = 0.

13. Static characteristics

Table 33. Static characteristics

V_{DD} = 3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Supply						
V_{DD}	supply voltage		3	-	5.5	V
I_{DD}	supply current	on pin V_{DD}; operating mode; f_{SCL} = 1 MHz				
		R_{ext} = 2 kΩ; LED[15:0] = off; IREFx = 00h	-	11	12	mA
		R_{ext} = 1 kΩ; LED[15:0] = off; IREFx = 00h	-	13	14	mA
		R_{ext} = 2 kΩ; LED[15:0] = on; IREFx = FFh	-	15	19	mA
		R_{ext} = 1 kΩ; LED[15:0] = on; IREFx = FFh	-	17	21	mA
I_{stb}	standby current	on pin V_{DD}; no load; f_{SCL} = 0 Hz; MODE1[4] = 1; $V_I = V_{DD}$				
		V_{DD} = 3.3 V	-	170	600	µA
		V_{DD} = 5.5 V	-	170	700	µA
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS}	-	2	-	V
V_{PDR}	power-down reset voltage	no load; $V_I = V_{DD}$ or V_{SS} [2][5]	-	1	-	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 3 V	20	-	-	mA
		V_{OL} = 0.4 V; V_{DD} = 5 V	30	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}	−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$	-	6	10	pF
Current controlled outputs (LED[15:0])						
$I_{O(LEDn)}$	output current on pin LEDn	V_O = 0.8 V; IREFx = 80h; R_{ext} = 1 kΩ	25	-	30	mA
		V_O = 0.8 V; IREFx = FFh; R_{ext} = 1 kΩ [5]	50	-	60	mA
ΔI_O	output current variation	V_{DD} = 3.0 V; T_{amb} = 25 °C; V_O = 0.8 V; IREFx = 80h; R_{ext} = 1 kΩ; guaranteed by design				
		between bits (different ICs, same channel) [3]	-	-	±6	%
		between bits (2 channels, same IC) [4]	-	-	±4	%
$V_{reg(drv)}$	driver regulation voltage	minimum regulation voltage; IREFx = FFh; R_{ext} = 1 kΩ	0.8	1	20	V
$I_{L(off)}$	off-state leakage current	V_O = 20 V	-	-	1	µA
V_{trip}	trip voltage	short LED protection; Error flag will trip during verification test if $V_O \geq V_{trip}$; R_{ext} = 1 kΩ	2.7	2.85	-	V

Table 33. Static characteristics *...continued*

V_{DD} = 3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
OE input, RESET input						
V_{IL}	LOW-level input voltage		−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	5.5	V
I_{LI}	input leakage current		−1	-	+1	µA
C_i	input capacitance	[5]	-	3.7	5	pF
Address inputs AD2, AD1, AD0						
V_I	input voltage	voltage on an input pin	−0.5	-	5.5	V
I_{LI}	input leakage current		−1	-	+1	µA
C_i	input capacitance	[5]	-	3.7	5	pF
Overtemperature protection						
$T_{th(otp)}$	overtemperature protection threshold temperature	rising [5]	130	-	150	°C
		hysteresis [5]	15	-	30	°C

[1] Typical limits at V_{DD} = 3.3 V, T_{amb} = 25 °C.

[2] V_{DD} must be lowered to 1 V in order to reset part.

[3] Part-to-part mismatch is calculated:

$$\Delta\% = \left(\frac{\left(\frac{I_{O(LED0)} + I_{O(LED1)} + \ldots + I_{O(LED14)} + I_{O(LED15)}}{16} \right) - ideal\ output\ current}{ideal\ output\ current} \right) \times 100$$

where 'ideal output current' = 28.68 mA (R_{ext} = 1 kΩ, IREFx = 80h).

[4] Channel-to-channel mismatch is calculated:

$$\Delta\% = \left(\frac{I_{O(LEDn)}\ (\text{where n = 0 to 15})}{\left(\frac{I_{O(LED0)} + I_{O(LED1)} + \ldots + I_{O(LED14)} + I_{O(LED15)}}{16} \right)} - 1 \right) \times 100$$

[5] Value not tested in production, but guaranteed by design and characterization.

14. Dynamic characteristics

Table 34. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Fast-mode Plus I²C-bus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{VD;DAT}$	data valid time	[2]	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
t_f	fall time of both SDA and SCL signals	[3][4]	-	300	$20 + 0.1C_b$[5]	300	-	120	ns
t_r	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$[5]	300	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[6]	-	50	-	50	-	50	ns
$t_{w(rst)}$	reset pulse width		2.5	-	2.5	-	2.5	-	µs

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

[4] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time (t_f) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[5] C_b = total capacitance of one bus line in pF.

[6] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

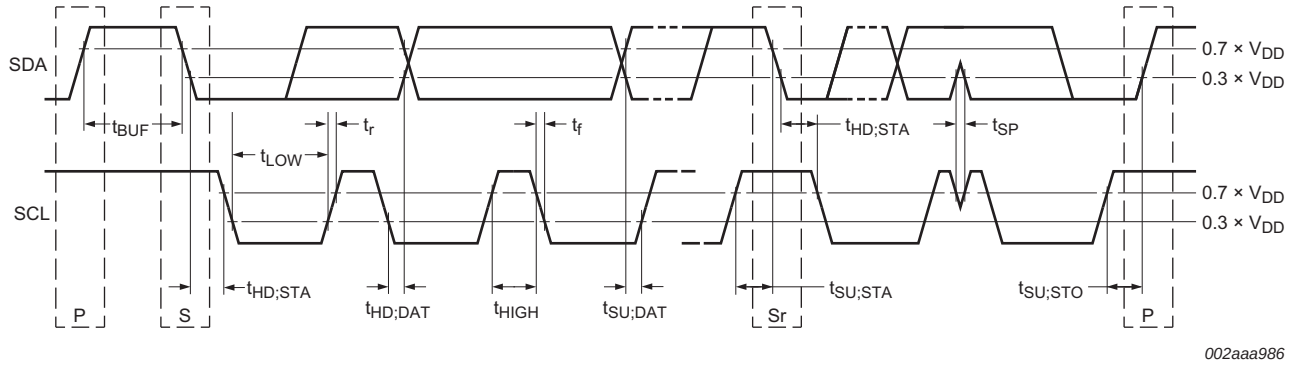
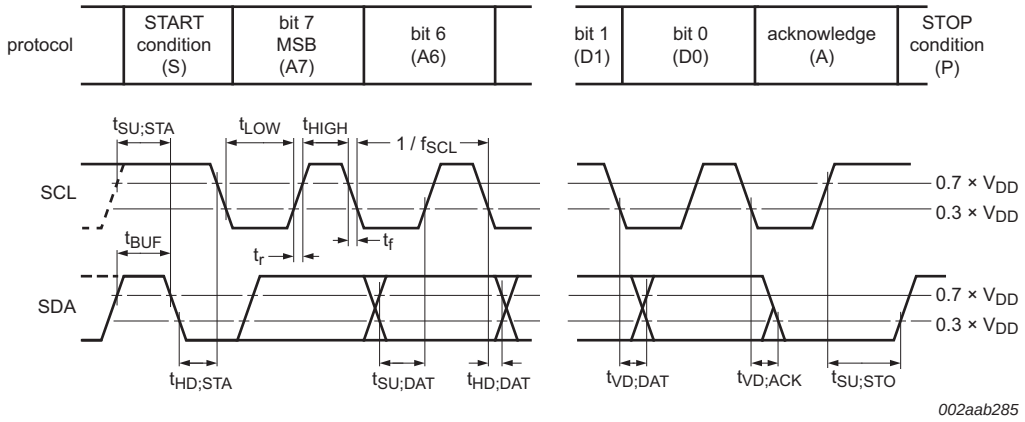


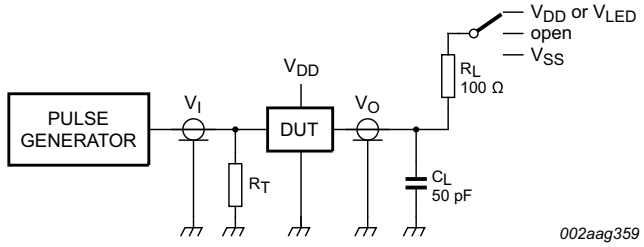
Fig 26. Definition of timing



Rise and fall times refer to V_{IL} and V_{IH}

Fig 27. I²C-bus timing diagram

15. Test information



R_L = Load resistor for LEDn

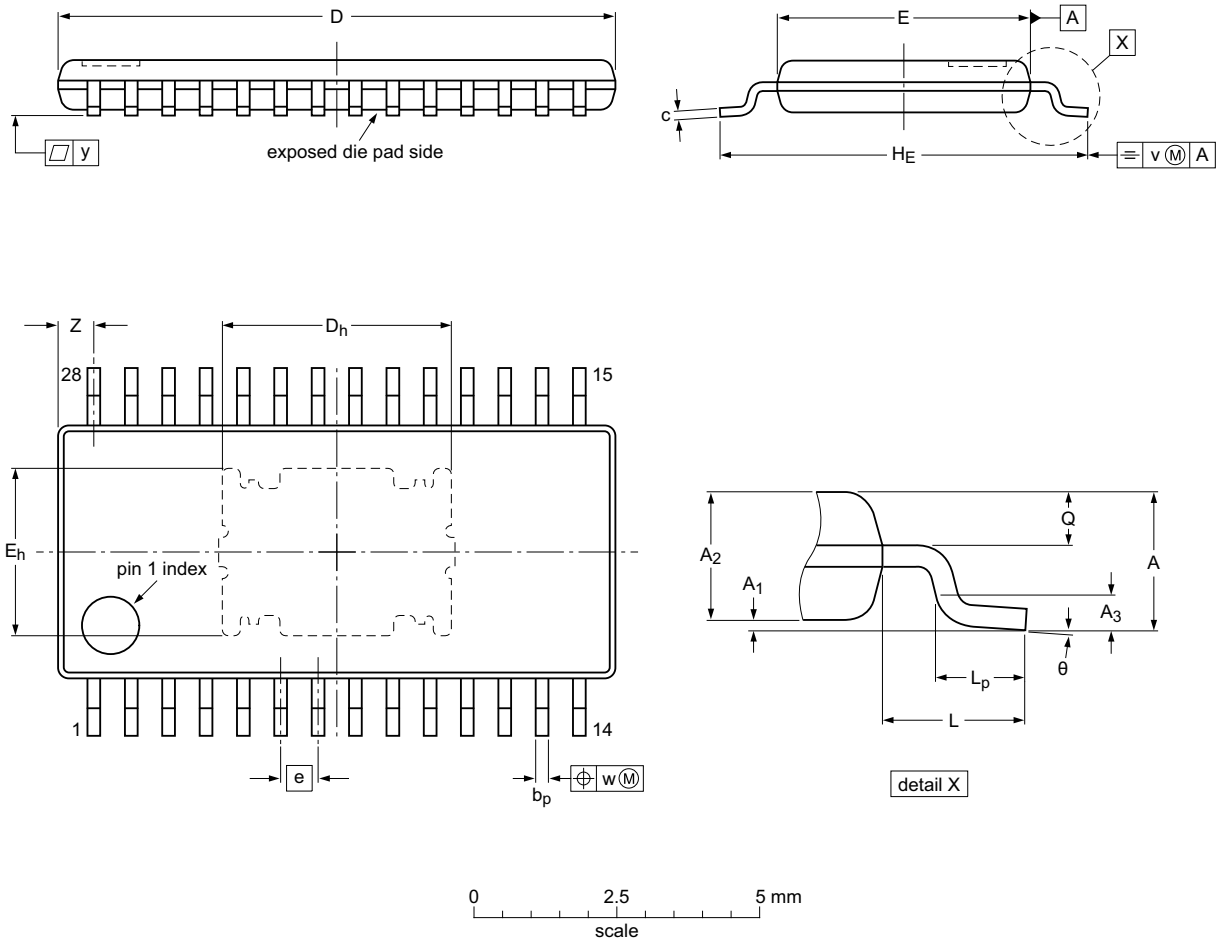
C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generators

Fig 28. Test circuitry for switching times

16. Package outline

HTSSOP28: plastic thermal enhanced thin shrink small outline package; 28 leads; body width 4.4 mm; lead pitch 0.65 mm; exposed die pad **SOT1172-3**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(2)}$	E_h	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
	max	1.1	0.15	0.95		0.30	0.20	9.8	4.1	4.5	3.0		6.6		0.75	0.40				0.80	8°
mm	nom		0.10	0.90	0.25	0.22	0.15	9.7	4.0	4.4	2.9	0.65	6.4	1.0	0.62	0.37	0.2	0.13	0.1	0.63	4°
	min		0.05	0.85		0.19	0.10	9.6	3.9	4.3	2.8		6.2		0.50	0.3				0.50	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot1172-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1172-3	- - -	MO-153	- - -			~~13-08-20~~ 13-09-12

Fig 29. Package outline SOT1172-3 (HTSSOP28)

17. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 30) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 35 and 36

Table 35. SnPb eutectic process (from J-STD-020D)

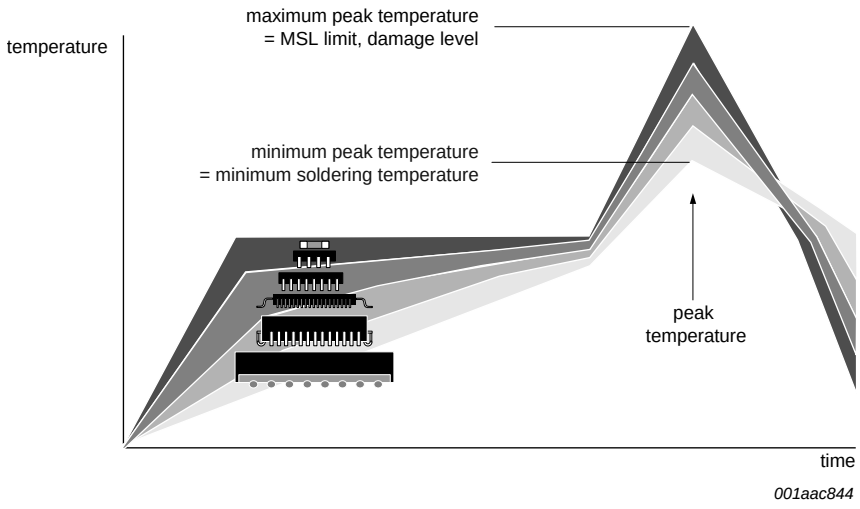
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 36. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 30.



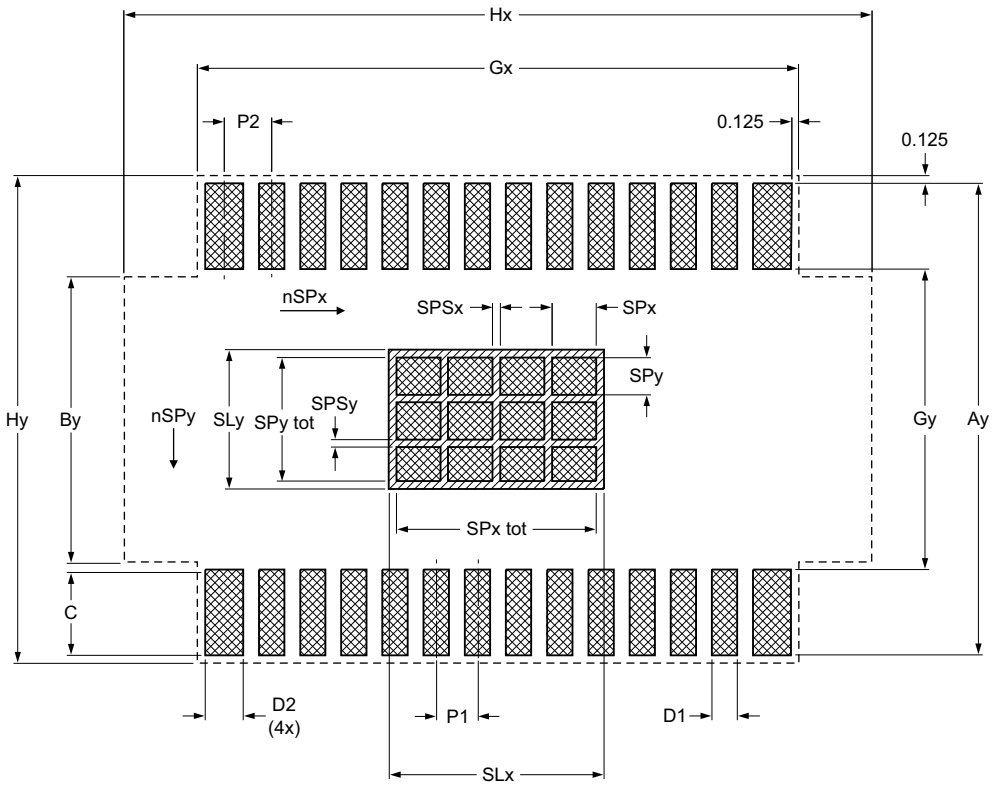
MSL: Moisture Sensitivity Level

Fig 30. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Soldering: PCB footprints

Footprint information for reflow soldering of HTSSOP28 package **SOT1172-3**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder land plus solder paste

occupied area

SPSx	SPSy	nSPx	nSPy
0.120	0.100	4	3

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.65	0.75	7.45	4.50	1.35	0.40	0.60	3.40	2.20	3.16	2.00	0.70	0.60	9.50	4.75	11.80	7.70

Issue date ~~13-08-20~~ 13-10-07

sot1172-3_fr

Fig 31. PCB footprint for SOT1172-3 (HTSSOP28); reflow soldering

20. Abbreviations

Table 37. Abbreviations

Acronym	Description
ACK	Acknowledge
CDM	Charged-Device Model
DAC	Digital-to-Analog Converter
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
LED	Light Emitting Diode
LSB	Least Significant Bit
MCU	MicroController Unit
MSB	Most Significant Bit
NMOS	Negative-channel Metal-Oxide Semiconductor
PCB	Printed-Circuit Board
PMOS	Positive-channel Metal-Oxide Semiconductor
PWM	Pulse Width Modulation
RGB	Red/Green/Blue
RGBA	Red/Green/Blue/Amber
SMBus	System Management Bus

21. Revision history

Table 38. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9955B v.2.1	20170502	Product data sheet	-	PCA9955B v.2
Modifications:	• Extended operating temperature range up to 105 °C			
PCA9955B v.2	20151120	Product data sheet	-	PCA9955B v.1
Modifications:	• Corrected Figure 1 “Block diagram of PCA9955B” • Table 3 “Pin description”: Corrected description for $\overline{\text{RESET}}$ pin • Corrected Figure 25 “Typical application”; added Figure note 3			
PCA9955B v.1	20150622	Product data sheet	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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