19-5318; Rev 1; 6/11

2.5A Step-Down Regulator with Remote Sense in 2mm x 2mm WLP

General Description

The MAX8952 high-efficiency DC-to-DC step-down switching regulator delivers up to 2.5A of output current. The device operates from a 2.5V to 5.5V input voltage range, supporting commonly-used battery technologies in handsets. The output voltage is I²C programmable from 0.77V to 1.40V. Remote sense ensures precise DC regulation at the load. Total output error is less than ±1.5% over load, line, and temperature.

The IC operates at a 3.25MHz fixed frequency. The high operating frequency minimizes the size of external components. The switching frequency of the converter can be synchronized to the master clock of the application. When synchronizing to an external clock, the IC measures the frequency of the external clock to ensure that the clock is stable before changing the switching frequency to the external clock frequency.

An on-board DAC allows adjustment of the output voltage in 10mV steps. The output voltage can be programmed directly through the I²C interface, or by preloading a set of on-board registers and using the two VID logic signals to select the appropriate register. Other features include internal soft-start control circuitry to reduce inrush current, output overvoltage, overcurrent, and overtemperature protection.

Applications

Cell Phones and Smartphones

PDAs and MP3 Players

Tablet PCs

Features

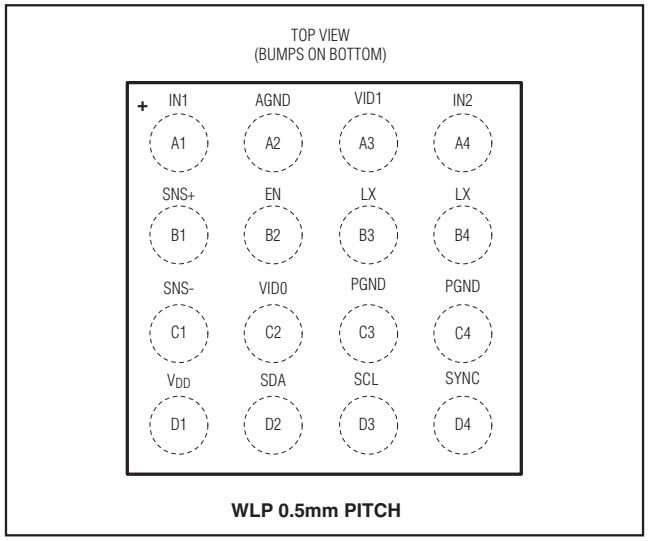
- **2.5A Guaranteed Output Current**
- **I²C Programmable V_{OUT} (770mV to 1.40V in 10mV Steps)**
- **Initial Accuracy ±0.5% at 1.40V Output**
- **±1.5% Output Accuracy Over Load, Line, and Temperature (DCR ≤ 38.5mΩ)**
- **Power-Save Mode Increases Light Load Efficiency**
- **Fixed 3.25MHz PWM Switching Frequency**
- **Small 1.0µH Inductor**
- **Synchronizes to 13MHz, 19.2MHz, or 26MHz System Clock When Available**
- **Overvoltage and Overcurrent Protection**
- **Operates from 2.5V to 5.5V Input Supply**
- **Thermal Shutdown Protection**
- **On-Chip FET and Synchronous Rectifier**
- **400kHz I²C Interface**
- **< 1µA Shutdown Current**
- **16-Bump, 2mm x 2mm WLP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8952EWE+T	-40°C to +85°C	16-Bump WLP (0.5mm pitch)

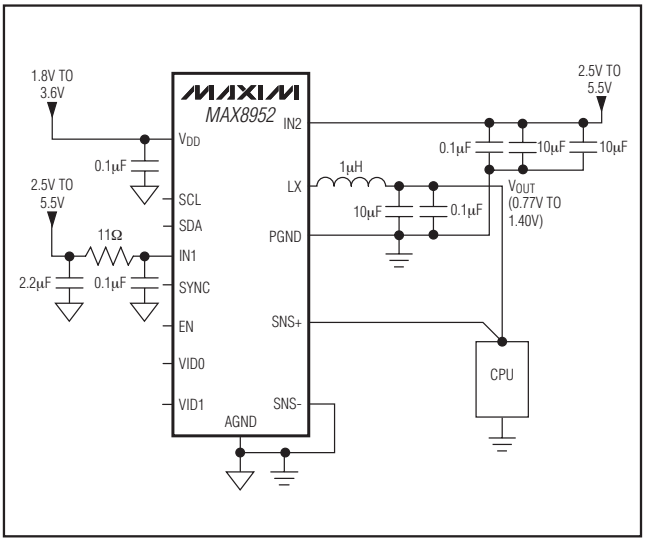
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Bump Configuration



WLP 0.5mm PITCH

Typical Operating Circuit



2.5A Step-Down Regulator with Remote Sense in 2mm x 2mm WLP

ABSOLUTE MAXIMUM RATINGS

IN1, IN2 to AGND .....-0.3V to +6.0V
V_{DD} to AGND.....-0.3V to +4.0V
LX, SNS+, VID0, VID1, EN to AGND.....-0.3V to (V_{IN1} + 0.3V)
SCL, SDA, SYNC to AGND.....-0.3V to (V_{DD} + 0.3V)
PGND, SNS- to AGND.....-0.3V to +0.3V
RMS LX Current 2500mA
Continuous Power Dissipation (T_A = +70°C)
16-Bump WLP 0.5mm Pitch
(derate 20.4mW/°C above +70°C).....1632mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....49°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7 using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{IN1} = V_{IN2} = 3.6V, V_{AGND} = V_{PGND} = 0V, V_{DD} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN1, IN2 Operating Range			2.5		5.5	V
V_{DD} Operating Range			1.8		3.6	V
V_{DD} Undervoltage Lockout (UVLO) Threshold	V_{DD} falling		0.54	0.865	1.35	V
V_{DD} UVLO Hysteresis				50		mV
IN_ Undervoltage Lockout (UVLO) Threshold	$V_{IN\_}$ falling		2.10	2.15	2.20	V
IN_ UVLO Hysteresis				70		mV
V_{DD} Shutdown Supply Current	V_{IN1} = V_{IN2} = 5.5V, EN = V_{DD} = AGND	T_A = +25°C		0.01	1	µA
		T_A = +85°C		0.01		
IN1, IN2 Shutdown Supply Current	V_{IN1} = V_{IN2} = 5.5V, EN = V_{DD} = AGND	T_A = +25°C		0.25	1	µA
		T_A = +85°C		0.25		
IN1, IN2 Standby Supply Current	V_{IN1} = V_{IN2} = 5.5V, SCL = SDA = V_{DD}, EN = AGND, I^2C ready	T_A = +25°C		0.35	1	µA
		T_A = +85°C		0.35		
V_{DD} Standby Supply Current	V_{IN1} = V_{IN2} = V_{DD} = 3.6V, SCL = SDA = V_{DD}, EN = AGND, I^2C ready	T_A = +25°C		0.02	1	µA
		T_A = +85°C		0.02		
LOGIC INTERFACE						
Logic Input High Voltage (V_{IH})	V_{IN1} = V_{IN2} = 2.5V to 5.5V, V_{DD} = 1.8V to 3.6V	EN, VID0, VID1	1.4			V
		SYNC, SCL, SDA	0.7 x V_{DD}			
Logic Input Low Voltage (V_{IL})	V_{IN1} = V_{IN2} = 2.5V to 5.5V, V_{DD} = 1.8V to 3.6V	EN, VID0, VID1			0.4	V
		SYNC, SCL, SDA			0.3 x V_{DD}	
SDA, SCL, SYNC Logic Input Current	V_{IL} = 0V or V_{IH} = 3.6V, EN = AGND	T_A = +25°C	-1	0.01	+1	µA
		T_A = +85°C		0.01		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN2} = 3.6V, V_{AGND} = V_{PGND} = 0V, V_{DD} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VID0, VID1, EN Logic Input Pulldown Resistor	Controlled by I²C command: VID0_PD = 1 VID1_PD = 1 EN_PD = 1	200	320	450	kΩ
I²C INTERFACE					
SDA Output Low Voltage	I_{SDA} = 3mA		0.03	0.4	V
I²C Clock Frequency				400	kHz
Bus-Free Time Between START and STOP	t_{BUF}	1.3			µs
Hold Time REPEATED START Condition	t_{HD_STA}	0.6	0.1		µs
SCL Low Period	t_{LOW}	1.3	0.2		µs
SCL High Period	t_{HIGH}	0.6	0.2		µs
Setup Time REPEATED START Condition	t_{SU_STA}	0.6	0.1		µs
SDA Hold Time	t_{HD_DAT}	0	-0.01		µs
SDA Setup Time	t_{SU_DAT}	0.1	0.05		µs
Setup Time for STOP Condition	t_{SU_STO}	0.6	0.1		µs
STEP-DOWN DC-DC REGULATOR					
IN1 + IN2 Supply Current	FPWM_EN_ = 0, V_{OUT} = 1.27V, no switching		54	80	µA
	FPWM_EN_ = 1, V_{OUT} = 1.27V, f_{sw} = 3.25MHz		9		mA
Minimum Output Capacitance Required for Stability	V_{OUT} = 0.77V to 1.40V, I_{OUT} = 0 to 2.5A		10		µF
OUT Voltage Range	10mV steps	0.770		1.400	V
Output Overvoltage Protection	Rising, 50mV hysteresis (typ)	1.65	1.8	1.9	V

2.5A Step-Down Regulator with Remote Sense in 2mm x 2mm WLP

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN2} = 3.6V, V_{AGND} = V_{PGND} = 0V, V_{DD} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OUT Voltage Accuracy	No load, $V_{IN\_}$ = 2.5V to 5.5V, V_{OUT} = 1.27V, FPWM_EN_ = 1		-0.5		+0.5	%
	No load, $V_{IN\_}$ = 2.5V to 5.5V, V_{OUT} = 0.77V, FPWM_EN_ = 1		-1.0		+1.0	
	No load, $V_{IN\_}$ = 2.5V to 5.5V, V_{OUT} = 1.40V, FPWM_EN_ = 1		-0.5		+0.5	
Load Regulation	R_L is the resistance from LX to SNS+ (output)			R_L/25		V/A
RAMP Timer	RAMP[2:0] = 000			32.50		mV/µs
	RAMP[2:0] = 001			16.25		
	RAMP[2:0] = 010			8.125		
	RAMP[2:0] = 011			4.063		
	RAMP[2:0] = 100			2.031		
	RAMP[2:0] = 101			1.016		
	RAMP[2:0] = 110			0.508		
	RAMP[2:0] = 111			0.254		
Peak Current Limit (p-Channel MOSFET)			3.45	4.2	4.8	A
Valley Current Limit (n-Channel MOSFET)	Hysteretic mode		2.7	3.6	4.5	A
Negative Current Limit (n-Channel MOSFET)	PWM mode		2.0	2.5	3.0	A
n-Channel Zero-Crossing Threshold				50		mA
LX pFET On-Resistance	IN2 to LX, I_{LX} = -200mA			0.08	0.16	Ω
LX nFET On-Resistance	FPWM_EN_ = 0, LX to PGND, I_{LX} = 200mA			0.06	0.12	Ω
LX Leakage	V_{LX} = 5.5V or 0V	T_A = +25°C	-1	0.03	+1	µA
		T_A = +85°C		0.05		
Operating Frequency	Internal oscillator, PWM mode		2.82	3.25	3.56	MHz
	Internal oscillator, power-save mode before entering PWM mode		2.43	3.25	4.06	
	13MHz = f_{SYNC}, SYNC[1:0] = 01			f_{SYNC}/4		
	19.2MHz = f_{SYNC}, SYNC[1:0] = 10 or 11			f_{SYNC}/6		
	26MHz = f_{SYNC}, SYNC[1:0] = 00			f_{SYNC}/8		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN2} = 3.6V, V_{AGND} = V_{PGND} = 0V, V_{DD} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Duty Cycle	Forced-PWM mode (FPWM_EN = 1), minimum duty cycle = 0%			16	%
Maximum Duty Cycle		60			%
Minimum On- and Off-Time		30	40	50	ns
OUT Discharge Resistance	During shutdown or UVLO, from SNS+ to PGND		650		Ω
SNS+, SNS- Input Impedance	V_{OUT} = 0.77V (OUT_MODEx [5:0] = 0b000000)	400	600	850	kΩ
Time Delay from PWM to Power-Save Mode	Time required for error amplifier to stabilize before switching mode		70		µs
Time Delay from Power-Save Mode to PWM	Time required for error amplifier to stabilize before switching mode		140		µs
SYNCHRONIZATION (SYNC)					
SYNC Capture Range	SYNC[1:0] = 00	18.9	26.0	38.0	MHz
	SYNC[1:0] = 1X	14.2	19.2	28.5	
	SYNC[1:0] = 01	9.5	13.0	19.0	
SYNC Pulse Width			13		ns
PROTECTION CIRCUITS					
Thermal-Shutdown Hysteresis			20		°C
Thermal Shutdown			+160		°C

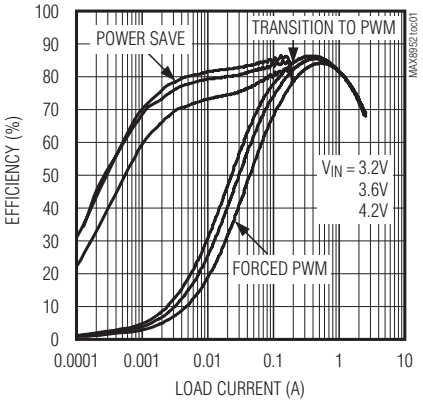
Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

2.5A Step-Down Regulator with Remote Sense in 2mm x 2mm WLP

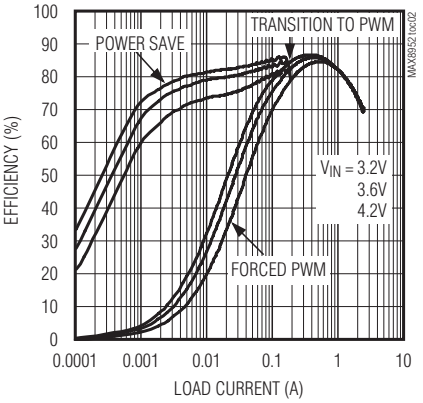
Typical Operating Characteristics

(*Typical Operating Circuit*, $V_{IN1} = V_{IN2} = 3.6V$, $V_{AGND} = V_{PGND} = 0V$, $V_{OUT} = 1.1V$, $V_{DD} = 1.8V$, $T_A = +25°C$, unless otherwise noted.)

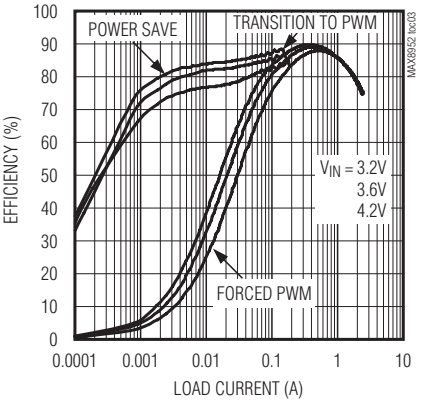
EFFICIENCY vs. LOAD CURRENT (1.0V OUTPUT, SYNC OFF)



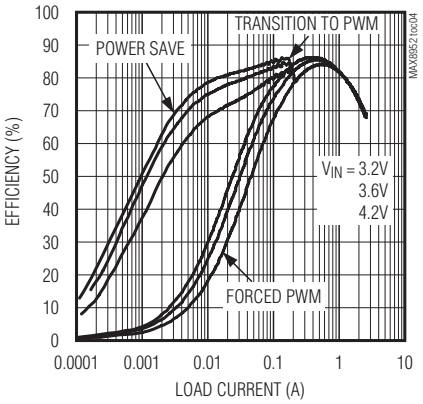
EFFICIENCY vs. LOAD CURRENT (1.1V OUTPUT, SYNC OFF)



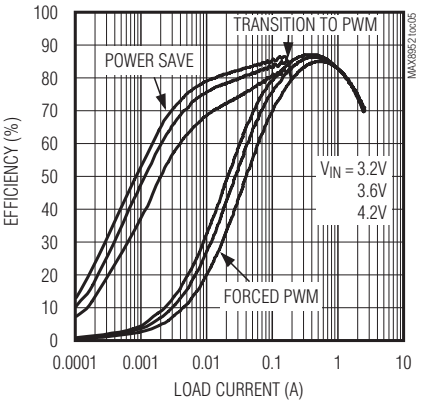
EFFICIENCY vs. LOAD CURRENT (1.4V OUTPUT, SYNC OFF)



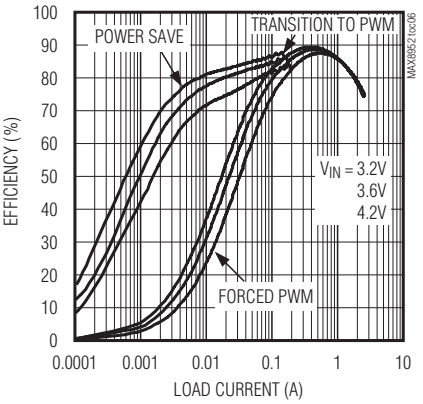
EFFICIENCY vs. LOAD CURRENT (1.0V OUTPUT, 26MHz SYNC)



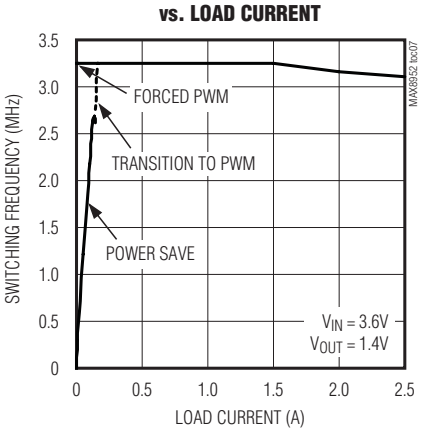
EFFICIENCY vs. LOAD CURRENT (1.1V OUTPUT, 26MHz SYNC)



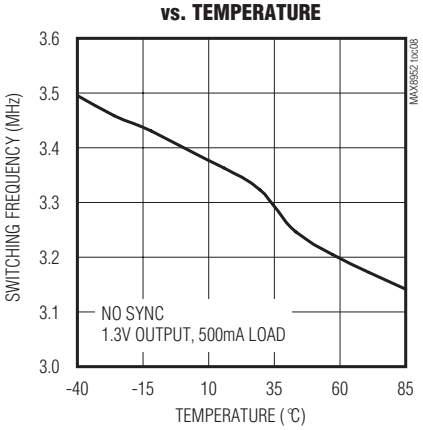
EFFICIENCY vs. LOAD CURRENT (1.4V OUTPUT, 26MHz SYNC)



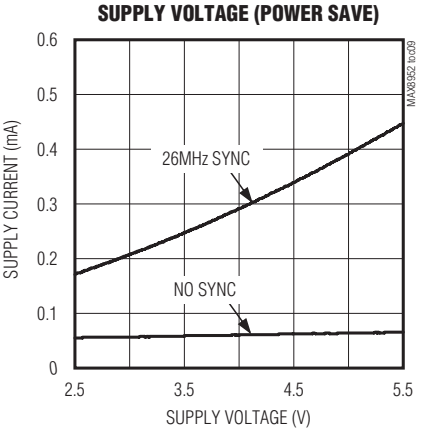
SWITCHING FREQUENCY vs. LOAD CURRENT



SWITCHING FREQUENCY vs. TEMPERATURE



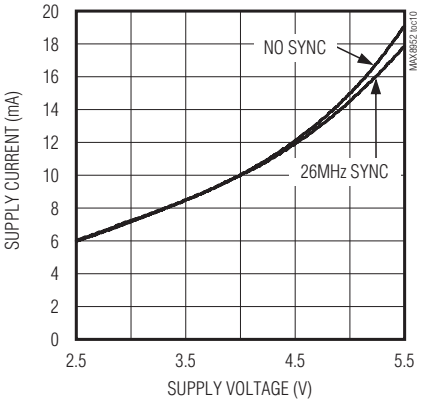
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE (POWER SAVE)



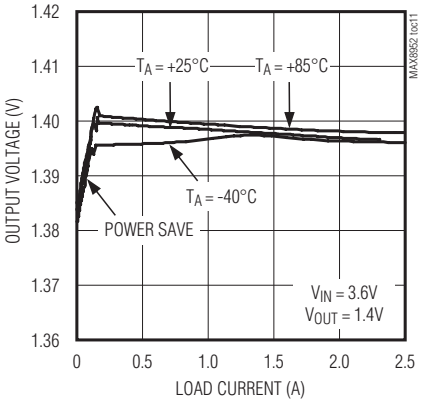
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, $V_{IN1} = V_{IN2} = 3.6V$, $V_{AGND} = V_{PGND} = 0V$, $V_{OUT} = 1.1V$, $V_{DD} = 1.8V$, $T_A = +25°C$, unless otherwise noted.)

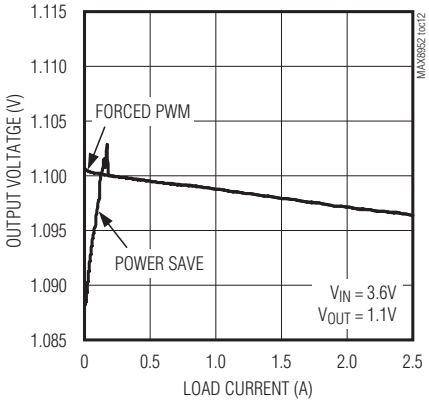
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE (FORCED PWM)



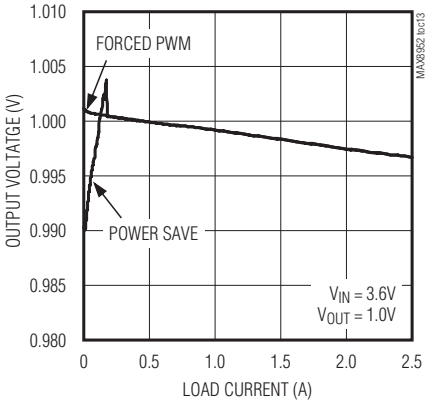
OUTPUT VOLTAGE vs. LOAD CURRENT



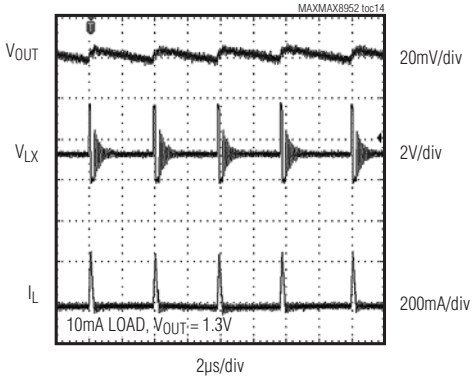
OUTPUT VOLTAGE vs. LOAD CURRENT



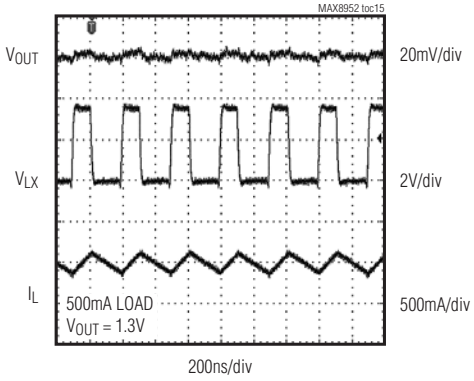
OUTPUT VOLTAGE vs. LOAD CURRENT



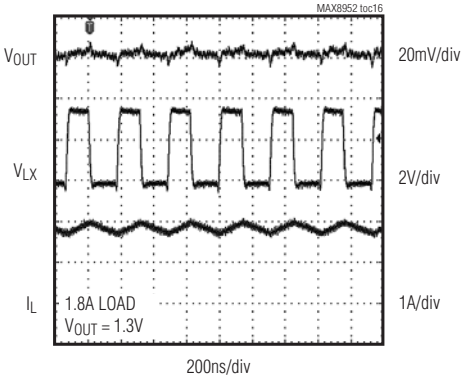
LIGHT LOAD SWITCHING WAVEFORMS



MEDIUM LOAD SWITCHING WAVEFORMS



HEAVY LOAD SWITCHING WAVEFORMS

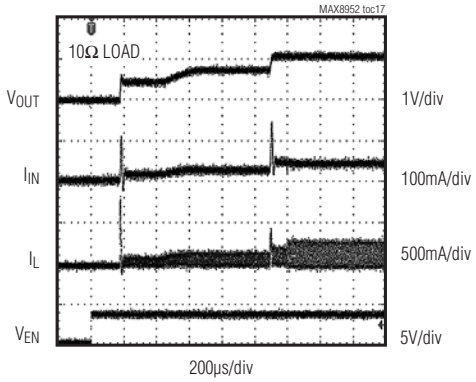


2.5A Step-Down Regulator with Remote Sense in 2mm x 2mm WLP

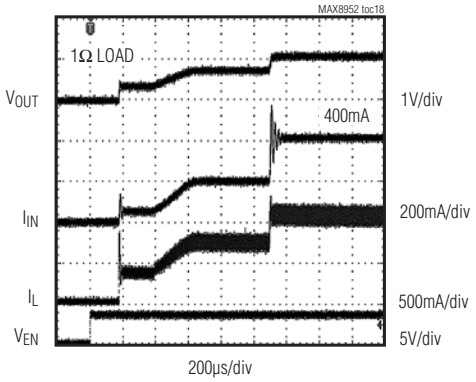
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, $V_{IN1} = V_{IN2} = 3.6V$, $V_{AGND} = V_{PGND} = 0V$, $V_{OUT} = 1.1V$, $V_{DD} = 1.8V$, $T_A = +25°C$, unless otherwise noted.)

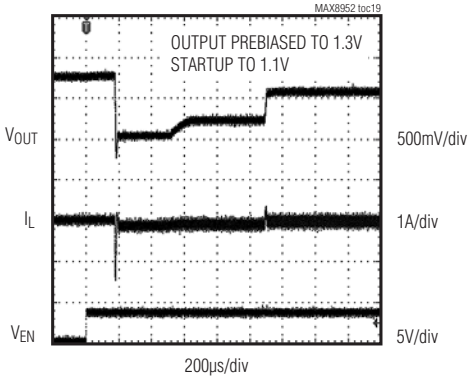
LIGHT LOAD STARTUP WAVEFORMS



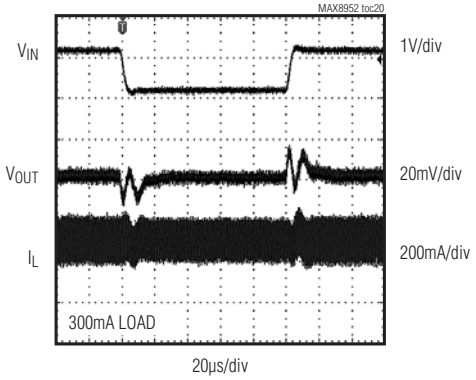
HEAVY LOAD STARTUP WAVEFORMS



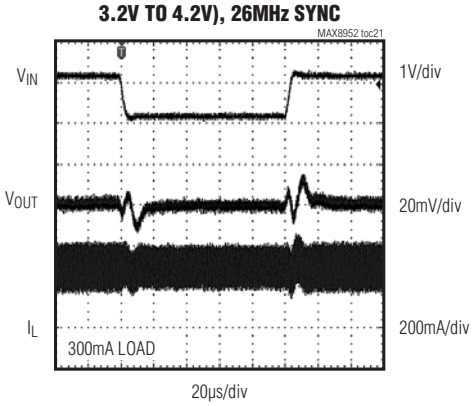
PREBIAS STARTUP WAVEFORMS (FORCED PWM)



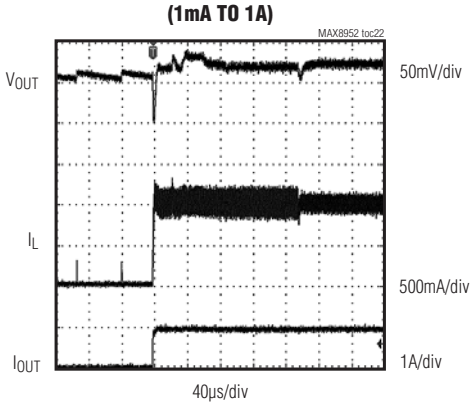
LINE TRANSIENT RESPONSE (4.2V TO 3.2V TO 4.2V), SYNC OFF



LINE TRANSIENT RESPONSE (4.2V TO 3.2V TO 4.2V), 26MHz SYNC



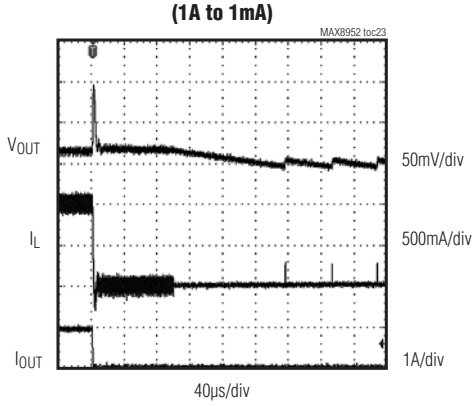
LOAD TRANSIENT RESPONSE (1mA TO 1A)



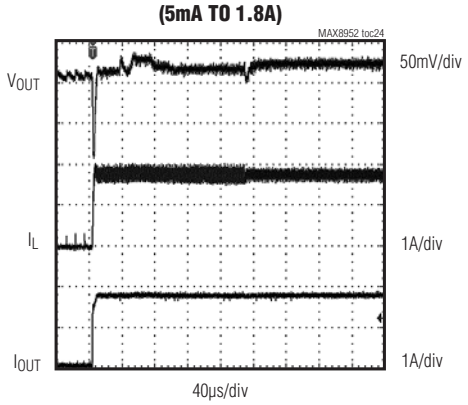
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, $V_{IN1} = V_{IN2} = 3.6V$, $V_{AGND} = V_{PGND} = 0V$, $V_{OUT} = 1.1V$, $V_{DD} = 1.8V$, $T_A = +25°C$, unless otherwise noted.)

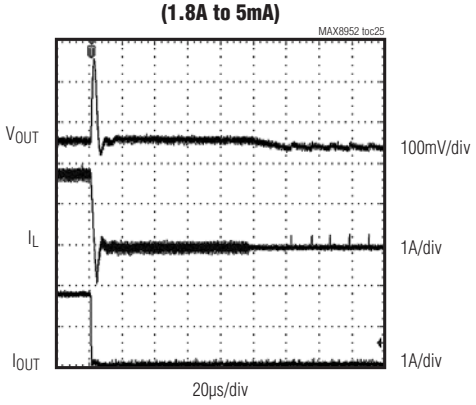
LOAD TRANSIENT RESPONSE (1A to 1mA)



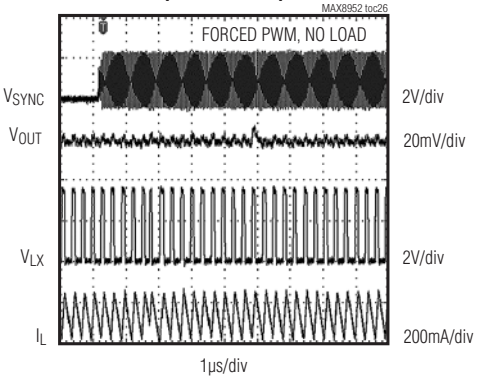
LOAD TRANSIENT RESPONSE (5mA TO 1.8A)



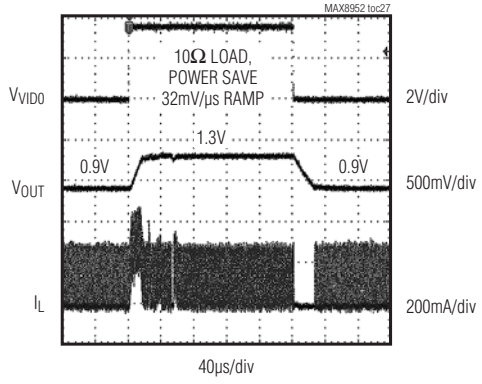
LOAD TRANSIENT RESPONSE (1.8A to 5mA)



SYNCHRONIZATION RESPONSE (26MHz SYNC)



OUTPUT VOLTAGE CHANGE RESPONSE



2.5A Step-Down Regulator with Remote Sense in 2mm x 2mm WLP

Bump Description

PIN	NAME	FUNCTION
A1	IN1	Analog Supply Voltage Input. The input voltage range is 2.5V to 5.5V. Install an 11Ω resistor between IN1 and the input supply. Bypass the IN1 to AGND with a 0.1µF ceramic capacitor as close as possible to the IC. Connect IN1 and IN2 to the same power source.
A2	AGND	Analog Ground. Connect AGND to the PCB ground plane.
A3	VID1	Voltage ID Control Input. The logic states of VID0 and VID1 select the register that sets the output voltage.
A4	IN2	Power-Supply Voltage Input. The input voltage range is from 2.5V to 5.5V. IN2 powers the internal p-channel and n-channel MOSFETs. Bypass IN2 to PGND with 2x 10µF and 0.1µF ceramic capacitor as close as possible to the IC. Connect IN1 and IN2 to the same power source.
B1	SNS+	Output Voltage Remote Sense, Positive Input. Connect SNS+ directly to the output at the load.
B2	EN	Logic Enable Input. Drive EN high to enable the DC-DC step-down regulator, or low to place in shutdown mode. In shutdown mode, this logic input has an internal pulldown resistor to AGND.
B3, B4	LX	Inductor Connection. LX is connected to the drains of the internal p-channel and n-channel MOSFETs. LX is high impedance during shutdown.
C1	SNS-	Output Voltage Sense, Negative Input. Connect to a quiet ground directly at the IC.
C2	VID0	Voltage ID Control Input. The logic states of VID0 and VID1 select the register that sets the output voltage.
C3, C4	PGND	Power Ground. Connect both PGND bumps to the PCB ground plane.
D1	V_{DD}	Logic Input Supply Voltage. Connect V_{DD} to the logic supply driving SDA, SCL, and SYNC. Bypass V_{DD} to AGND with a 0.1µF ceramic capacitor. When V_{DD} drops below the UVLO threshold, the I^2C registers are reset, but the EN control is still active in this mode.
D2	SDA	I^2C Data Input. Data is read on the rising edge of SCL and data is clocked out on the falling edge of SCL.
D3	SCL	I^2C Clock Input
D4	SYNC	External Clock Synchronization Input. Connect SYNC to a 13MHz, 19.2MHz, or 26MHz system clock. The DC-DC regulator can be forced to synchronize to this external clock depending on I^2C setting. See Table 8. SYNC does not have an internal pulldown. Connect SYNC to AGND if not used.

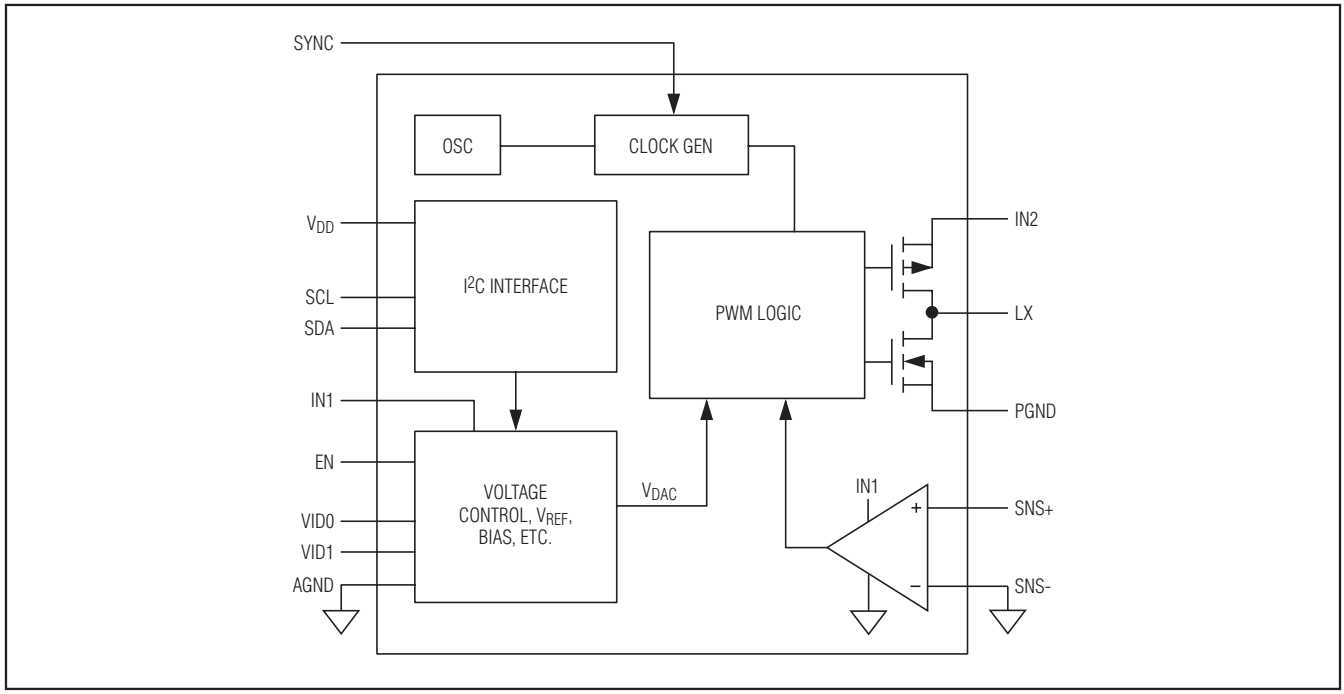


Figure 1. Block Diagram

Detailed Description

The MAX8952 high-efficiency, 3.25MHz step-down switching regulator delivers up to 2.5A of output current. The device operates from a 2.5V to 5.5V input voltage range, and the output voltage is I²C programmable from 0.77V to 1.40V in 10mV increments. Remote sense ensures precise DC regulation at the load. Total output error is less than ±1.5% over load, line, and temperature.

Dynamic Voltage Scaling

The output voltage is dynamically adjusted by use of the VID0 and VID1 logic inputs, allowing selection between four predefined operation modes/voltage configurations.

For each of the different output modes, the following parameters are programmable:

- Output voltage from 0.77V to 1.40V in 10mV steps
- Mode of operation: Forced PWM or power save
- Enable/disable of synchronization of switching frequency to external clock source

The relation between the VID0/VID1 and operation mode is given by Table 1.

The VID_ inputs have internal pulldown resistors. These pulldown resistors can be disabled through the CONTROL register after the IC is enabled, achieving lowest possible quiescent current. When EN is low, the CONTROL register is reset to default, enabling the pulldown resistors.

Table 1. VID0 and VID1 Configuration

VID1	VID0	MODE	I²C REGISTER	DEFAULT SWITCHING MODE	DEFAULT SYNCHRONIZATION	DEFAULT OUTPUT VOLTAGE (V)
0	0	MODE0	Table 3	POWER SAVE	OFF	1.40
0	1	MODE1	Table 4	POWER SAVE	OFF	1.00
1	0	MODE2	Table 5	POWER SAVE	OFF	1.40
1	1	MODE3	Table 6	POWER SAVE	OFF	1.10

2.5A Step-Down Regulator with Remote Sense in 2mm x 2mm WLP

Enable

The MAX8952 DC-DC step-down regulator is enabled/disabled using the EN logic input. The EN input is able to handle input voltages up to V_{IN1}, ensuring that the EN logic input can be controlled by a wide variety of signals/supplies.

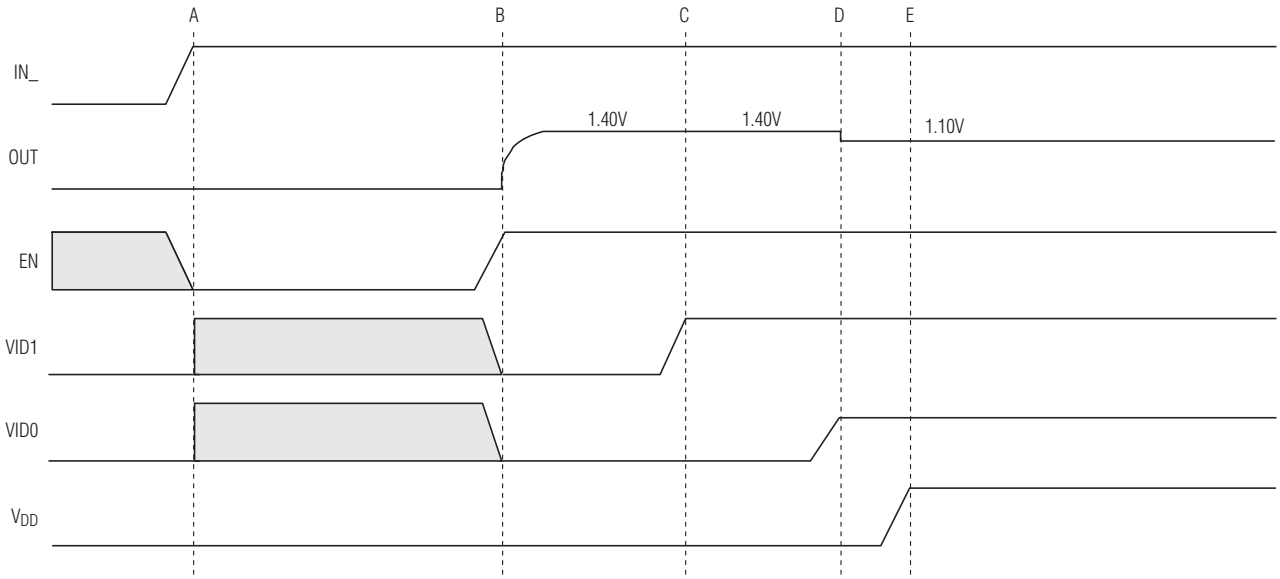
The EN input has an internal pulldown resistor that ensures EN is discharged during off conditions. This pulldown resistor can be disabled through the CONTROL register (see Table 7) once the IC is enabled, achieving lowest possible quiescent current. When EN is low, the CONTROL register is reset to default, enabling the pulldown resistors on EN, VID0, and VID1. See Figures 2 and 3 for detailed information on power-up and power-down sequencing and operation mode changes.

DC-DC Regulator Operating Modes

The IC operates in one of four modes determined by the state of the VID_ inputs (see Table 1). At power-up, the IC is set to operate in power-save operation for MODE0 through MODE3. For each of the operation modes, the DC-DC step-down regulator can be set to operate in either power-save mode or forced-PWM mode. This is done by writing to the MODE_ registers (see Table 3 to Table 6). The mode of operation can be changed at any time.

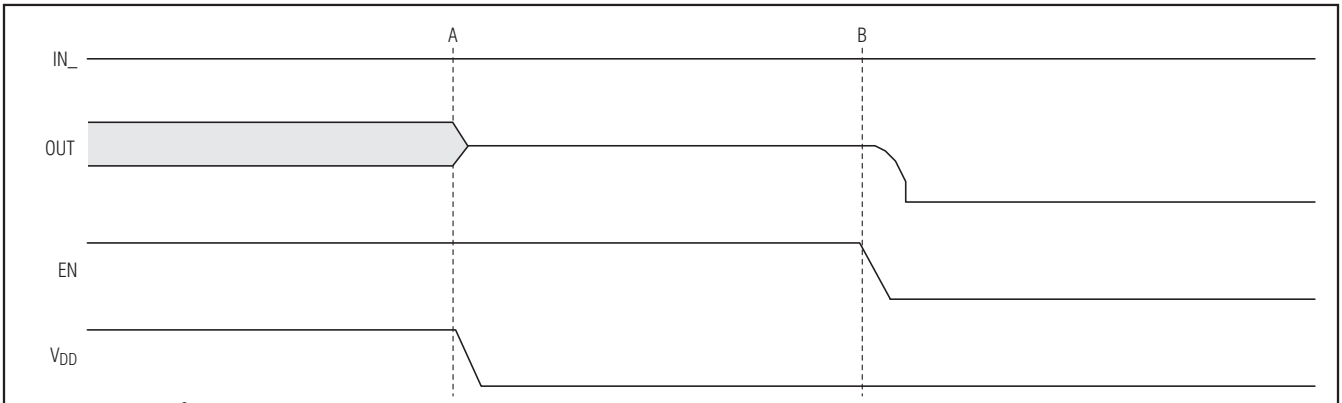
In power-save mode, the MAX8952 PWM switching frequency depends on the load current. For medium to high load condition, the IC operates in fixed-frequency PWM mode. For light load conditions, the IC operates in hysteretic mode. The proprietary hysteretic PWM control scheme ensures high efficiency, fast switching, and fast transient response. This control scheme is simple: when the output voltage is below the regulation threshold, the error comparator begins a switching cycle by turning on the high-side switch. This switch remains on until the minimum on-time expires and the output voltage is above the regulation threshold plus hysteresis or the inductor current is above the current-limit threshold. Once off, the high-side switch remains off until the minimum off-time expires and the output voltage falls again below the regulation threshold. During the off period, the low-side synchronous rectifier turns on and remains on until either the high-side switch turns on again or the inductor current approaches zero. The internal synchronous rectifier eliminates the need for an external Schottky diode.

The transition between PWM and hysteretic operation is based on the number of consecutive zero-crossing cycles. When more than 16 consecutive zero-crossing cycles are detected, the DC-DC step-down converter enables the bias for hysteretic operation. Once correct-



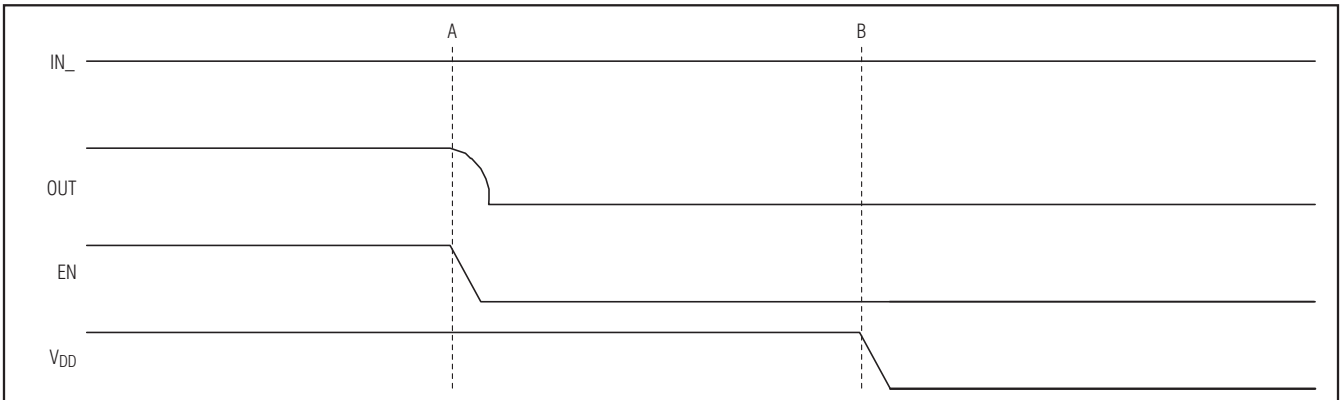
A: POWER CONNECTED TO IN1 AND IN2.
B: EN LOGIC INPUT PULLED HIGH, OUTPUT VOLTAGE IS SET TO CONDITION DEFINED BY THE DEFAULT VALUE OF THE I^2C REGISTER FOR MODE0 (SEE TABLE 1).
C: OUTPUT VOLTAGE IS SET TO CONDITION DEFINED BY THE DEFAULT VALUE OF THE I^2C REGISTER FOR MODE2.
D: OUTPUT VOLTAGE IS SET TO CONDITION DEFINED BY THE DEFAULT VALUE OF THE I^2C REGISTER FOR MODE3.
E: V_{DD} PULLED HIGH, ENABLING I^2C INTERFACE.

Figure 2. Power-Up Sequence



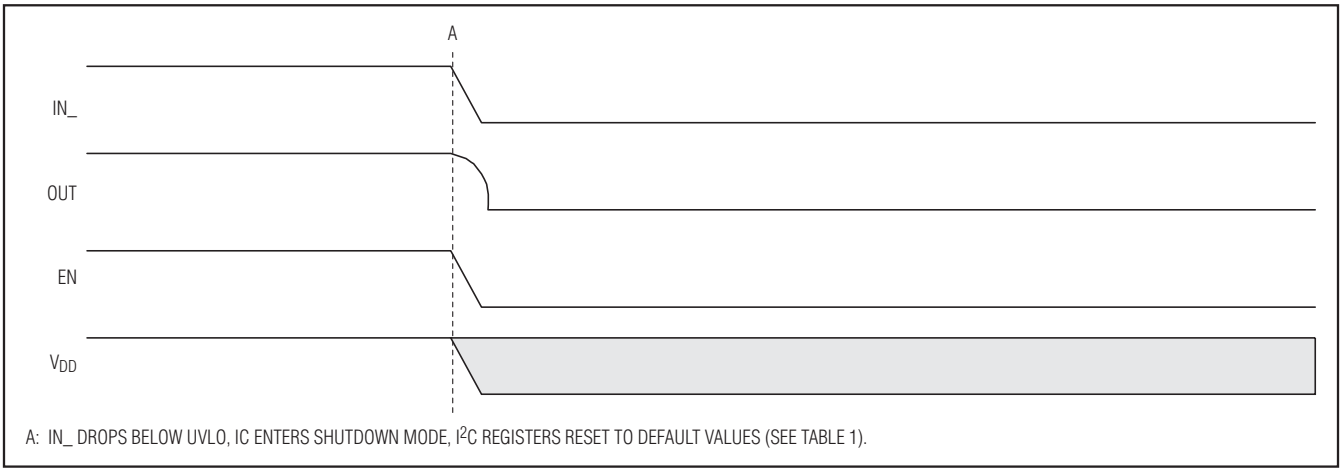
A: V_{DD} PULLED LOW, I^2C REGISTERS RESET TO DEFAULT VALUES (SEE TABLE 1) AND THE OUTPUT VOLTAGE CHANGES TO THE DEFAULT VALUE.
B: EN LOGIC INPUT PULLED LOW, STEP-DOWN REGULATOR ENTERS SHUTDOWN MODE.

Figure 3a. Shutdown by Pulling V_{DD} Low Before EN



A: EN LOGIC INPUT PULLED LOW, STEP-DOWN REGULATOR ENTERS I^2C READY MODE, OUTPUT DISABLED.
B: V_{DD} PULLED LOW, I^2C REGISTERS RESET TO DEFAULT VALUES (SEE TABLE 1).

Figure 3b. Shutdown by Pulling EN Low Before V_{DD}



A: IN_ DROPS BELOW UVLO, IC ENTERS SHUTDOWN MODE, I^2C REGISTERS RESET TO DEFAULT VALUES (SEE TABLE 1).

Figure 3c. Shutdown Due to IN1 Undervoltage Lockout

2.5A Step-Down Regulator with Remote Sense in 2mm x 2mm WLP

ly biased and the number of consecutive zero-crossing cycles exceeds 24, the DC-DC step-down converter begins hysteretic operation.

During hysteretic operation, there is a silent DC offset due to the use of valley regulation. See Figure 4.

When operating in power-save mode and the load current is increased so that the number of consecutive zero-crossing cycles is less than 16, the PWM mode is biased. Once fully biased and the number of zero-crossing cycles drops below 8, the DC-DC converter then begins PWM operation. Since there is a delay between the increase in load current and the DC-DC converter starting PWM, the converter supports full current on the output during hysteretic operation. See Figure 5 for a detailed state diagram.

Power-save operation offers improved efficiency at light loads by changing to hysteretic mode, reducing the switching frequency depending on the load condition. With moderate to heavy loading, the regulator switches at a fixed switching frequency as it does in forced-PWM mode. In power-save mode, the transition from hysteretic mode to fixed-frequency switching occurs at the load current specified in the following equation:

$$I_{OUT} = \frac{V_{IN} - V_{OUT}}{2 \times L} \times \frac{V_{OUT}}{V_{IN} \times f_{OSC}}$$

In forced-PWM mode, the regulator operates with a constant (3.25MHz or synchronized to external clock source) switching frequency regardless of output load.

Forced-PWM mode is ideal for low-noise systems because switching harmonics occur at multiples of the constant switching frequency and are easily filtered. However, light-load power consumption in forced-PWM mode is higher than that of power-save mode.

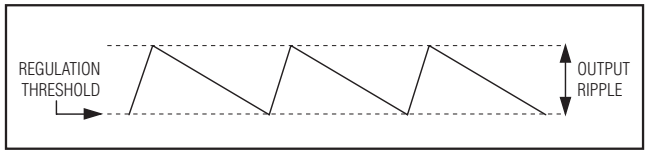


Figure 4. Output Regulation in Hysteretic Operation

Soft-Start

The IC includes internal soft-start circuitry that eliminates inrush current at startup, reducing transients on the input source (see the *Typical Operating Charac-*

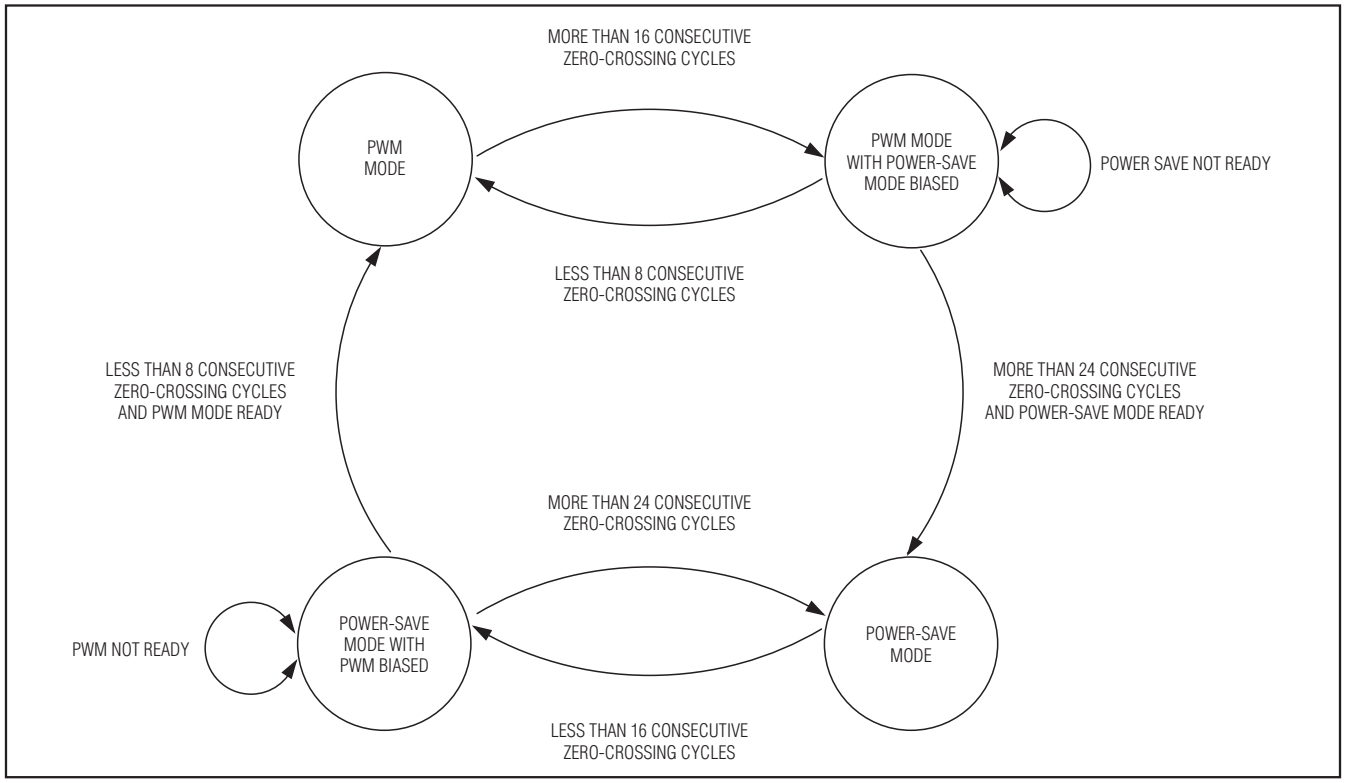


Figure 5. Mode Change for DC-DC Step-Down Converter

teristics). Soft-start is particularly useful for high-impedance input sources, such as Li+ and alkaline cells. When enabling the IC into a prebiased output, the IC performs a complete soft-start cycle.

Synchronous Rectification

An internal n-channel synchronous rectifier eliminates the need for an external Schottky diode and improves efficiency. The synchronous rectifier turns on during the second half of each switching cycle (off-time). During this time, the voltage across the inductor is reversed, and the inductor current ramps down. In PWM mode, the synchronous rectifier turns off at the end of the switching cycle. In power-save mode, the synchronous rectifier turns off when the inductor current falls below 50mA (typ) or at the end of the switching cycle, whichever occurs first.

Ramp-Rate Control

The MAX8952 output voltage has an actively controlled variable ramp rate, set with the I²C interface (see Figures 6, 7, and 8). The value set in the RAMP register controls the output voltage ramp rate. The RAMP_DOWN bit controls the active ramp-down behavior in power-save mode. When the regulator is set for power-save mode and the RAMP_DOWN bit is cleared, the ramp-down is not actively controlled, and the regulator output voltage ramps down at the rate determined by the output capacitance and the external load. Small loads result in an output-voltage decay that is slower than that specified by RAMP; large loads result in an output-voltage decay that is no faster than that specified by RAMP When the RAMP_DOWN bit is set in power-save mode, the zero-cross comparator is disabled during the ramp-down condition. Active ramp-down functionality is inherent in forced-PWM operation.

Calculate the maximum and minimum values for the ramp rate as follows:

$$t_{RAMP\_MIN} = \frac{V_{OUT\_LSB}}{t_{CLK\_MAX}} \times \frac{1}{2^{RAMP\_CODE}}$$

$$t_{RAMP\_MAX} = \frac{V_{OUT\_LSB}}{t_{CLK\_MIN}} \times \frac{1}{2^{RAMP\_CODE}}$$

where:

$$V_{OUT\_LSB} = 10mV$$

$$t_{CLK\_MAX} = \frac{1}{f_{SW\_MIN}}$$

$$t_{CLK\_MIN} = \frac{1}{f_{SW\_MAX}}$$

f_{SW} = 3.25MHz ±10% for PWM operation

f_{SW} = 3.25MHz ±25% for hysteretic operation

$$f_{SW} = \frac{f_{SYNC}}{n}$$

f_{SYNC} = frequency of external clock

n = 4 for 13MHz, 6 for 19.2MHz, and 8 for 26MHz

RAMP_CODE = value of the RAMP[2:0] register (see Table 9)

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the IC. When internal thermal sensors detect a

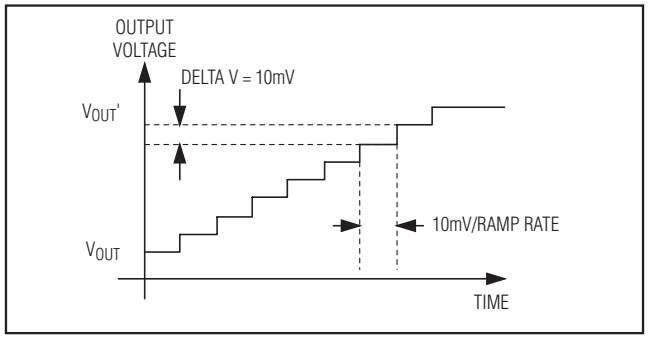


Figure 6. Ramp-Up Function

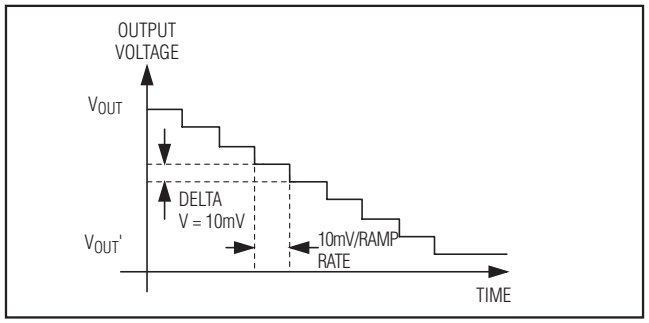


Figure 7. Ramp-Down Function

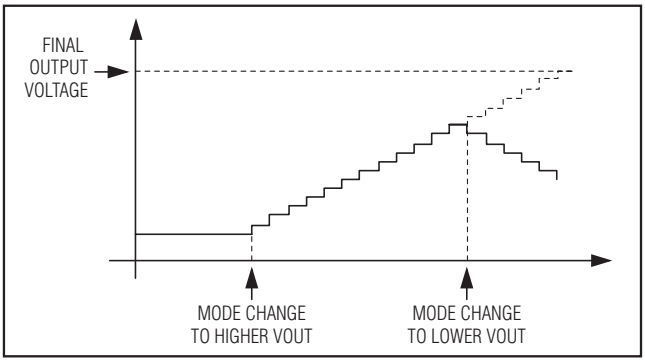


Figure 8. Mode Change Before Final Value is Reached

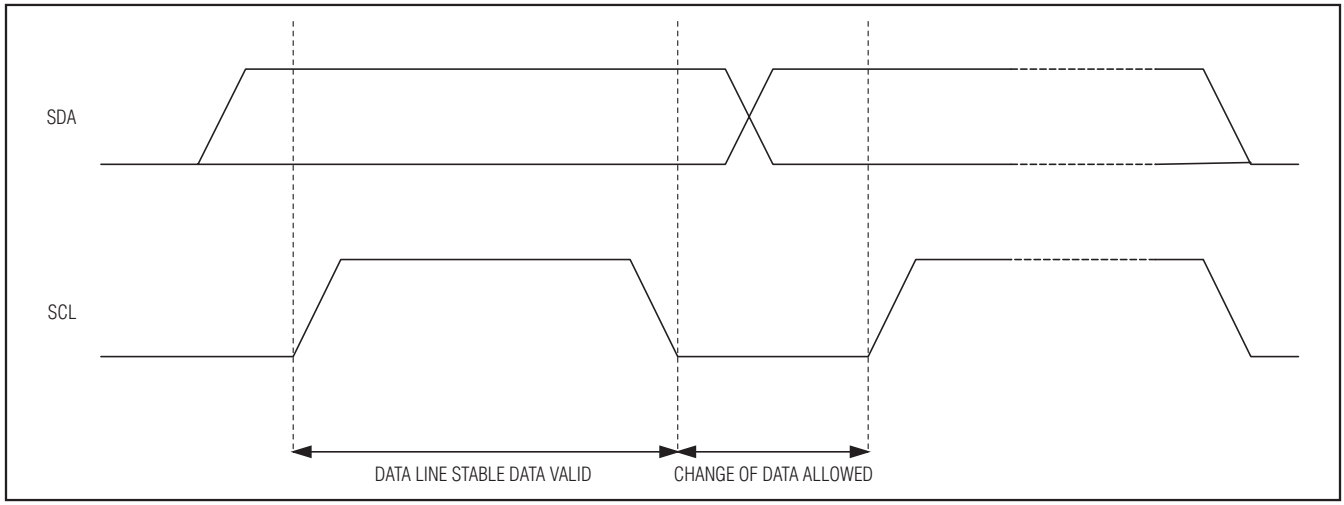


Figure 9. I²C Bit Transfer

die temperature in excess of +160°C (typ), the DC-DC step-down regulator is shut down, allowing the IC to cool. The DC-DC step-down regulator is turned on again after the junction cools by 20°C (typ), resulting in a pulsed output during continuous thermal-overload conditions.

During thermal overload, the I²C interface remains active and all register values are maintained.

I²C Interface

An I²C-compatible, 2-wire serial interface controls the step-down converter output voltage, ramp rate, operating mode, and synchronization. The serial bus consists of a bidirectional serial-data line (SDA) and a serial-clock input (SCL). The master initiates data transfer on the bus and generates SCL to permit data transfer.

I²C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus signals.

Bit Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse (see Figure 9). Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section for more information).

Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is 9 bits long; 8 bits of data followed by the acknowledge bit. The IC supports data transfer rates with SCL frequencies up to 400kHz.

START and STOP Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high (Figure 10).

A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission by issuing a not acknowledge followed by

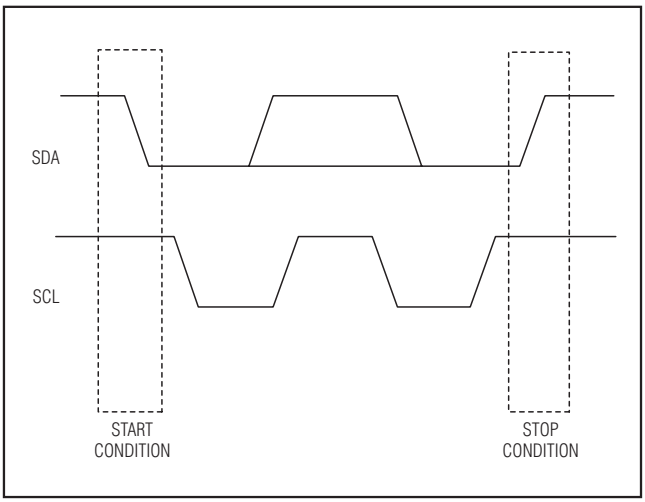


Figure 10. I²C START and STOP Conditions

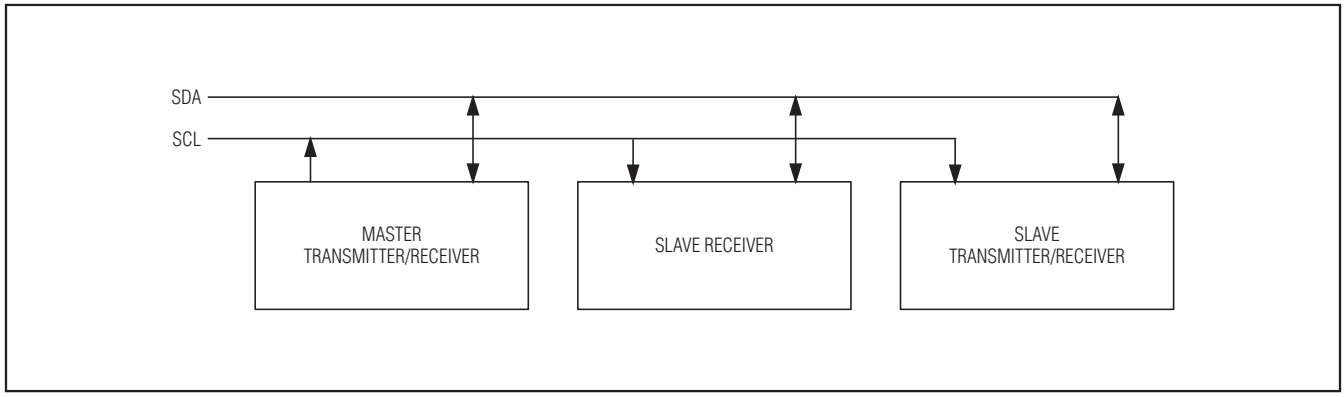


Figure 11. I²C Master/Slave Configuration

a STOP condition (see the *Acknowledge* section for more information). The STOP condition frees the bus. To issue a series of commands to the slave, the master can issue REPEATED START (Sr) commands instead of a STOP command to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the IC internally disconnects SCL from the serial interface until the next START condition, minimizing digital noise and feedthrough.

System Configuration

A device on the I²C bus that generates a message is called a transmitter and a device that receives the message is a receiver. The device that controls the message is the master and the devices that are controlled by the master are called slaves. See Figure 11.

Acknowledge

The number of data bytes between the START and STOP conditions for the transmitter and receiver are unlimited. Each 8-bit byte is followed by an acknowledge bit. The acknowledge bit is a low-level signal put on SDA by the receiver during which time the master generates an extra acknowledge-related clock pulse. A slave receiver that is addressed must generate an acknowledge after each byte it receives. Also, a master receiver must generate an acknowledge after each byte it receives that has been clocked out of the slave transmitter. See Figure 12.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge clock pulse (setup and hold times must also be met). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave SDA high to enable the master to generate a STOP condition.

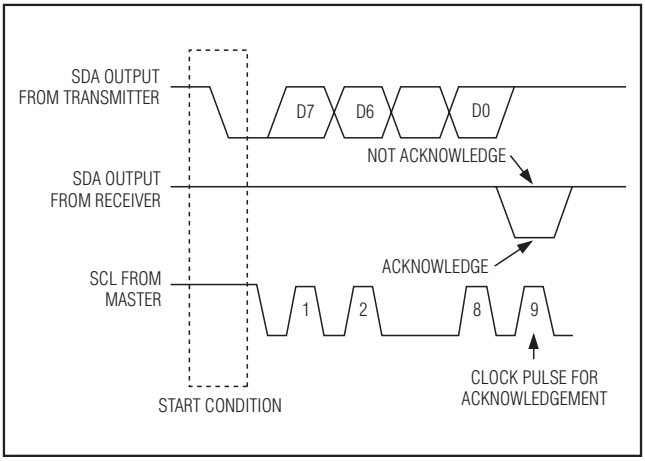


Figure 12. I²C Acknowledge

Register Reset

The I²C resisters reset back to their default values when the voltage at either IN1 or V_{DD} drops below the corresponding UVLO threshold (see the *Electrical Characteristics* table).

Update of Output Operation Mode

If updating the output voltage or Operation Mode register for the mode that the IC is currently operating in, the

2.5A Step-Down Regulator with Remote Sense in 2mm x 2mm WLP

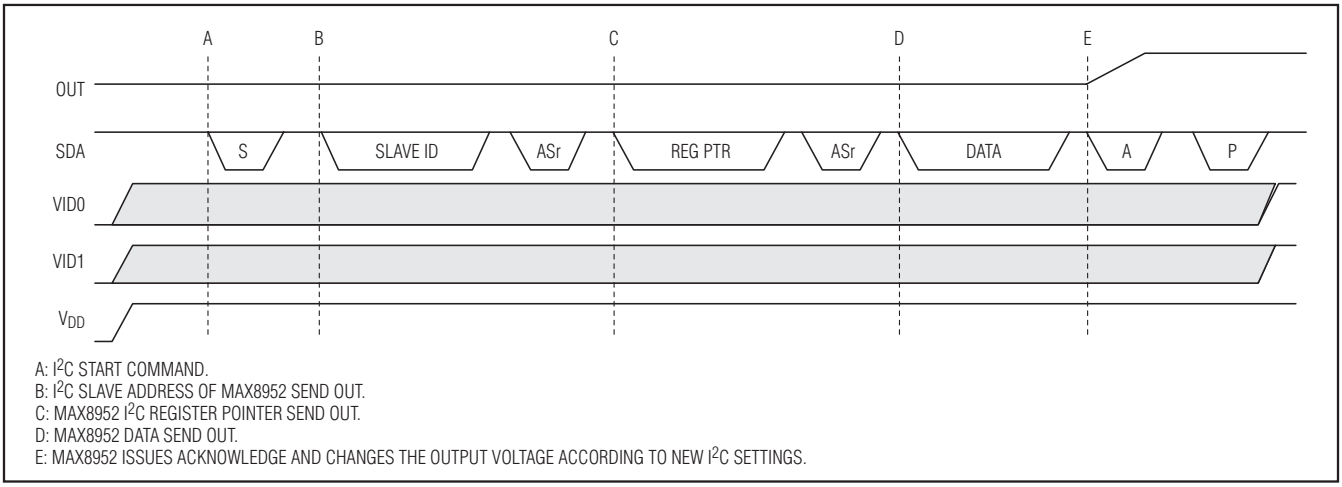


Figure 13. Update Output Operation

output voltage/operation mode is updated at the same time the IC sends the acknowledge for the I²C data byte (see Figure 13).

Slave Address

A bus master initiates communication with a slave device (MAX8952) by issuing a START condition followed by the slave address. The slave address byte consists of 7 address bits (1100 000x) and a read/write bit (R/$\overline{W}$). After receiving the proper address, the IC issues an acknowledge by pulling SDA low during the ninth clock cycle.

Other slave addresses can be assigned. Contact the factory for details.

Write Operations

The IC recognizes the write byte protocol as defined in the SMBus™ specification and shown in Figures 14a and 14b. The write byte protocol allows the I²C master device to send 1 byte of data to the slave device. The write byte protocol requires a register pointer address for the subsequent write. The IC acknowledges any register pointer even though only a subset of those registers actually exists in the device. The write byte protocol is as follows:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte.
8) The slave updates with the new data.
9) The master sends a STOP condition.

In addition to the write-byte protocol, the IC can write to multiple registers as shown in Figure 14b. This protocol allows the I²C master device to address the slave only once and then send data to a sequential block of registers starting at the specified register pointer.

Use the following procedure to write to a sequential block of registers:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends the 8-bit register pointer of the first register to write.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte.
8) The slave updates with the new data.
9) Steps 6 to 8 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
10) The master sends a STOP condition.

Read Operations

The method for reading a single register (byte) is shown in Figure 15a. To read a single register:

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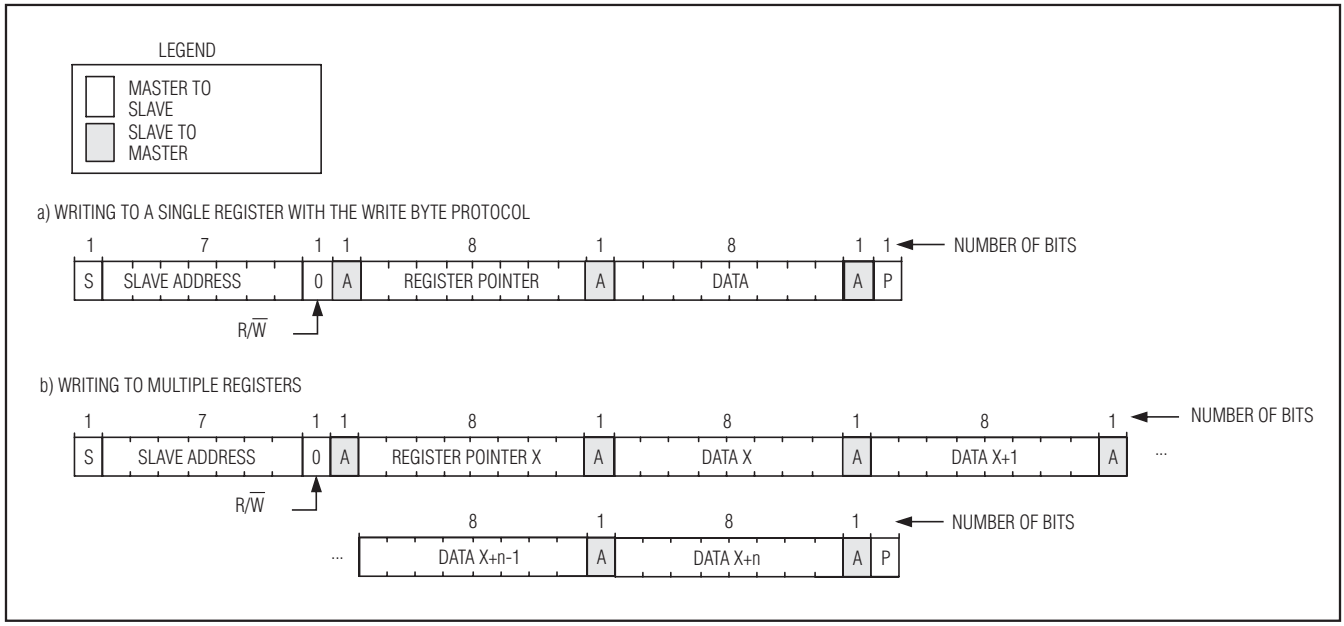


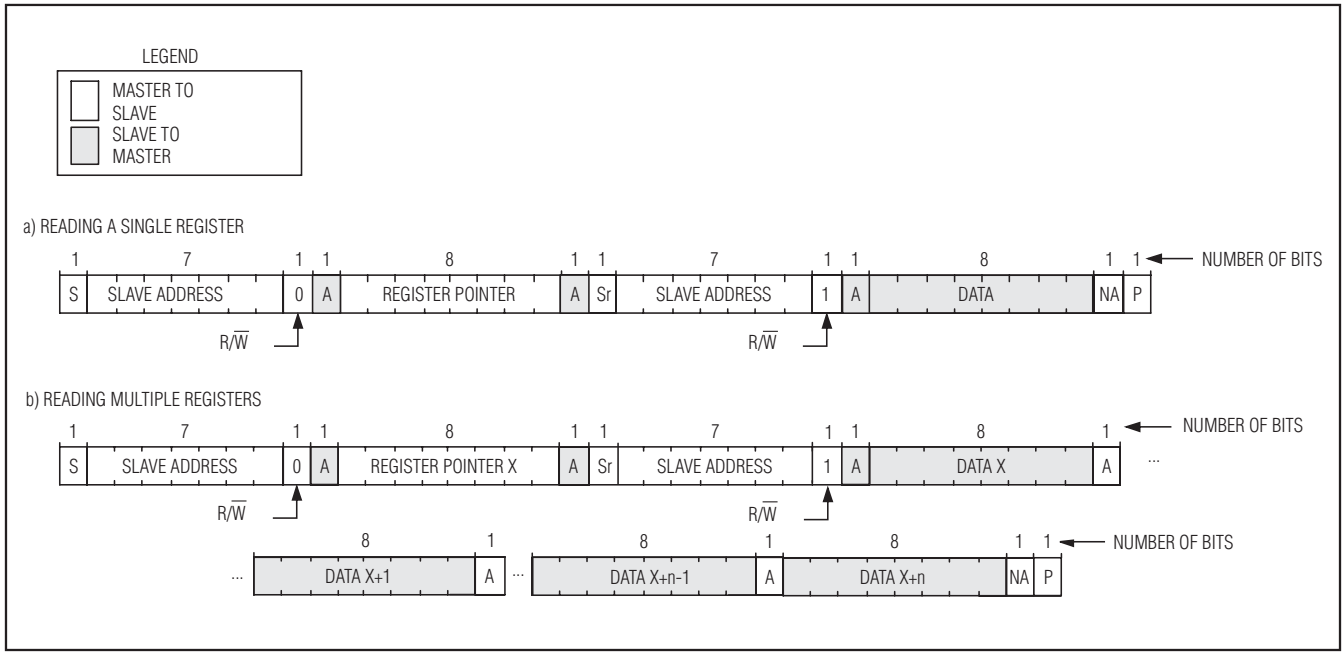
Figures 14a and 14b. Writing to the IC

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START condition.
7) The master sends the 7-bit slave address followed by a read bit.
8) The slave asserts an acknowledge by pulling SDA low.
9) The slave sends the 8-bit data (contents of the register).
10) The master asserts a not acknowledge by keeping SDA high.
11) The master sends a STOP condition.

In addition, the IC can read a block of multiple sequential registers as shown in Figure 15b. Use the following procedure to read a sequential block of registers:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer of the first register in the block.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START condition.
7) The master sends the 7-bit slave address followed by a read bit.
8) The slave asserts an acknowledge by pulling SDA low.
9) The slave sends the 8-bit data (contents of the register).
10) The master asserts an acknowledge by pulling SDA low when there is more data to read, or a not acknowledge by keeping SDA high when all data has been read.
11) Steps 9 and 10 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
12) The master sends a STOP condition.

2.5A Step-Down Regulator with Remote Sense in 2mm x 2mm WLP



Figures 15a and 15b. Reading from the IC

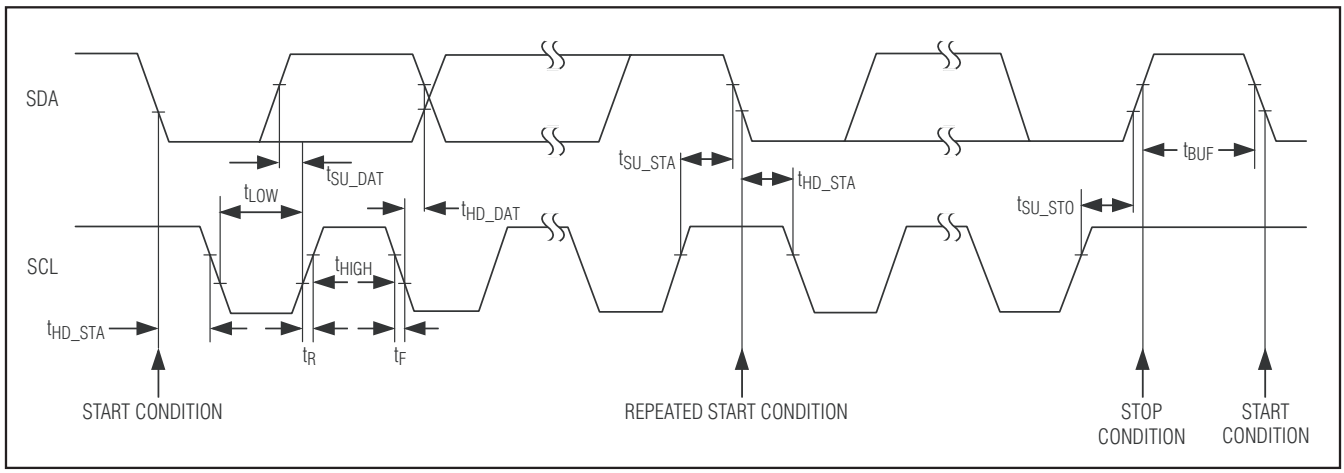


Figure 16. I²C Timing Diagram

Table 2. I²C Register Map

POINTER	REGISTER	POR	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x00	MODE0	0x3F	OPER MODE	SYNC MODE	VOUT MODE0[5:0]					
0x01	MODE1	0x17	OPER MODE	SYNC MODE	VOUT MODE1[5:0]					
0x02	MODE2	0x3F	OPER MODE	SYNC MODE	VOUT MODE2[5:0]					
0x03	MODE3	0x21	OPER MODE	SYNC MODE	VOUT MODE3[5:0]					
0x04	CONTROL	0xE0	EN_PD	VID0_PD	VID1_PD	—	—	—	—	—
0x05	SYNC	0x00	SYNC[1:0]		—	—	—	—	—	—
0x06	RAMP	0x01	RAMP[2:0]			FORCE_HYS	FORCE_OSC	—	RAMP_DOWN	—
0x08	CHIP_ID1	0x20	DIE TYPE[7:4]				DIE TYPE[3:0]			
0x09	CHIP_ID2	0x1A	DASH[3:0]				MASK REV[3:0]			

Table 3. I²C Register: MODE0

This register contains output voltage and operation mode control for MODE0, VID0 = GND, VID1 = GND.

REGISTER NAME	MODE0
Address	0x00h
Reset Value	0x3Fh
Type	Read/write
Special Features	Reset upon V_{DD} or IN_ UVLO

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	FPWM_EN0	**DC-DC Step-Down Converter Operation Mode for MODE0** 0 = DC-DC converter automatically changes between hysteretic mode for light load conditions and PWM mode for medium to heavy load conditions. 1 = DC-DC converter operates in forced-PWM mode.	0
B6	SYNC_MODE0	**Disable/Enable Synchronization to External Clock** 0 = DC-DC converter ignores the external SYNC input regardless of operation mode. 1 = DC-DC converter synchronizes to external SYNC input when available.	0
B5	OUT_ MODE0[5:0]	**Output Voltage Selection for MODE0** 000000 = 0.77V 000001 = 0.78V 110011 = 1.28V 110100 = 1.29V 110101 = 1.30V 111110 = 1.39V 111111 = 1.40V	111111 (1.4V)
B4			
B3			
B2			
B1			
B0 (LSB)			

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Table 4. I²C Register: MODE1

This register contains output voltage and operation mode control for MODE1, VID1 = GND, VID0 = V_{DD}.

REGISTER NAME	MODE1
Address	0x01h
Reset Value	0x17h
Type	Read/write
Special Features	Reset upon V_{DD} or IN_ UVLO

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	FPWM_EN1	**DC-DC Step-Down Converter Operation Mode for MODE1** 0 = DC-DC converter automatically changes between hysteretic mode for light load conditions and PWM mode for medium to heavy load conditions. 1 = DC-DC converter operates in forced-PWM mode.	0
B6	SYNC_MODE1	**Disable/Enable Synchronization to External Clock** 0 = DC-DC converter ignores the external SYNC input regardless of operation mode. 1 = DC-DC converter synchronizes to external SYNC input when available.	0
B5	OUT_MODE1[5:0]	**Output Voltage Selection for MODE1** 000000 = 0.77V 000001 = 0.78V 010110 = 0.99V 010111 = 1.00V 011000 = 1.01V 111110 = 1.39V 111111 = 1.40V	010111 (1.00V)
B4			
B3			
B2			
B1			
B0 (LSB)			

Table 5. I²C Register: MODE2

This register contains output voltage and operation mode control for MODE2, VID1 = V_{DD}, VID0 = GND.

REGISTER NAME	MODE2
Address	0x02h
Reset Value	0x3Fh
Type	Read/write
Special Features	Reset upon V_{DD} or IN_ UVLO

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	FPWM_EN2	**DC-DC Step-Down Converter Operation Mode for MODE2** 0 = DC-DC converter automatically changes between hysteretic mode for light load conditions and PWM mode for medium to heavy load conditions. 1 = DC-DC converter operates in forced-PWM mode.	0
B6	SYNC_MODE2	**Disable/Enable Synchronization to External Clock** 0 = DC-DC converter ignores the external SYNC input regardless of operation mode. 1 = DC-DC converter synchronizes to external SYNC input when available.	0
B5	OUT_MODE2[5:0]	**Output Voltage Selection for MODE2** 000000 = 0.77V 000001 = 0.78V 110011 = 1.28V 110100 = 1.29V 110101 = 1.30V 111110 = 1.39V 111111 = 1.40V	111111 (1.4V)
B4			
B3			
B2			
B1			
B0 (LSB)			

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Table 6. I²C Register: MODE3

This register contains output voltage and operation mode control for MODE3, VID1 = V_{DD}, VID0 = V_{DD}.

REGISTER NAME	MODE3
Address	0x03h
Reset Value	0x21h
Type	Read/write
Special Features	Reset upon V_{DD} or IN_ UVLO

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	FPWM_EN3	**DC-DC Step-Down Converter Operation Mode for MODE3** 0 = DC-DC converter automatically changes between hysteretic mode for light load conditions and PWM mode for medium to heavy load conditions. 1 = DC-DC converter operates in forced-PWM mode.	0
B6	SYNC_MODE3	**Disable/Enable Synchronization to External Clock** 0 = DC-DC converter ignores the external SYNC input regardless of operation mode. 1 = DC-DC converter synchronizes to external SYNC input when available.	0
B5	OUT_MODE3[5:0]	**Output Voltage Selection for MODE3** 000000 = 0.77V 000001 = 0.78V 100000 = 1.09V 100001 = 1.10V 100010 = 1.11V 111110 = 1.39V 111111 = 1.40V	100001
B4			
B3			
B2			
B1			
B0 (LSB)			

Table 7. I²C Register: CONTROL

This register enables or disables pulldown resistors.

REGISTER NAME	CONTROL
Address	0x04h
Reset Value	0xE0h
Type	Read/write
Special Features	Reset upon V_{DD}, IN_ UVLO or EN pulled low

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	EN_PD	0 = Pulldown on EN input is disabled. 1 = Pulldown on EN input is enabled.	1
B6	VID0_PD	0 = Pulldown on VID0 input is disabled. 1 = Pulldown on VID0 input is enabled.	1
B5	VID1_PD	0 = Pulldown on VID1 input is disabled. 1 = Pulldown on VID1 input is enabled.	1
B4	—	Reserved for future use.	0
B3	—	Reserved for future use.	0
B2	—	Reserved for future use.	0
B1	—	Reserved for future use.	0
B0 (LSB)	—	Reserved for future use.	0

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Table 8. I²C Register: SYNC

This register specifies the clock frequency of external clock source.

REGISTER NAME	SYNC
Address	0x05h
Reset Value	0x00h
Type	Read
Special Features	Reset upon V_{DD} or IN_ UVLO

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	SYNC[1:0]	**Sets Clock Frequency of External Clock Present on SYNC Input** 00 = 26MHz 01 = 13MHz 10 = 19.2MHz 11 = 19.2MHz	00
B6			
B5	—	Reserved for future use.	0
B4	—	Reserved for future use.	0
B3	—	Reserved for future use.	0
B2	—	Reserved for future use.	0
B1	—	Reserved for future use.	0
B0 (LSB)	—	Reserved for future use.	0

Table 9. I²C Register: RAMP

This register controls of ramp-up/down function.

REGISTER NAME	RAMP
Address	0x06h
Reset Value	0x01h
Type	Read
Special Features	Reset upon V_{DD} or IN_ UVLO

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	RAMP[2:0]	**Control the RAMP Timing** 000 = 32mV/µs 001 = 16mV/µs 010 = 8mV/µs 011 = 4mV/µs 100 = 2mV/µs 101 = 1mV/µs 110 = 0.5mV/µs 111 = 0.25mV/µs	000
B6			
B5			
B4	FORCE_HYS	**Only Valid When Converter is Operating with FPWM_EN_ = 0** 0 = Automatically change between power-save mode and PWM mode, depending on load current. 1 = Converter always operates in power-save mode regardless of load current as long as FPWM_EN_ = 0. If FPWM_EN_ = 1, this setting is ignored.	0
B3	FORCE_OSC	**Force Oscillator While Running in Hysteretic Mode** 0 = Internal oscillator is disabled in power save when operating in hysteretic mode. 1 = Internal oscillator is enabled in power save even when operating in hysteretic mode.	0
B2	—	Reserved for future use.	0
B1	RAMP_DOWN	**Active Ramp-Down Control for Power-Save Mode** 0 = Active ramp disabled for power-save mode. 1 = During ramp-down, the error crossing detector is disabled allowing negative current to flow through the nMOS device.	0
B0 (LSB)	—	Reserved for future use.	0

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Table 10. I²C Register: CHIP_ID1

This register contains the die type number (20).

REGISTER NAME	CHIP_ID1
Address	0x08h
Reset Value	0x20h
Type	Read
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	DIE_TYPE[7:4]	BCD character (2)	0010
B6			
B5			
B4			
B3	DIE_TYPE[3:0]	BCD character (0)	0000
B2			
B1			
B0 (LSB)			

Table 11. I²C Register: CHIP_ID2

This register contains the die type dash number and mask revision level.

REGISTER NAME	CHIP_ID2
Address	0x09h
Reset Value	0x1Ah
Type	Read
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	DASH[7:4]	BCD character 1 (1)	0001
B6			
B5			
B4			
B3	MASK_REV[3:0]	BCD character A (A)	1010
B2			
B1			
B0 (LSB)			

Applications Information

Inductor Selection

Calculate the inductor value (L_{IDEAL}) using the following formula:

$$L_{IDEAL} = \frac{4 \times V_{IN} \times D \times (1-D)}{I_{OUT(MAX)} \times f_{OSC}}$$

This sets the peak-to-peak inductor current ripple to 1/4 the maximum output current. The oscillator frequency, f_{OSC}, is 3.25MHz, and the duty cycle, D, is:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Given L_{IDEAL}, the peak-to-peak inductor ripple current is 0.25 x $I_{OUT(MAX)}$. The peak inductor current is 1.125 x $I_{OUT(MAX)}$. Make sure that the saturation current of the inductor exceeds the peak inductor current, and the rated maximum DC inductor current exceeds the maximum output current ($I_{OUT(MAX)}$). Inductance values smaller than L_{IDEAL} can be used to reduce inductor size; however, if much smaller values are used, peak inductor current rises and a larger output capacitance may be required to suppress output ripple. Larger inductance values than L_{IDEAL} can be used to obtain higher output current, but typically require a physically larger inductor size. See Table 12 for recommended inductors.

Table 12. Recommended Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	DC RESISTANCE (Ω typ)	CURRENT RATING (mA)	DIMENSIONS L x W x H (mm)
Toko	DE2815C	0.47 1.0	0.025 0.033	3800 2700	3.2 x 3.0 x 1.5
	DB3015C	1.0	0.036	2700	3.2 x 3.2 x 1.5
TDK	VLS252010ET	0.47	0.038	2800	2.5 x 2.0 x 1.0
	VLS4012ET	1.0	0.050	2800	4.0 x 4.0 x 1.2
Coilcraft	LPS5015	1.0	0.050	3900	5.0 x 5.0 x 1.5
	LPS5010	0.47	0.038	3400	5.0 x 5.0 x 1.0
	LPS4414	0.7	0.055	3800	4.4 x 4.4 x 1.4
Wurth	744042001	1.0	0.030	2600	4.8 x 4.8 x 1.8

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Input Capacitor Selection

The input capacitor in a step-down DC-DC regulator reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. 10µF ceramic capacitors in parallel with a 0.1µF ceramic capacitor are recommended for most applications. The impedance of the input capacitor at the switching frequency should be less than that of the input source so that high-frequency switching currents do not pass through the input source. The input capacitor must meet the input ripple-current requirement imposed by the step-down regulator. Ceramic capacitors are preferred due to their resilience to power-up surge currents. Choose the input capacitor so that the temperature rise due to input ripple current does not exceed approximately +10°C. For a step-down DC-DC regulator, the maximum input ripple current is 1/2 of the output current. This maximum input ripple current occurs when the step-down regulator operates at 50% duty factor (V_{IN} = 2 x V_{OUT}). Refer to the MAX8952 Evaluation Kit for specific input capacitor recommendations.

Output Capacitor Selection

The step-down DC-DC regulator output capacitor keeps output ripple small and ensures control-loop stability. A 10µF ceramic capacitor in parallel with a 0.1µF ceramic capacitor is recommended for most applications. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and lowest high-frequency impedance.

Output ripple due to capacitance (neglecting ESR) is approximately:

$$V_{RIPPLE} = \frac{I_{L(PEAK)}}{2\pi \times f_{OSC} \times C_{OUT}}$$

Additional ripple due to capacitor ESR is:

$$V_{RIPPLE}(ESR) = I_{L(PEAK)} \times ESR$$

Refer to the MAX8952 Evaluation Kit for specific output capacitor recommendations.

Power Dissipation

The IC has a thermal-shutdown feature that protects the IC from damage when the die temperature exceeds +160°C. See the *Thermal-Overload Protection* section for more information. To prevent thermal overload and allow the maximum load current on each regulator, it is important to ensure that the heat generated by the IC can be dissipated into the PCB.

When properly mounted on a multilayer PCB, the junction-to-ambient thermal resistance (θ_{JA}) is typically 49°C/W.

PCB Layout

Due to fast switching waveforms and high current paths, careful PCB layout is required to achieve optimal performance. Minimize trace lengths between the IC and the inductor, the input capacitor, and the output capacitor; keep these traces short, direct, and wide. The ground connections of C_{IN} and C_{OUT} should be as close together as possible and connected to PGND. Connect AGND and PGND directly to the ground plane. The MAX8952 Evaluation Kit illustrates an example PCB layout and routing scheme.

Special care should be taken when routing the remote sense signals. Use a wide SNS+ trace to minimize parasitic inductance in the SNS+ feedback trace. Do not use vias on the SNS+ trace because these introduce additional inductance. Connect SNS- to the local AGND plane for the MAX8952.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 WLP	W162B2+1	**21-0200**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/10	Initial release	—
1	6/11	Updated remote sense, *Typical Operating Circuit*, SNS+ and SNS- impedance entry, C1 bump description, Figure 1, and *PCB Layout* section	1, 5, 10, 11, 30