# NAU85L40B

## Quad Audio ADC with Integrated FLL and Microphone Preamplifier

### Description

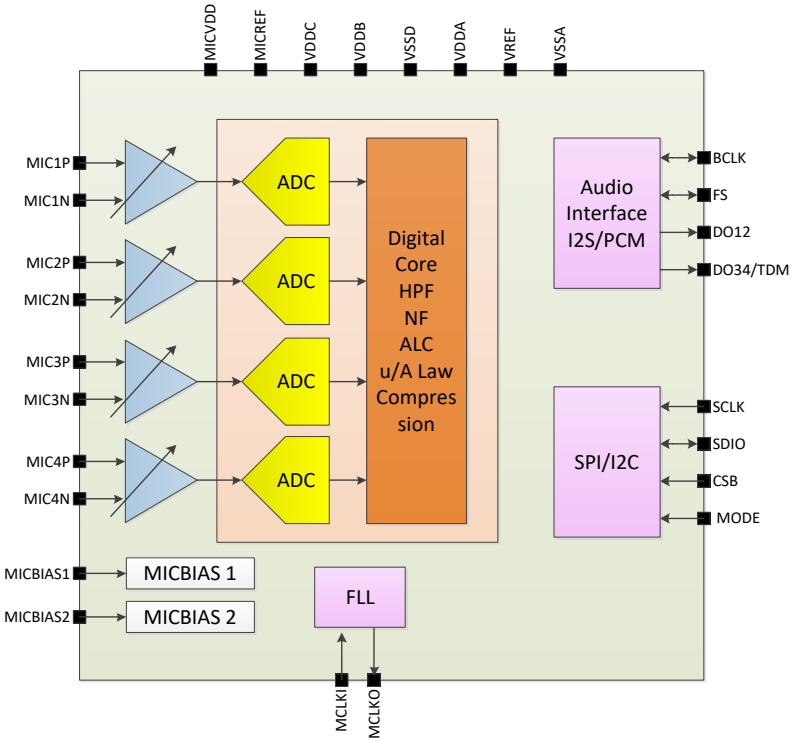
The NAU85L40B is a low power, high quality, 4-channel ADC for microphone array application. The NAU85L40B integrates programmable gain preamplifiers for quad differential microphones, significantly reducing external component requirements. A fractional FLL is available to accurately generate any audio sample rate using any commonly available system clock source from 8KHz through 33MHz. Audio data can be directed to two I2S data out lines or onto a single time division multiplexed (TDM) PCM data output.

The NAU85L40B operates with analog supply voltages from 1.6V to 2V, while the digital core can operate down to 1.2V to conserve power. Internal register controls enable flexible power saving modes by powering down sub-sections of the chip under software control. The NAU85L40B is specified for operation from -40°C to +85°C, and is available in a 28-lead QFN package.

### Features

- 103dB SNR (A-weighted) @ 0dB gain, VDDA=1.8V, Fs = 16 kHz, OSR=256x
- 92dB THD+N @ 0dB gain, 0.8Vrms in, VDDA=1.8V, Fs=48 kHz, OSR=128x
- -124dB Channel Crosstalk @ 0dB gain, 0.9Vrms in, VDDA=1.8V, Fs=48 kHz, OSR=128x
- Integrated programmable gain microphone amplifier
- On-chip FLL
- I2C Serial control interface with read/write capability
- Supports sample rates from 8 kHz to 48 kHz at 24-bit resolution
- Two separate microphone bias supplies for low noise microphone biasing.
- Standard audio data bus interfaces: I2S, Left or Right justified, TDM (4 channel), Two's compliment, MSB first
- 32-bit audio sub frames
- Package: Pb free 28L-QFN
- Temperature range: -40 to 85°

## Block Diagram



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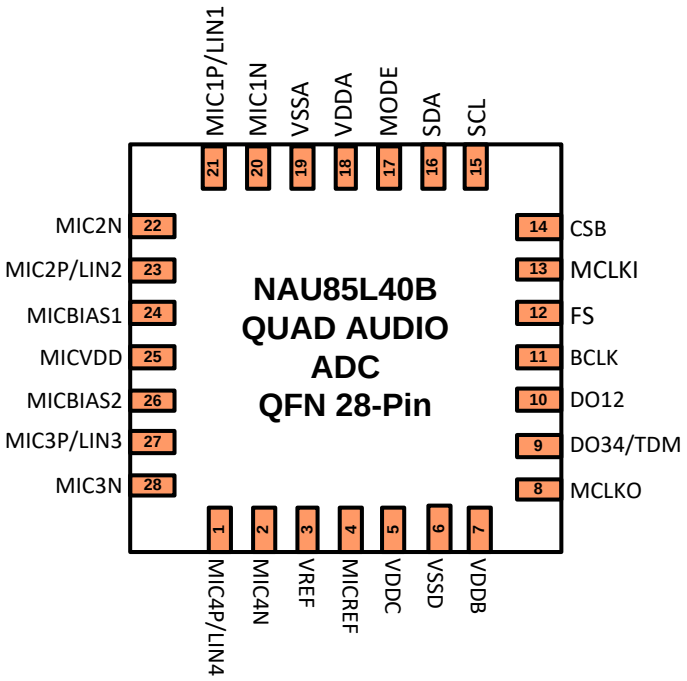


## Ordering Information

| Part Number | Dimension | Package | Package Material |
|---|---|---|---|
| NAU85L40YGB | 4 x 4 mm | 28 QFN | Green |

## Pin Description

| Pin # | Name | Type | Functionality |
|---|---|---|---|
| 1 | MIC4P/LIN4 | Analog Input | MICP Input 4 / Line In Input 4 |
| 2 | MIC4N | Analog Input | MICN Input 4 |
| 3 | VREF | Reference | Decoupling for Mid-rail Reference Voltage |
| 4 | MICREF | Analog Output | Decoupling for MIC Reference Voltage |
| 5 | VDDC | Supply | Digital Core Supply |
| 6 | VSSD | Supply | Digital Ground |
| 7 | VDDB | Supply | Digital Buffer (Input/Output) Supply |
| 8 | MCLKO | Digital Output | Output from PLL |
| 9 | DO34 | Digital Output | Digital Audio ADC Data Output for ADC 3 and 4 or TDM |
| 10 | DO12 | Digital Output | Digital Audio ADC Data Output for ADC 1 and 2 |
| 11 | BCLK | Digital I/O | Digital Audio Bit Clock |
| 12 | FS | Digital I/O | Digital Audio Frame Sync |
| 13 | MCLKI | Digital Input | Master Clock Input |
| 14 | CSB | Digital Input | 3-Wire MPU Chip Select/I2C address LSB |
| 15 | SCL | Digital Input | 3-Wire MPU Clock Input/I2C Clock (SCL) |
| 16 | SDA | Digital I/O | 3-Wire MPU Data Input/I2C Data I/O (SDA) |
| 17 | MODE | Digital Input | Control Interface Mode Selection Pin (I2C=1, SPI=0). This pin has to be tied to VDDB or VSSD only, depending on the applicable serial interface mode’ |
| 18 | VDDA | Supply | Analog Power Supply |
| 19 | VSSA | Supply | Analog Ground |
| 20 | MIC1N | Analog Input | MICN Input 1 |
| 21 | MIC1P/LIN1 | Analog Input | MICP Input 1 / Line In Input 1 |
| 22 | MIC2N | Analog Input | MICN Input 2 |
| 23 | MIC2P/LIN2 | Analog Input | MICP Input 2 / Line In Input 2 |
| 24 | MICBIAS1 | Analog Output | Microphone Bias for Microphone ADC 1 and 2 |
| 25 | MICVDD | Supply | Microphone Supply |
| 26 | MICBIAS2 | Analog Output | Microphone Bias for Microphone ADC 3 and 4 |
| 27 | MIC3P/LIN3 | Analog Input | MICP Input 3 / Line In Input 3 |
| 28 | MIC3N | Analog Input | MICN Input 3 |

## Electrical Characteristics

Conditions: VDDA = VDDC=1.8V, VDDB = 3.3V, MICVDD=3.3V, MCLK = 12.88MHz, $T_A$ = +25°C, 1 kHz signal, Fs = 48 kHz, 24-bit audio data, with differential inputs unless otherwise stated.

| Symbol | Parameter | Conditions | Typical | Limit | Units (Limit) |
|---|---|---|---|---|---|
| ISD | Shutdown Current | $V_{DD}$A | 0.5 | 1 | µA |
| | | $V_{DD}$A When $V_{DD}$C=1.2V | 16.7 | | |
| | | $V_{DD}$B | 0.2 | 1 | |
| | | $V_{DD}$C | 2 | 10 | |
| | | $V_{DD}$MIC | 0.5 | 1 | |
| **ADC** | | | | | |
| THD+N | ADC Total Harmonic Distortion + Noise | MIC Input, MIC_GAIN = 6dB, f=1KHz, Fs = 16KHz, OSR=128X | -92 | -80 | dB |
| | | Reference= @ 0dB gain, 0.8Vrms in, VDDA=1.8V, Fs=48 kHz, OSR=128x | -92 | | dB |
| SNR<br>Signal to Noise Ratio | | Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 0dB,fs = 8KHz, Mono Differential Input | 101 | | dB |
| | | Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 6dB,fs = 8KHz, Mono Differential Input | 100 | | dB |
| | | Reference== VOUT(0dBFS), (A-weighted) @ 0dB gain, VDDA=1.8V, Fs = 16 kHz, OSR=256x | 103 | | dB |
| | | Reference = VOUT(0dBFS), A-Weighted, Quad Input, Gain = 12dB,fs = 16KHz, OSR=256x | 100 | | dB |
| | | Reference = VOUT(0dBFS), A-Weighted, Quad Input, Gain = 12dB,fs = 16KHz, OSR=128x | 98 | | dB |
| | | Reference= MIC Gain= 0dB gain, (A-weighted) VDDA=1.8V, Fs = 48 kHz, OSR=128x | 101 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_{RIPPLE}$ = 200mVP_P applied to AVDD, $f_{RIPPLE}$ = 217Hz, Input Referred, MIC_GAIN = 0dB Differential Input | 65 | | dB |
| Xtalk | ADC channel cross talk | MIC Input, MIC_GAIN = 0dB, VIN = 0.8Vrms, f=1KHz, Fs = 48KHz , Channel 1(3) to Channel 2 (4) | -124 | | dB |
| $FS_{ADC}$ | ADC Full Scale Input Level | $AV_{DD}$ = 1.8V | 1 | | $V_{RMS}$ |
| **MICBIAS** | | | | | |
| $V_{BIAS}$ | Output Voltage | Programmable 2.1V to 2.8V in 0.1V Steps | 2.5 | | V |
| $I_{OUT}$ | Output Current | | | 4 | mA |

| | | | | | |
|---|---|---|---|---|---|
| $e_{OS}$ | Output Noise | A-weighted 20Hz-20kHz | -115 | | dBV |

**Notes**

1. Full Scale input level is relative to the magnitude of VDDA and can be calculated as FS = $1V_{rms}$*VDDA/1.8.
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurements is at 3dB below full scale, unless otherwise noted.
3. Unused analog input pins should be left as no-connection.
4. Unused digital input pins should be tied to ground.

## Digital I/O

| Parameter | Symbol | Comments/Conditions | | Min | Max | Units |
|---|---|---|---|---|---|---|
| Input LOW level | $V_{IL}$ | VDDB = 1.8V | | | 0.33 * VDDB | V |
| | | VDDB = 3.3V | | | 0.37 * VDDB | |
| Input HIGH level | $V_{IH}$ | VDDB = 1.8V | | 0.67 * VDDB | | V |
| | | VDDB = 3.3V | | 0.63 * VDDB | | |
| Output HIGH level | $V_{OH}$ | $I_{Load}$ = 1mA | VDDB = 1.8V | 0.9 * VDDB | | V |
| | | | VDDB = 3.3V | 0.95 * VDDB | | |
| Output LOW level | $V_{OL}$ | $I_{Load}$ = 1mA | VDDB = 1.8V | | 0.1 * VDDB | V |
| | | | VDDB = 3.3V | | 0.05 * VDDB | |

## Recommended Operating Conditions

| Condition | Symbol | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| Digital Supply Range with sample rate > 48 kHz or FLL enabled | VDDC | 1.62 | 1.8 | 1.98 | V |
| Digital Supply Range with sample rate <= 48kHz and FLL disabled | VDDC | 1.2 | 1.8 | 1.98 | V |
| Digital I/O Supply Range | VDDB | 1.62 | 1.8 | 3.6 | V |
| Analog Supply Range | VDDA | 1.62 | 1.8 | 1.98 | V |
| Microphone Bias Supply Voltage | VDDMIC | 2.5 | 4.2 | 5.5 | V |
| Temperature Range | $T_A$ | -40 | | +85 | °C |

*CAUTION: Below conditions needed to be followed for regular operation: VDDB > VDDC – 0.6V.*

## Absolute Maximum Ratings

| Parameter | Min | Max | Units |
|---|---|---|---|
| Digital Supply Range (VDDC) | -0.3 | 2.2 | V |
| Digital I/O Supply Range (VDDB) | -0.3 | 6.0 | V |
| Analog Supply Range (VDDA) | -0.3 | 2.2 | V |
| Microphone Bias Supply Voltage (MICVDD) | -0.3 | 6.0 | V |
| Voltage Input Digital Range | VSSD - 0.3 | VDDB + 0.3 | V |
| Voltage Input Analog Range | VSSA - 0.3 | VDDA + 0.3 | V |
| Junction Temperature, $T_J$ | -40 | +150 | °C |
| Storage Temperature | -65 | +150 | °C |

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.*

*CAUTION: The following condition need to be followed for maximum ratings: VDDB > VDDC – 0.6V.*

# 1 General Description

The NAU85L40B is a low power, high quality, 4-channel ADC for microphone array applications. There are eight analog inputs with individual input PGA gain stages and are passed to the ADC path for signal processing. A low noise microphone bias circuit supplies a programmable voltage reference for one or more electret microphones on two buffered MICBIAS outputs that are available to separately supply microphones associated with channels 1 & 2 and channels 3 & 4. The digital audio data from the ADC's can be processed by a Volume Control, High Pass filter, and ALC before it is passed on to the serial I2S or TDM PCM interface. This digital serial output data can be available in two separate dual channel formats on ADCOUT12 for channel 1 & 2 and ADCOUT34 for channel 3 & 4. The 4-channel serial digital audio can also be combined into one serial bit stream on ADCOUT34 in TDM mode. The device clock can be locked to an external clock reference or generated internally by the on-chip FLL. The registers that control the NAU85L40B can be programmed through standard I2C or SPI interface.

# 2 Analog Inputs

NAU85L40B has four low noise, high common mode rejection ratio analog microphone differential inputs – MIC1/MIC1P together are MIC.1, MIC2N/MIC2P together are MIC.2, MIC3N/MIC3P together are MIC.3, MIC4N/MIC4P together are MIC.4. Each of these microphone inputs are followed by a -1dB to 36dB PGA gain stage with a fixed 12kOhm input impedance.

All inputs are maintained at a DC bias at approximately 1/2 of the VDDA supply voltage. Connections to these inputs should be AC-coupled by means of DC blocking capacitors suitable for the device application.

The differential microphone input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary such as in portable digital media devices and cell phones. Differential inputs are also very useful to reduce ground noise in systems in which there are ground voltage differences between different chips and components. When properly implemented, the differential input architecture offers an improved power-supply rejection ratio (PSRR) and higher ground noise immunity.

A detailed diagram of the input PGA connections and associated registers is shown in Figure 1. The PGA inputs can also be disconnected from the amplifier for applications where the inputs are shared with other devices. In addition, there is a pre-charge circuit that can speed up charging the external coupling capacitor set with ERROR! REFERENCE SOURCE NOT FOUND..**ACDC_CTRL REG0X6A[15:8]**. The PGA ain can be set from -1dB to 36dB in 1dB steps and the embedded antialiasing filter also has a single bit adjustment to shift the cut-off frequency.

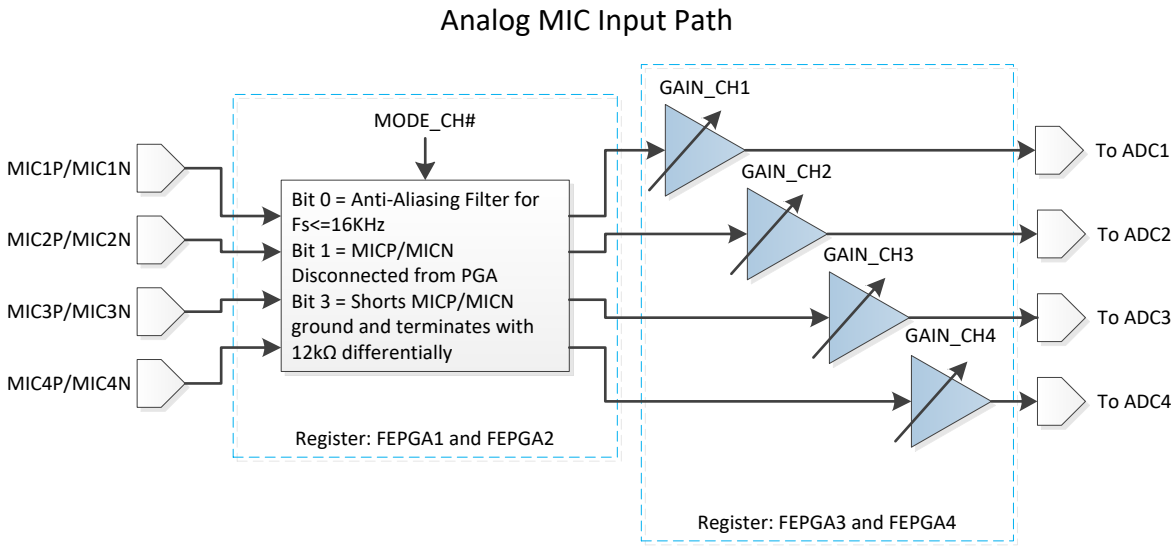


Figure 1: Analog Input Structure

## 2.1 ADC and Digital Signal Processing

The NAU85L40B has four independent high quality ADCs. These are high performance 24-bit sigma-delta converters that are suitable for a very wide range of applications. All digital processing is with 24-bit precision minimizing processing artifacts and maximizing the audio dynamic range supported by the NAU84L04.

The ADCs are supported by a wide range mixed-mode Automatic Level Control (ALC), a high pass filter, and a notch filter. All of which are optional and programmable. The high pass filter function is intended for DC-blocking or low frequency noise reduction, such as to reduce unwanted ambient noise or "wind noise" on a microphone input. The notch filter may be programmed to greatly reduce a specific frequency band or frequency, such as a 50Hz, 60Hz, or 217Hz unwanted noise. The 4-channel ADC TDM interface also provides for flexible routing options.

## 2.2 ADC Digital Block

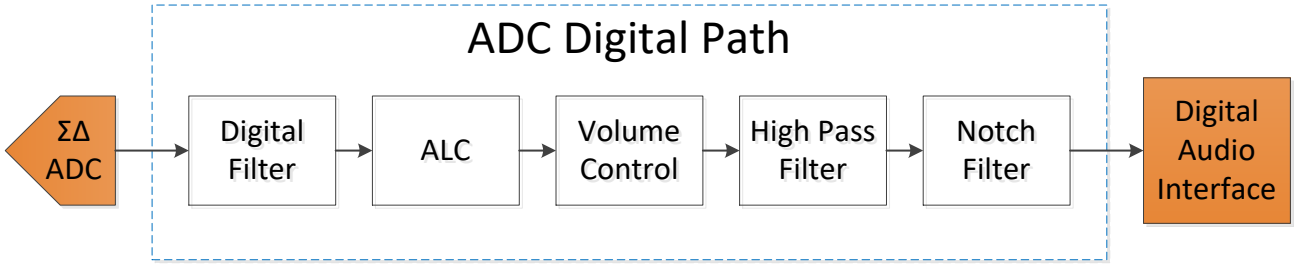


Figure 2: ADC Digital Path

The ADC digital block performs 24-bit analog-to-digital conversion and signal processing, making available a high quality audio sample stream the audio path digital interface. This block consists of a sigma-delta modulator, digital decimator/ filter, ALC, volume control, high pass filter, and a notch filter.

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### 2.2.1 Input Limiter / Automatic Level Control (ALC)

The ADC digital path of the NAU85L40B is supported by the digital Automatic Level Control (ALC) function. This can be used to automatically manage the gain to optimize the signal level at the output of the ADC by automatically amplifying input signals that are too small or decreasing the amplitude of the signals that are too loud.

The ALC monitors the output of the ADC, measured after the digital decimator. The ADC output is fed into a peak detector, which updates the measured peak value whenever the absolute value of the input signal is higher than the current measured peak. The measured peak gradually decays to zero unless a new peak is detected, allowing for an accurate measurement of the signal envelope. The peak value is then used by a logic algorithm to determine whether the gain should be increased, decreased, or remain the same.

In normal mode, when sudden peaks occur above the desired gain settings, the ALC reduces volume at a register determined rate and step size. This continues until the output level of the ADC is again at the desired target level. If the input signal suddenly becomes quiet, the ALC increases volume at a register determined rate and step size until the output level from the ADC reaches the target level. If the input gain stays within the target level, the ALC will remain in a steady state.

In addition to the normal operation mode, the ALC may be operated in a special limiter mode that functions similarly to the normal mode but with faster attack times. This mode is primarily used to quickly ramp down signals that are too loud.

#### 2.2.1.1 ALC Peak Limiter Function

Both normal and limiter mode include a peak limiter function. This implements an emergency gain reduction when the ADC output level exceeds a set gain value. When the ADC output exceeds 87.5% of full scale, the ALC block ramps down the gain at the maximum ALC Attack Time rate. This is regardless of the mode and attack rate settings. This continues until the ADC output level has been reduced to below the emergency limit threshold. This action limits ADC clipping if there is a sudden increase in the input signal level.

#### 2.2.1.2 ALC Parameter Definitions

ALC Maximum Gain (ALCMAX): This sets the maximum allowed gain during normal mode ALC operation. In the Limiter mode of ALC operation, the ALCMXGAIN value is not used, instead, the maximum gain allowed is set equal to the pre-existing gain value that was in effect at the moment in time that the Limiter mode is enabled.

ALC Minimum Gain (ALCMIN): This sets the minimum allowed gain during all modes of ALC operation. This is useful to keep the ALC operating range close to the desired range for a given application scenario.

ALC Target Value (ALCLVL): Determines the value used by the ALC logic decisions comparing this fixed value with the output of the ADC. This value is expressed as a fraction of Full Scale (FS) output from the ADC. Depending on the logic conditions, either the output value used in the comparison may be the instantaneous value of the ADC, or a time weighted average of the ADC peak output level. See.

ALC Attack Time (ALCATK): Attack time refers to how quickly a system responds to an increasing volume level that is greater than some defined threshold. Typically, attack time is much faster than decay time. In the NAU85L40B, when the absolute value of the ADC output exceeds the ALC Target Value, the gain will be reduced at a step size and rate determined by this parameter. When the peak ADC output is at least 1.5dB lower than the ALC Target Value, the stepped gain reduction will halt.

ALC Decay Time (ALCDCY): Decay time refers to how quickly a system responds to a decreasing volume level. Typically, decay time is much slower than attack time. When the ADC output level is below the ALC Target value by at least 1.5dB, the gain will increase at a rate determined by this parameter. In Limiter mode, the time constants are faster than in ALC mode. ALC Hold Time (ALCHLD): Hold time

refers to the duration of time when no action is taken. This is typically to avoid undesirable sounds that can happen when an ALC responds too quickly to a changing input signal. In the NAU85L40B, the hold time value is the duration of time that the ADC output peak value must be less than the target value before there is an actual gain increase. .

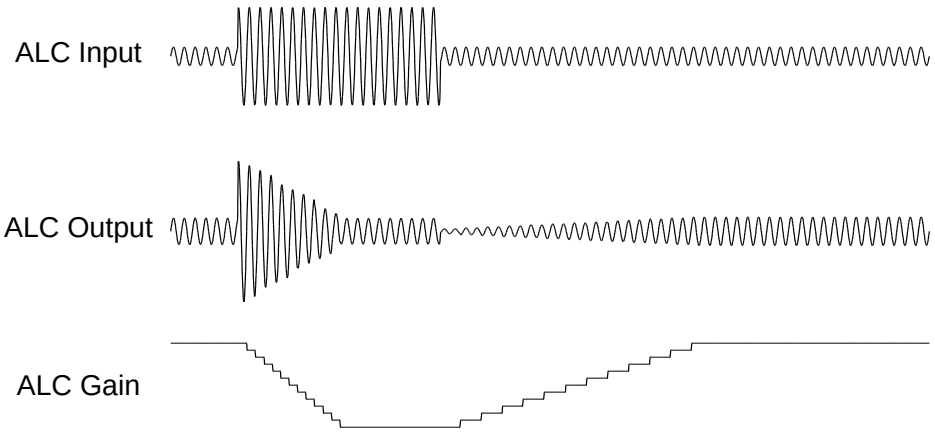



Figure 3: ALC Operation

#### 2.2.1.3 ALC Normal Mode Example Using ALC Hold Time Feature

Input signals with different characteristics (e.g., voice vs. music) may require different settings for this parameter for optimum performance. Increasing the ALC hold time prevents the ALC from reacting too quickly to brief periods of silence such as those that may appear in music recordings. Having a shorter hold time may be useful in voice applications where a faster reaction time helps to adjust the volume setting for speakers with different volumes.

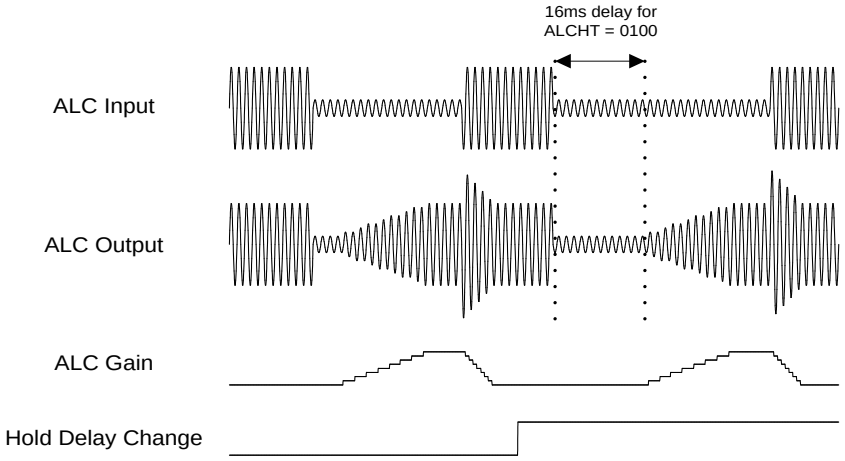



Figure 4: ALC using Hold time

#### 2.2.1.4 Noise Gate (Normal Mode Only)

A noise gate threshold prevents ALC amplification of noise when there is no input signal or no signal above an expected background noise level.

When there is no signal or a very quiet signal (pause) composed mostly of noise, the ALC holds the gain constant instead of amplifying the signal towards the target threshold. The NAU85L40B accomplishes this by comparing the input signal level against the noise gate threshold. The noise gate only operates in conjunction with the ALC and only in Normal mode.

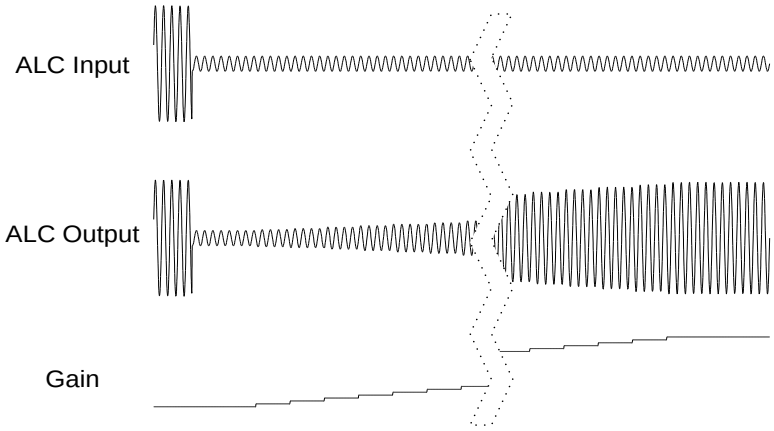



Figure 5: ALC without Noise gate

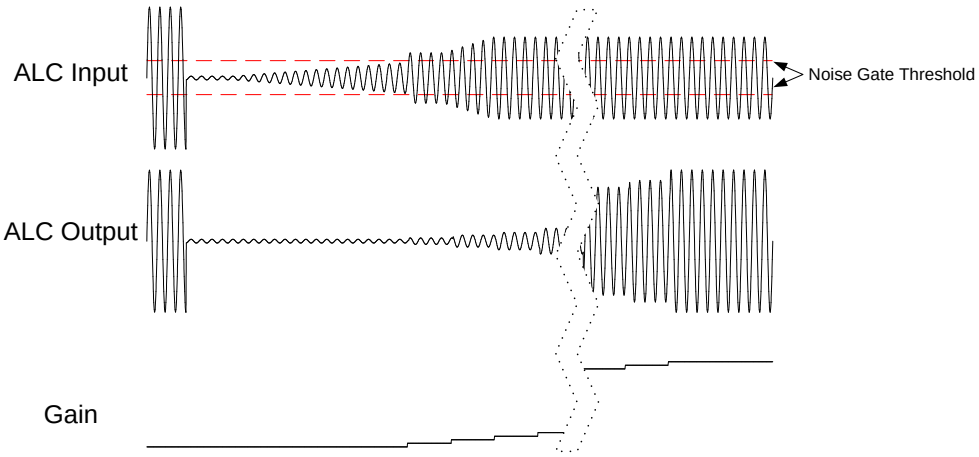
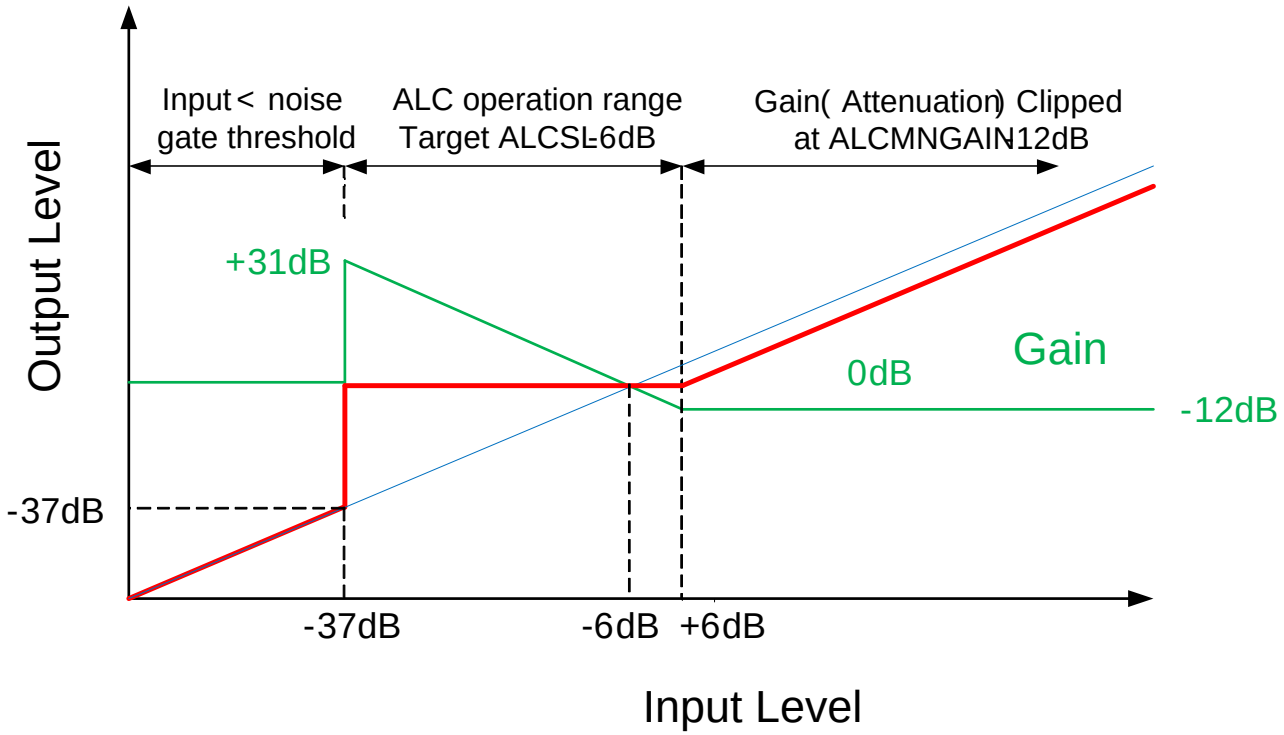



Figure 6: ALC with noise gate

#### 2.2.1.5 ALC Example with ALC Min/Max Limits and Noise Gate Operation

The drawing below shows the effects of ALC operation over the full scale signal range. The drawing is color coded as follows:

Blue Original Input signal (linear line from zero to maximum)
Green PGA gain value over time (inverse to signal in target range)
Red Output signal (held to a constant value in target range)




| Register | Bits | Name | Value | Description |
|---|---|---|---|---|
| 22 | 12-15 | ALCCH(1-4)E | 1111 | ALC enabled all channels |
| 21 | 12-14 | ALCMAXGAIN | 111 | Max ALC gain@ 35.25dB |
| 21 | 8-10 | ALCMINGAIN | 000 | Min ALC gain@ -12dB |
| 21 | 0-3 | ALCLVL | 1011 | Target ALC gain@ -6 dBFS |
| 20 | 4 | NGEN | 1 | Noise gate enabled |
| 20 | 0-3 | NGTH | 0100 | Noise gate@ -37dB |

Figure 7: ALC Response Envelope

### 2.2.2 ADC Digital Volume Control

The effective output audio volume of each ADC can be changed from +36dB through -128dB in 0.125dB steps using the digital volume control feature. Included in the volume control is a “digital mute” value that will completely mute the signal output of the ADC.

In addition, the ADC has an analog gain control, which can be set from -1dB to 36dB.

### 2.2.3 ADC Programmable High Pass Filter

A high pass filter in the digital output path optionally supports each ADC.

The high pass filter has two different operating modes. In the audio mode, the filter is a simple first order DC blocking filter, with a cut-off frequency of 3.7Hz. In the application specific mode, the filter is a second order audio frequency filter, with a programmable cut-off frequency. The following table provides the exact cutoff frequencies with different sample rates. These cutoff frequencies can be selected by setting the registers.

| HPF_CUT | SMPL_RATE REG0X3A[7:5] in kHz (FS) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 101 or 100 | | | 011 or 010 | | | 001 or 000 | | |
| | 8 | 11.025 | 12 | 16 | 22.05 | 24 | 32 | 44.1 | 48 |
| 000 | 82 | 113 | 122 | 82 | 113 | 122 | 82 | 113 | 122 |
| 001 | 102 | 141 | 153 | 102 | 141 | 153 | 102 | 141 | 153 |
| 010 | 131 | 180 | 156 | 131 | 180 | 156 | 131 | 180 | 156 |
| 011 | 163 | 225 | 245 | 163 | 225 | 245 | 163 | 225 | 245 |
| 100 | 204 | 281 | 306 | 204 | 281 | 306 | 204 | 281 | 306 |
| 101 | 261 | 360 | 392 | 261 | 360 | 392 | 261 | 360 | 392 |
| 110 | 327 | 450 | 490 | 327 | 450 | 490 | 327 | 450 | 490 |
| 111 | 408 | 563 | 612 | 408 | 563 | 612 | 408 | 563 | 612 |

Table 1: High Pass Filter Cut-off Frequencies in Hz (with HPF_AM = 1)

### 2.2.4 Programmable Notch Filter

A notch filter in the digital output path optionally supports each ADC. The notch filter is used to stop a very narrow band of frequencies around a center frequency.

It is important to note that the register update bits are write-only bits. The update bit function is important so that all filter coefficients actively being used are changed simultaneously; even though the register values must be written sequentially. When there is a write operation to any of the filter coefficient settings, but the update bit is not set (value = 0), the value is stored as pending a future update, but does not go into effect. When there is a write operation to any coefficient register, and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any other pending coefficient value is put into effect at the same time.

| $A_0$ | $A_1$ | Notation | Register Value (DEC) |
|---|---|---|---|
| $\frac{1-\tan\frac{2\pi f_b}{2f_s}}{1+\tan\frac{2\pi f_b}{2f_s}}$ | $-(1+A_0)\times\cos\frac{2\pi f_c}{f_s}$ | $f_c$ = center frequency (Hz)<br>$f_b$ = -3dB bandwidth (Hz)<br>$f_s$ = sample frequency (Hz) | NFCA0 = $-A_0 \times 2^{13}$<br>NFCA1 = $-A_1 \times 2^{12}$<br>Note: Values are rounded to the nearest whole number and converted to 2's complement |

Table 2: Equations to calculate notch filter coefficients

## 2.3 Audio Data Companding

Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates, using non-linear algorithms. The NAU85L40B supports the two main telecommunications companding standards: A-law and µ-law. The A-law algorithm is primarily used in European communication systems and the µ-law algorithm is primarily used by North America, Japan, and Australia.

Companding converts 13 bits (µ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. The companded signal is an 8bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits)

Following are the data compression equations set in the ITU-T G.711 standard and implemented in the NAU85L40B.

### 2.3.1 µ-law

$$F(x) = \frac{\ln(1+\mu\times|x|)}{\ln(1+\mu)}, \qquad -1 < x < 1$$

$$\mu = 255$$

### 2.3.2 A-law

$$F(x) = \frac{A \times |x|}{(1 + \ln(A))}, \qquad x \le \frac{1}{A}$$

$$F(x) = \frac{(1 + \ln(A \times |x|)}{(1 + \ln(A))}, \qquad \frac{1}{A} \le x \le 1$$

$$A = 87.6$$

## 2.4 Digital Interfaces

Command and control of the device is accomplished using a 2-wire/3-wire serial control interface. This simple, but highly flexible, interface is compatible with many commonly used command and control serial data protocols and host drivers. .

Digital audio input/output data streams are transferred to and from the device separately for command and control. The digital audio data interface supports either I2S or PCM audio data protocols, and is compatible with commonly used industry standard devices that follow either of these two serial data formats.

**Power Supply**

The NAU85L40B has been designed to operate reliably using a wide range of power supply conditions and power-on/power-off sequences. However, because of existence of ESD protection diodes between the supplies, that will have impact on the application of the supplies. Because of these diodes, the following conditions need to be met:

VDDB > VDDC – 0.6V.

## 2.5 Power on and off reset

The NAU85L40B includes a power on and off reset circuit on chip. The circuit resets the internal logic control at VDDC and VDDA supply power up and this reset function is automatically generated internally when power supplies are too low for reliable operation. The reset threshold is approximately 0.55Vdc and 1.0Vdc for VDDC and VDDA, respectively. It should be noted that these values are much lower than the required voltage for normal operation of the chip.

The reset is held on while the power levels for both VDDC and VDDA are below their respective thresholds. Once the power levels rise above their thresholds, the reset is released. Once the reset is released, the registers are ready to be written to. It is also important to note that all the registers should be kept in their reset state for at least 6µs.

An additional internal RC filter based circuit is added which helps the circuit respond for fast ramp rates (~10µs) and generate the desired reset period width (~10µs at typical corner). This filter is also used to eliminate supply glitches which can generate a false reset condition, typically 50ns.

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Note that when VDDA and/or VDDC are below the power on reset threshold, then the digital IO pins will go into a tri-state condition.

## 2.6 Reference Voltage Generation

The NAU85L40B includes a mid-supply reference circuit that is decoupled to VSS through the VREF pin by means of a bypass capacitor. The VREF voltage is used as the reference for the majority of the circuits inside NAU85L40B. Therefore, the bypass capacitor needs to be large in order to achieve good power supply rejection at low frequencies. Typically, a 4.7uF capacitor can be used. However, a larger value can be chosen but it will increase the rise time of VREF and therefore it will delay the valid line output signal. However, a pre-charge circuit can pre-charge the capacitor close to VDDA/2 at power up in order to reduce the rise time for fast line out availability. This bypass capacitor should also be low leakage due to the high impedance nature of the VREF pin

impedance is set as per the following table.

| VMIDSEL REG0X60[5:4] | VREF Resistor Selection | VREF Impedance |
|---|---|---|
| 00 | Open, no resistor selected | Open, no impedance installed |
| 01 | 50kOhm | 25kOhm |
| 10 | 250kOhm | 125kOhm |
| 11 | 5kOhm | 2.5kOhm |

Table 3: $V_{REF}$ Impedance

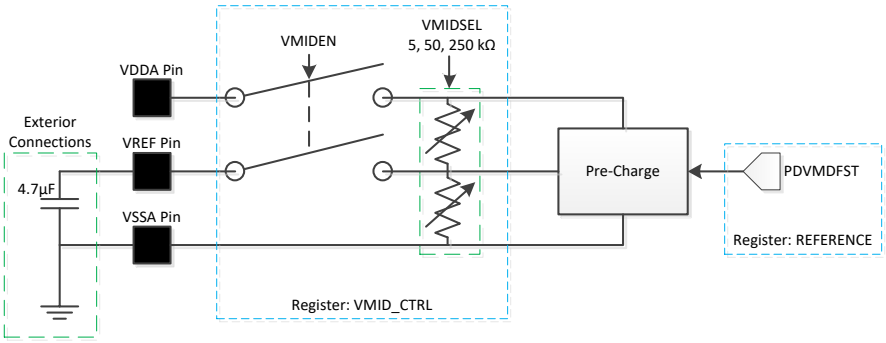


Figure 8: $V_{REF}$ Circuitry

## 2.7 Microphone Bias Generation

The NAU85L40B provides two microphone bias pins which can be used in various stereo applications. The microphone bias can be used to power electret microphones. In order to ensure safe operation of the device, it is recommended that the microphones do not draw more than 4mA of current from each MICBIAS pin.

# 3 Clocking and Sample Rates

The internal clocks for the NAU85L40B are derived from a common internal clock source, MCLK. This clock is the reference for the ADCs and DSP core functions, digital audio interface and other internal functions.

MCLK can be derived directly from MCLKI pin or may be generated from a Frequency Locked Loop (FLL) using MCLKI, BCLK or FS as a reference. The FLL provides additional flexibility for a wide range of MCLK frequencies and can be used to generate a free-running clock in the absence of an external reference source.

for further details.

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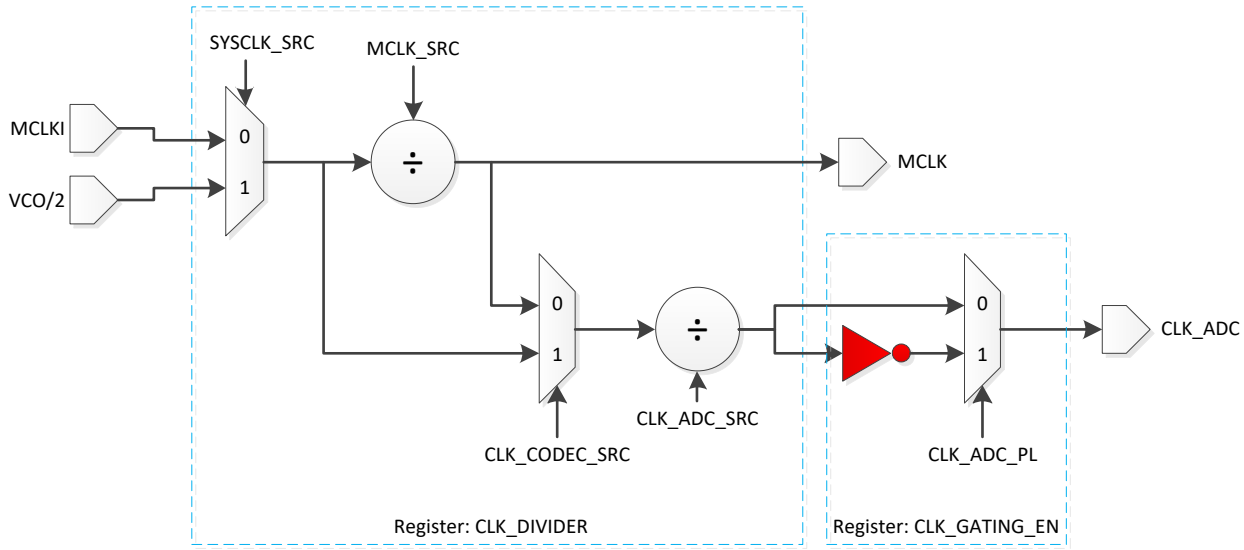


Figure 9: Clock Generation

| Bits | MCLK_SRC REG0X03[4:0] |
|---|---|
| 0000 | Divide by 1 |
| 0001 | Invert |
| 0010 | Divide by 2 |
| 0011 | Divide by 4 |
| 0100 | Divide by 8 |
| 0101 | Divide by 16 |
| 0110 | Divide by 32 |
| 0111 | Divide by 3 |
| 1001 | Invert |
| 1010 | Divide by 6 |
| 1011 | Divide by 12 |
| 1100 | Divide by 24 |

Table 4: ERROR! REFERENCE SOURCE NOT FOUND..**MCLK_SRC REG0X03[4:0]** Register Settings

| Bits | CLK_ADC_SRC REG0X03[7:6] |
|---|---|
| 00 | Divide by 1 |
| 01 | Divide by 2 |
| 10 | Divide by 4 |
| 11 | Divide by 8 |

Table 5:

.

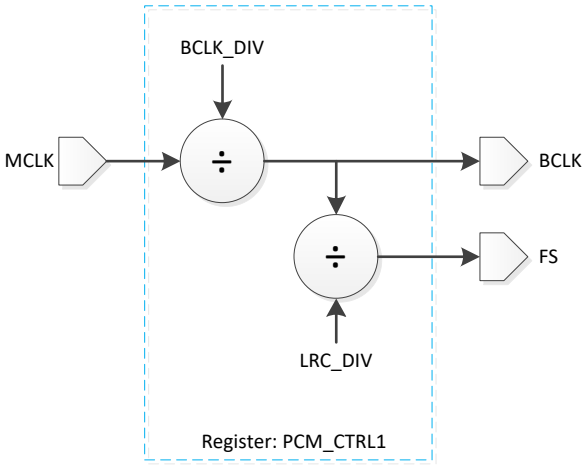


Figure 10: Master Mode PCM Clock Generation

| Bits | BCLK_DIV REG0X11[2:0] |
|---|---|
| 000 | Divide by 1 |
| 001 | Divide by 2 |
| 010 | Divide by 4 |
| 011 | Divide by 8 |
| 100 | Divide by 16 |
| 101 | Divide by 32 |

| Bits | LRC_DIV REG0X11[13:12] |
|---|---|
| 00 | Divide by 256 |
| 01 | Divide by 128 |
| 10 | Divide by 64 |
| 11 | Divide by 32 |

## 3.1 Frequency Locked Loop (FLL)

The integrated FLL can be used to generate a master system clock, MCLK, from MCLKI, BCLK or FS as a reference. Because of the FLL's tolerance of jitter, it may be used to generate a stable MCLK from less stable input clock sources or it can be used to generate a free-running clock in the absence of an external reference clock source.

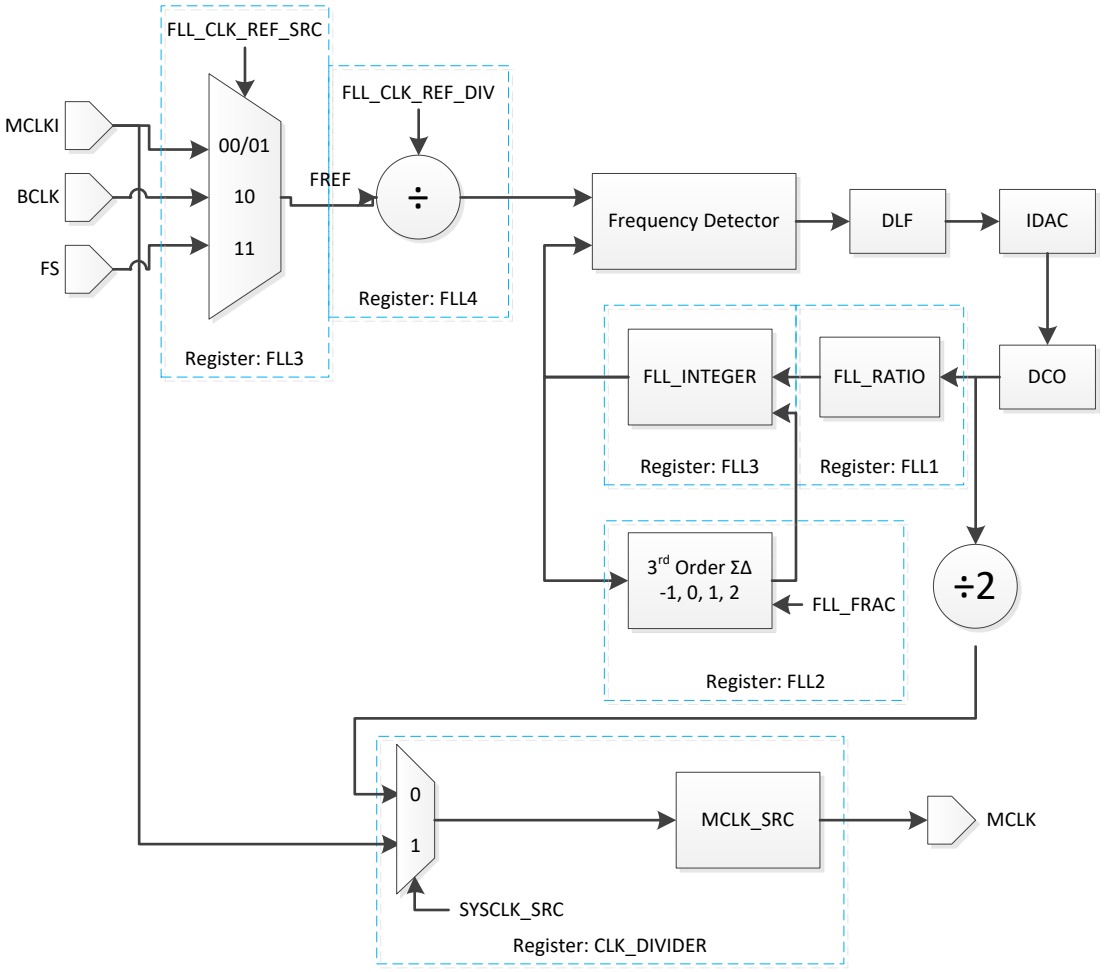


Figure 11: FLL Block diagram

# 4 Control Interfaces

## 4.1 Selection of Control Mode

The NAU85L40B features include a serial control bus that provides access to all of the device control registers. This bus may be configured either as a 2-wire interface that is interoperable with industry standard implementations of the I2C serial bus, or as a 3-wire bus compatible with commonly used industry implementations of the SPI (Serial Peripheral Interface) bus.

The timing in all three bus configurations is fully static resulting in good compatibility with standard bus interfaces and software simulated buses. A software simulated bus can be very simple and low cost, such as by utilizing general purpose I/O pins on the host controller and software “bit banging” techniques to create the required timing.

## 4.2 2-Wire-Serial Control Mode (I²C Style Interface)

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and the receiving device as the receiver (or slave). The NAU85L40B can function only as a slave device when in the 2-wire interface configuration.

## 4.3 2-Wire Protocol Convention

All 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH. All 2-Wire interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

An acknowledge (ACK), is a software convention used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.

Following a START condition, the master must output a device address byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W=1, this indicates the master is initiating a read operation from the slave device, and when R/W=0, the master is initiating a write operation to the slave device. If the device address matches the address of the slave device, the slave will output an ACK during the period when the master allows for the ACK signal.

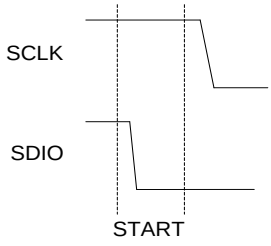


Figure 12: Valid START Condition

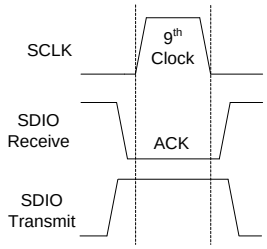


Figure 13: Valid Acknowledge

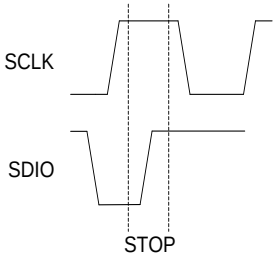


Figure 14: Valid STOP Condition

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 | csb | R/W | Device Address Byte |
| A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | Control Address Bytes |
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | Data Bytes |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |

Figure 15: Slave Address Byte, Control Address Bytes, and Data Byte Order

## 4.4 2-Wire Write Operation

A Write operation consists of a three-byte instruction followed by one or more Data Bytes. A Write operation requires a START condition, followed by a valid device address byte with R/W=0, a valid control address byte, data byte(s), and a STOP condition.

The Device Address of the NAU85L40B is either 0x1C (CSB=0) or 0x1D (CSB=1). In I2C mode the CSB pin will set the LSB of the Slave Address. If the Device Address matches this value, the NAU85L40B will respond with the expected ACK signaling as it accepts the data being transmitted to it.

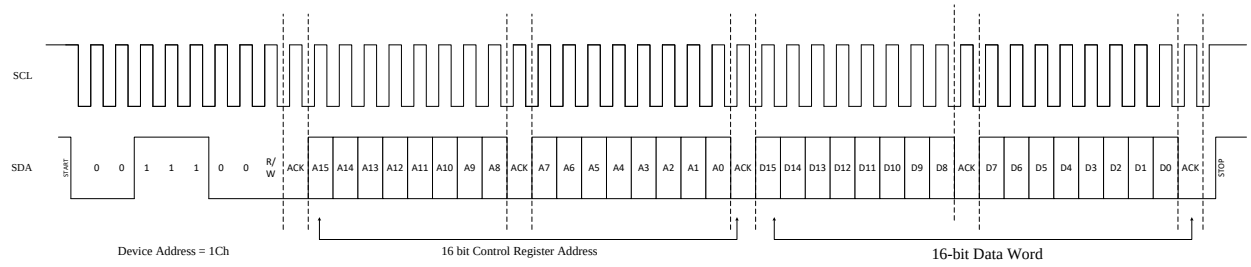


Figure 16: Byte Write Sequence

## 4.5 2-Wire Read Operation

A Read operation consists of a three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, device address byte with the R/W bit set to “0”, and a Control Register Address byte. This indicates to the slave device which of its control registers is to be accessed.

If the device address matches this value, the NAU85L40B will respond with the expected ACK signaling as it accepts the Control Register Address being transmitted into it. After this, the master transmits a second START condition, and a second instantiation of the same device address, but now with R/W=1.

After again recognizing its device address, the NAU85L40B transmits an ACK, followed by a two byte value containing the 16 bits of data from the selected control register inside the NAU85L40B.

During this phase, the master generates the ACK signaling with each byte transferred from the NAU85L40B. If there is no STOP signal from the master, the NAU85L40B will internally auto-increment the target Control Register Address and then output the two data bytes for this next register in the sequence.

This process will continue as long as the master continues to issue ACK signaling. If the Control Register Address being indexed inside the NAU85L40B reaches the value 0xFFFF (hexadecimal) and the value for this register is output, the index will roll over to 0x0000. The data bytes will continue to be output until the master terminates the read operation by issuing a STOP condition.

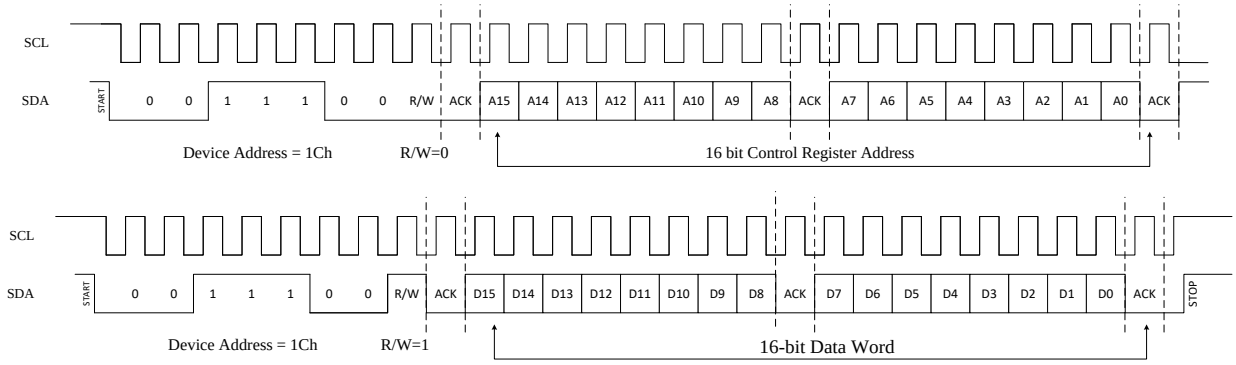


Figure 17: Read Sequence

## 4.6 Digital Serial Interface Timing

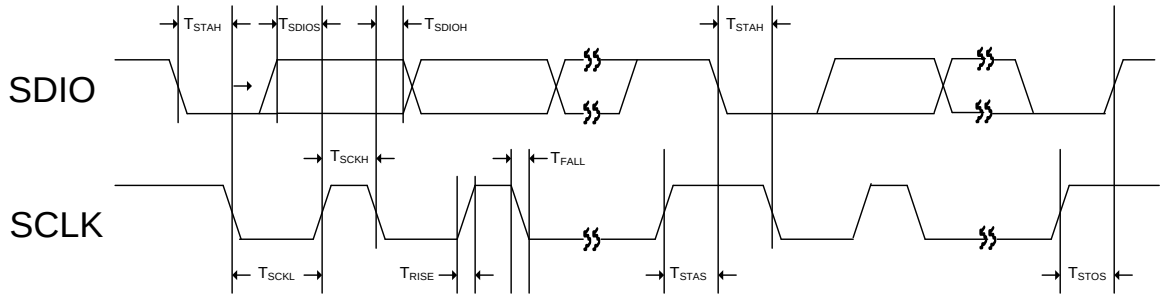


Figure 18: Two-Wire Control Mode Timing

| Symbol | Description | min | typ | max | unit |
|---|---|---|---|---|---|
| $T_{STAH}$ | SDIO falling edge to SCLK falling edge hold timing in START / Repeat START condition | 600 | - | - | ns |
| $T_{STAS}$ | SCLK rising edge to SDIO falling edge setup timing in Repeat START condition | 600 | - | - | ns |
| $T_{STOS}$ | SCLK rising edge to SDIO rising edge setup timing in STOP condition | 600 | - | - | ns |
| $T_{SCKH}$ | SCLK High Pulse Width | 600 | - | - | ns |
| $T_{SCKL}$ | SCLK Low Pulse Width | 1,300 | - | - | ns |
| $T_{RISE}$ | Rise Time for all 2-wire Mode Signals | - | - | 300 | ns |
| $T_{FALL}$ | Fall Time for all 2-wire Mode Signals | - | - | 300 | ns |
| $T_{SDIOS}$ | SDIO to SCLK Rising Edge DATA Setup Time | 100 | - | - | ns |
| $T_{SDIOH}$ | SCLK falling Edge to SDIO DATA Hold Time | 0 | - | 600 | ns |

## 4.7 Software Reset

The entire NAU85L40B and all of its control registers can be reset to default initial conditions .

# 5 Digital Audio Interface

The NAU85L40B can be configured as either the master or the slave. By default, the NAU85L40B is in Slave mode. In master mode, NAU85L40B outputs both Frame Sync (FS) and the audio data bit clock (BCLK) which has full control of the data transfer. In the slave mode, an external controller supplies BCLK and FS. Data is latched on the rising edge of BCLK.

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Table 6: Digital Audio Interface Normal Modes

## 5.1 Right-Justified Audio Data

In right-justified mode, the LSB is clocked on the last BCLK rising edge before FS transitions. When FS is HIGH, left channel data is transmitted and when FS is LOW, right channel data is transmitted. This is shown in the figure below where N is the word length.

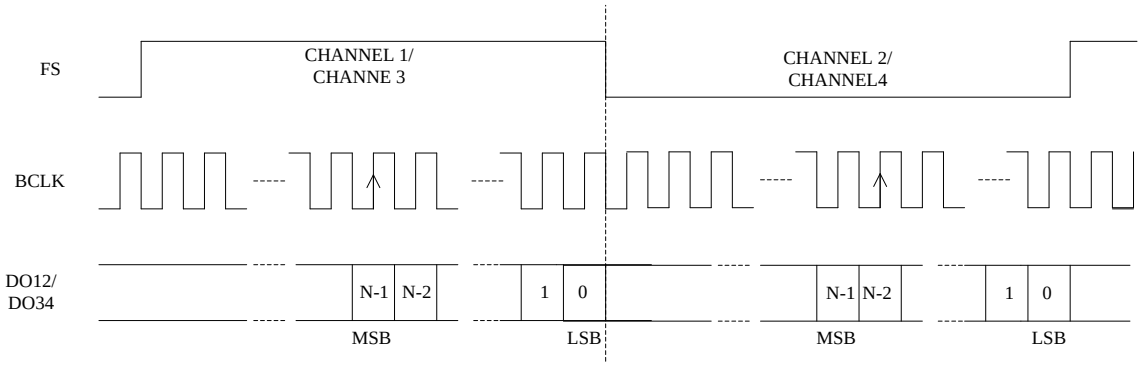



Figure 19: Right Justified Audio Format

## 5.2 Left-Justified Audio Data

In left-justified mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, left channel data is transmitted and when FS is LOW, right channel data is transmitted. This is shown in the figure below.

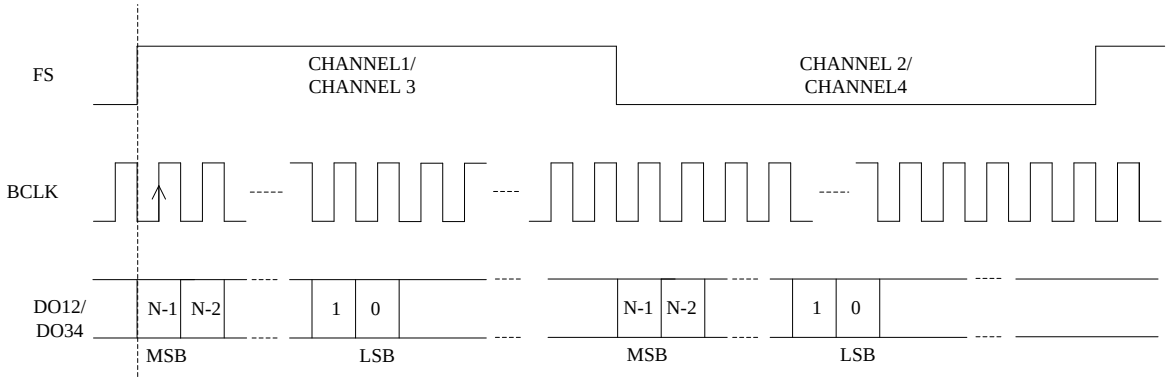



Figure 20: Left Justified Audio Format

## 5.3 I2S Audio Data Mode

In I2S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, left channel data is transmitted and when FS is HIGH, right channel data is transmitted. This is shown in the figure below.

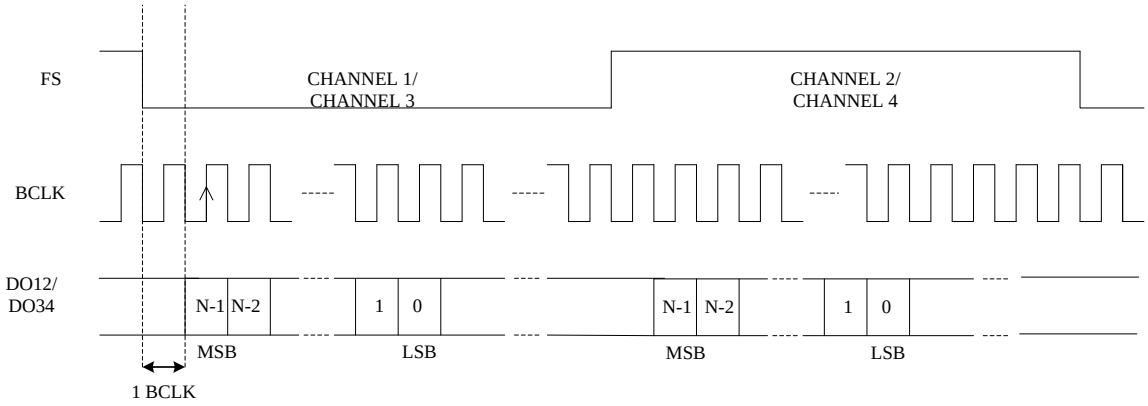



Figure 21: I2S Audio Format

## 5.4 PCM A Audio Data

In the PCM A mode, left channel data is transmitted first followed immediately by right channel data. The left channel MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the right channel MSB is clocked on the next SCLK after the left channel LSB. This is shown in the figure below.

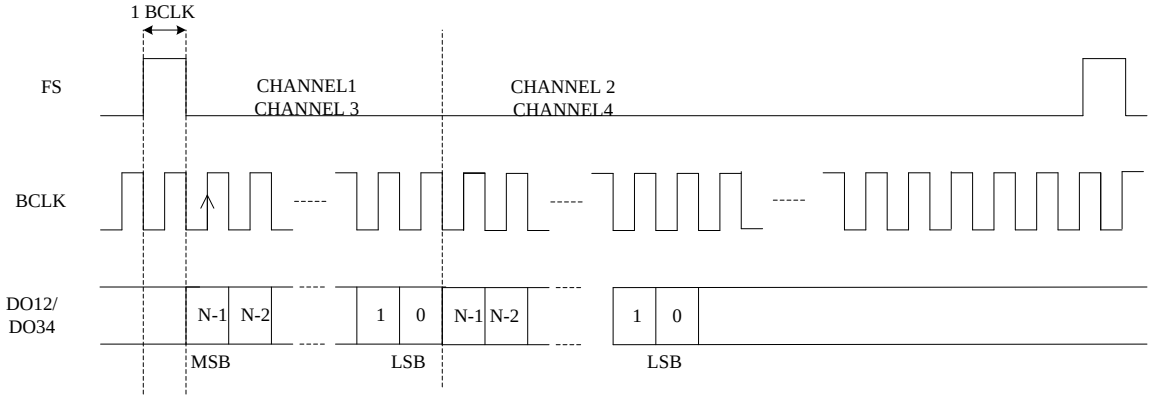



Figure 22: PCM A Audio Format

## 5.5 PCM B Audio Data

In the PCM B mode, left channel data is transmitted first followed immediately by right channel data. The left channel MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and the right channel MSB is clocked on the next SCLK after the left channel LSB. This is shown in the figure below.

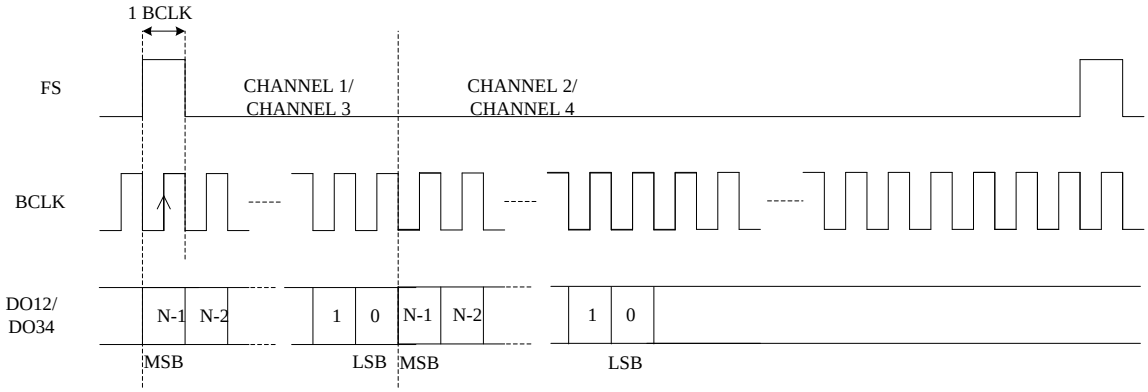



Figure 23: PCM B Audio Format

## 5.6 PCM Time Slot Audio Data

The PCM time slot mode is used to delay the time at ADC data are clocked. This increases the flexibility of the NAU85L40B to be used in a wide range of system designs. One key application of this feature is to enable multiple NAU85L40B or other devices to share the audio data bus, thus enabling more than two channels of audio. This feature may also be used to swap left and right channel data, or to cause both the left and right channels to use the same data.

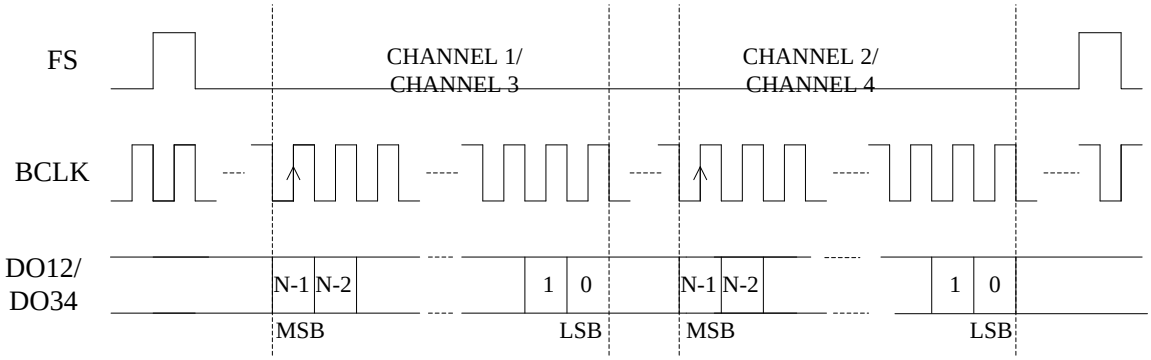



Figure 24: PCM Time Slot Audio Format

Table 7: Digital Audio Interface TDM Modes.

## 5.7 AUDIO INTERFACE TIMING DIAGRAM

I2S timing diagram shows the audio timing diagram among BCLK, FS, DACIN, and ADCOUT. For NAU85L40B.

### 5.7.1 AUDIO INTERFACE IN SLAVE MODE

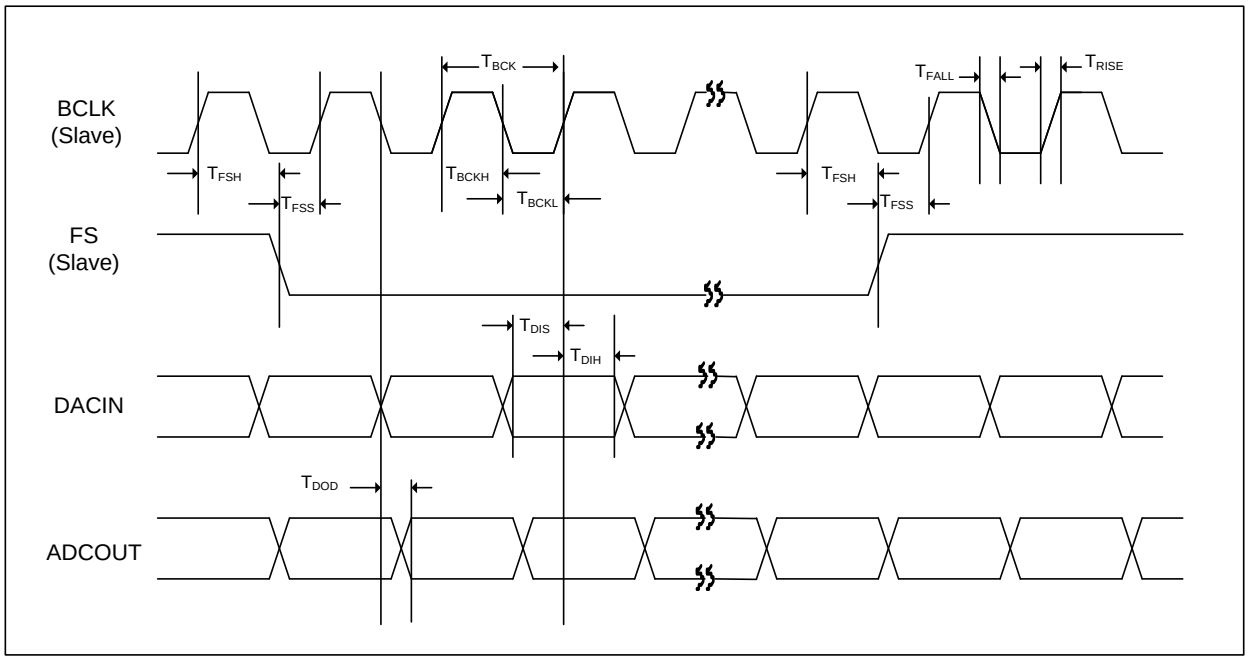



Figure 25:Audio Interface Slave Mode Timing Diagram

### 5.7.2 AUDIO INTERFACE IN MASTER MODE

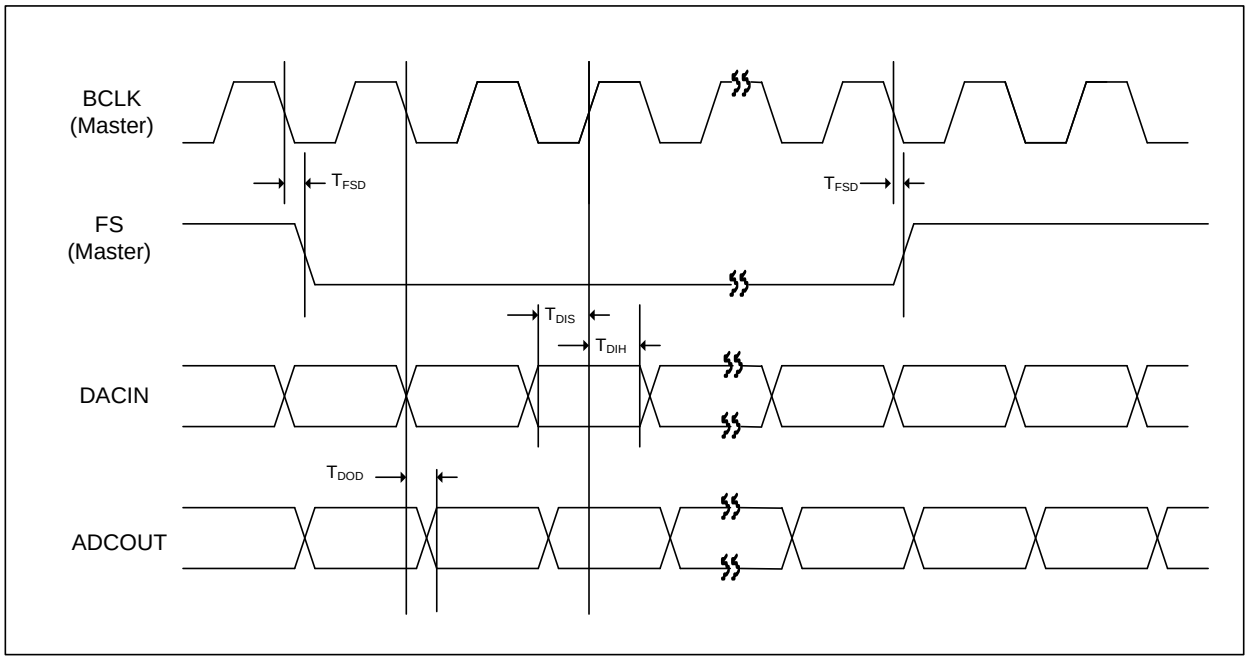



Figure 25: Audio Interface in Master Mode Timing Diagram

### 5.7.3 PCM AUDIO INTERFACE IN SLAVE MODE (PCM Audo Data)

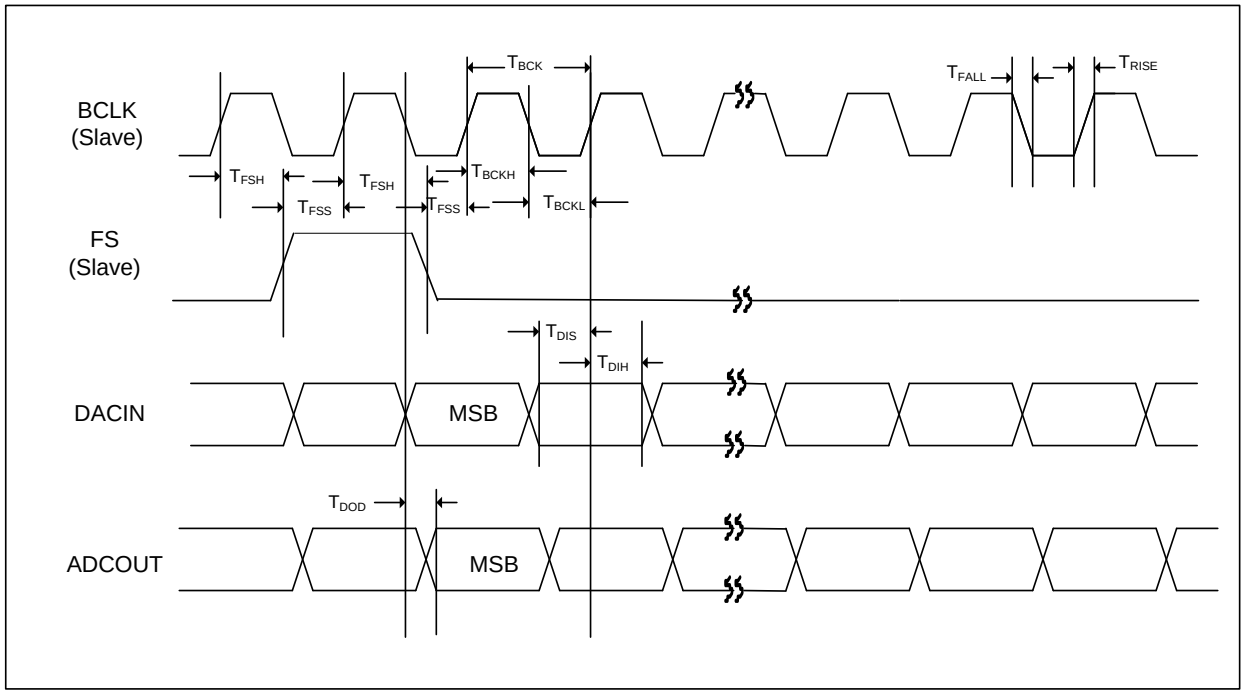



Figure 26:PCM Audio Interface Slave Mode Timing Diagram

### 5.7.4 PCM AUDIO INTERFACE IN MASTER MODE

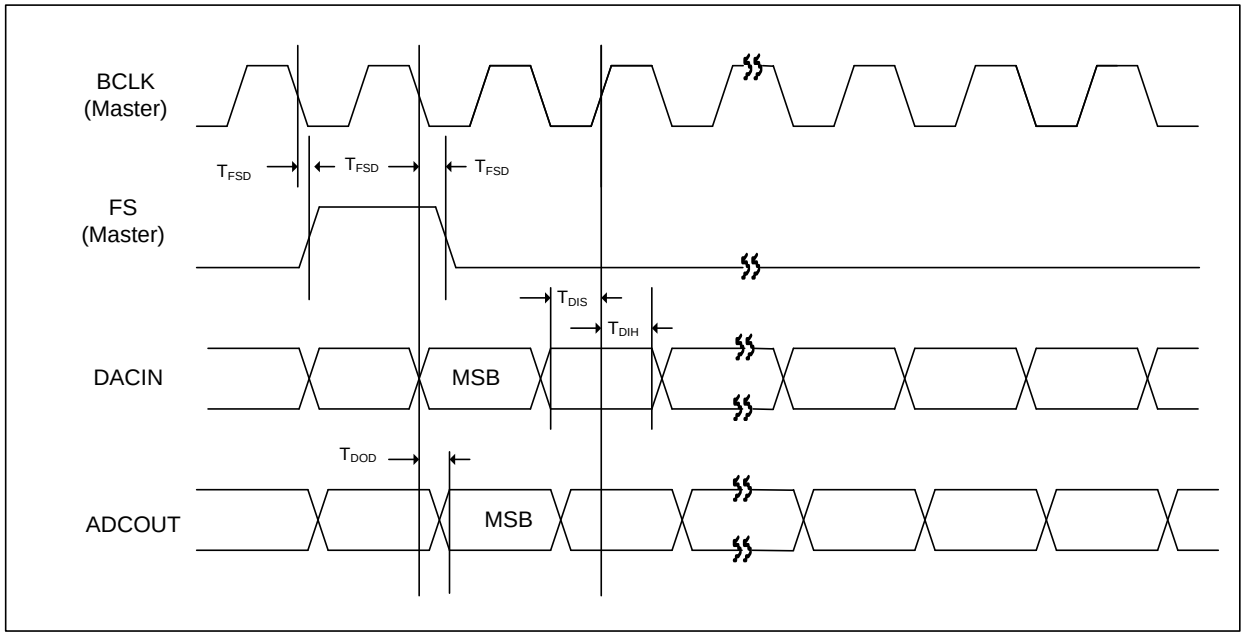



Figure 28:PCM AUDIO Interface Master Mode Timing Diagram

### 5.7.5 PCM AUDIO INTERFACE IN SLAVE MODE (PCM Time Slot Mode)

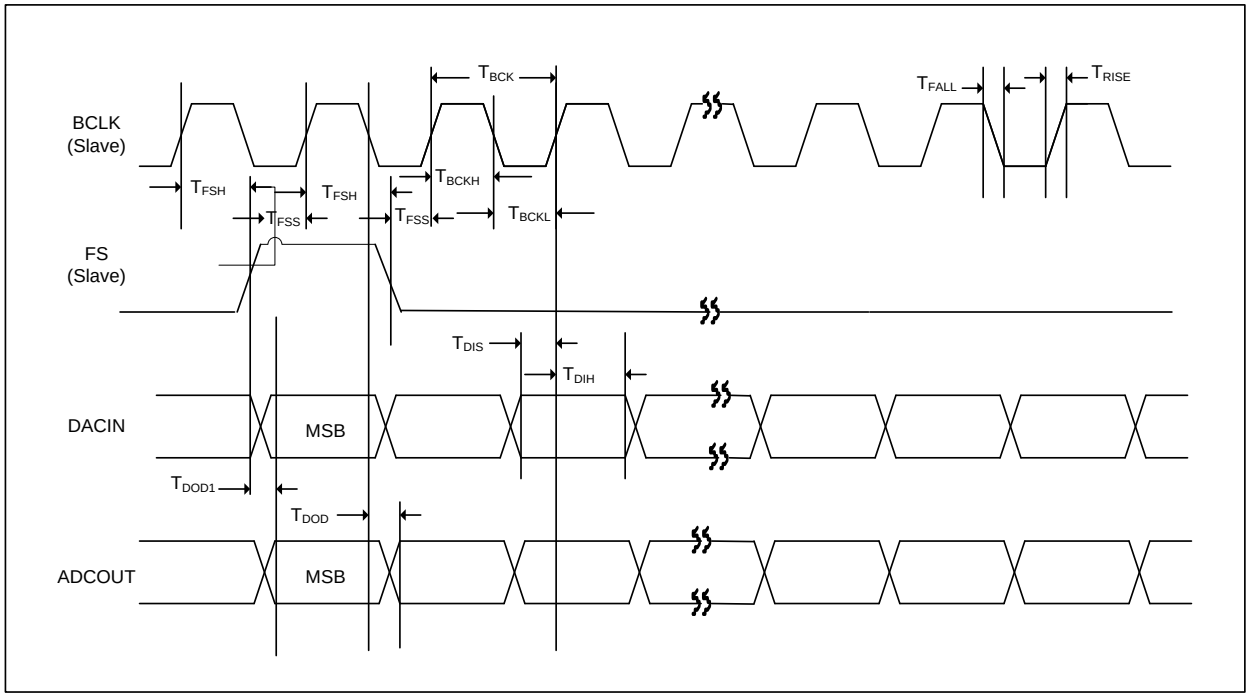



Figure 29:PCM Audio Interface Slave Mode (PCM Time Slot Mode)

### 5.7.6 PCM AUDIO INTERFACE IN MASTER MODE (PCM Time Slot Mode)

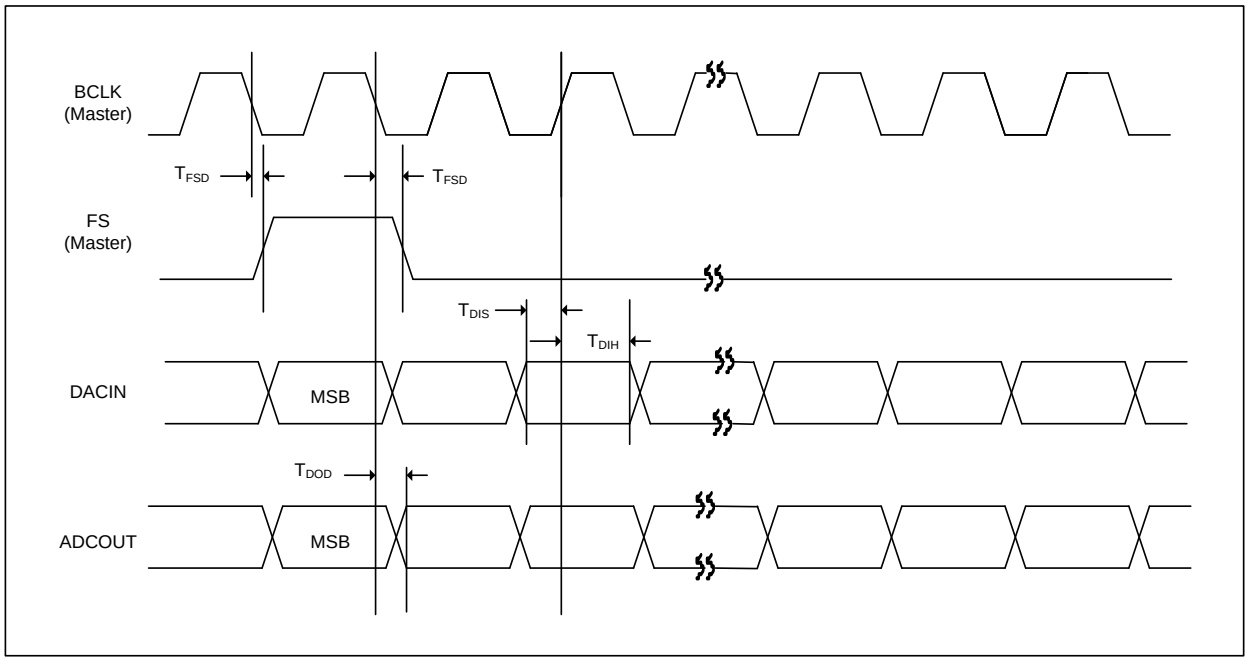



Figure 27:PCM Audio Interface Master Mode (PCM Time Slot Mode )Timing Diagram

### 5.7.7 AUDIO Timing Parameter

Parameters are under Fs=24KHz and word length 24bits, VDDA=VDDB=VDDC=1.8V and VDDMIC=4.2V at 27°C

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{BCK}$ | BCLK Cycle Time (Slave Mode) | 50 | --- | --- | ns |
| $T_{BCKH}$ | BCLK High Pulse Width (Slave Mode) | 20 | --- | --- | ns |
| $T_{BCKL}$ | BCLK Low Pulse Width (Slave Mode) | 20 | --- | --- | ns |
| $T_{FSS}$ | Fs to CLK Rising Edge Setup Time (Slave Mode) | 20 | --- | --- | ns |
| $T_{FSH}$ | BCLK Rising Edge to Fs Hold Time (Slave Mode) | 20 | --- | --- | ns |
| $T_{FSD}$ | Fs to SCK falling to Fs transition (Master Mode) | --- | --- | TBD | ns |
| $T_{RISE}$ | Rise Time for All Audio Interface Signals | --- | --- | TBD | ns |
| $T_{FALL}$ | Fall Time for All Audio Interface Signals | --- | --- | TBD | ns |
| $T_{DIS}$ | ADCIN to BCLK Rising Edge Setup Time | 15 | --- | --- | ns |
| $T_{DOD}$ | Delay Time from SCLK falling Edge to ADCOUT | --- | 45/27* | 70/42* | ns |

Table 8:AUDIO Interface Timing Parameters

* Fs=24KHz, word length 24bits, VDDA =VDDC=1.8V, VDDB=3.3, and VDDMIC=4.2V at 27°C

## 5.8 TDM Right Justified Audio Data

In right justified mode, the LSB is clocked on the last BCLK rising edge before FS transitions. When FS is HIGH, channel 1 then channel 3 data is transmitted and when FS is LOW, channel 2 then channel 4 data is transmitted. This is shown in the figure below.

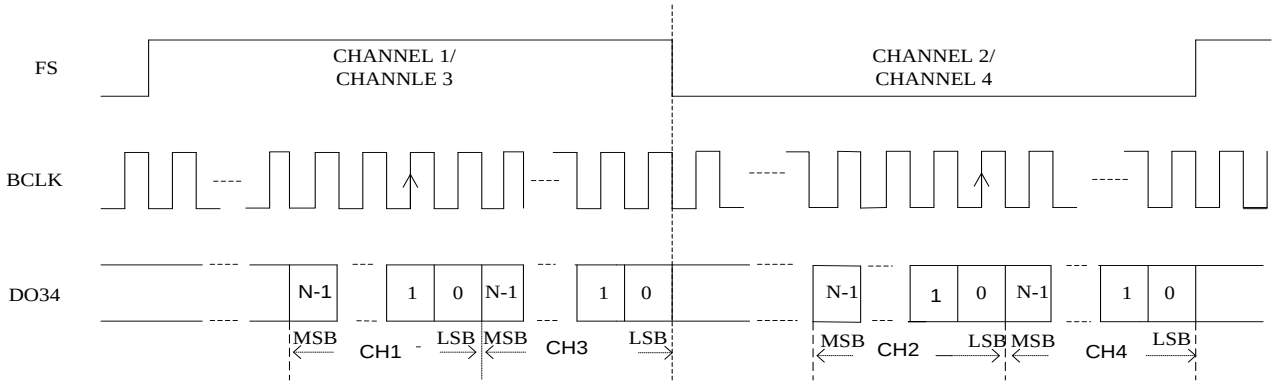



Figure 31: TDM Right Justified Audio Format

## 5.9 TDM Left Justified Audio Data

In left justified mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, channel 1 then channel 3 data is transmitted and when FS is LOW, channel 2 then channel 4 channel data is transmitted. This is shown in the figure below.

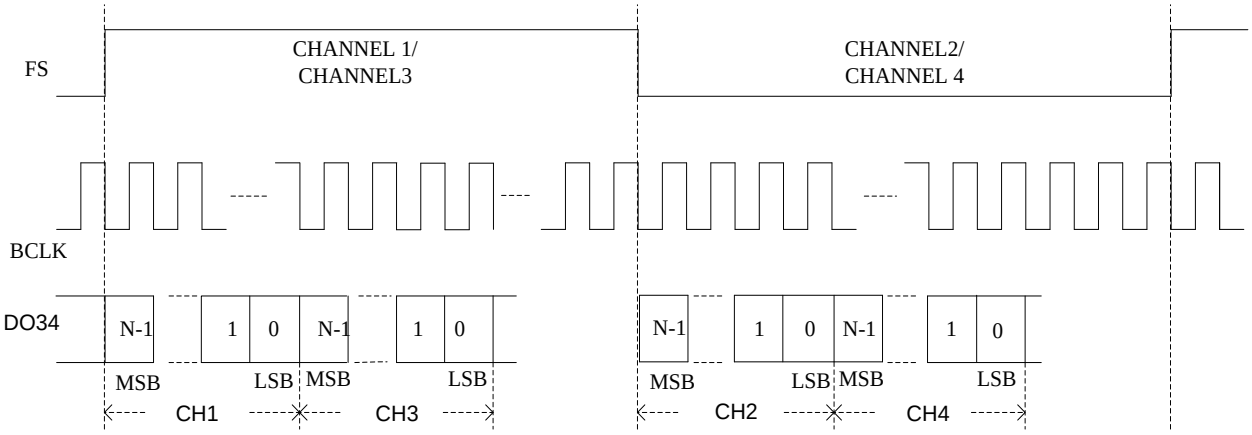



Figure 32: TDM Left Justified Audio Format

## 5.10 TDM I2S Audio Data

In I2S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, channel 1 then channel 3 channel data is transmitted and when FS is HIGH, channel 2 then channel 4 channel data is transmitted. This is shown in the figure below.

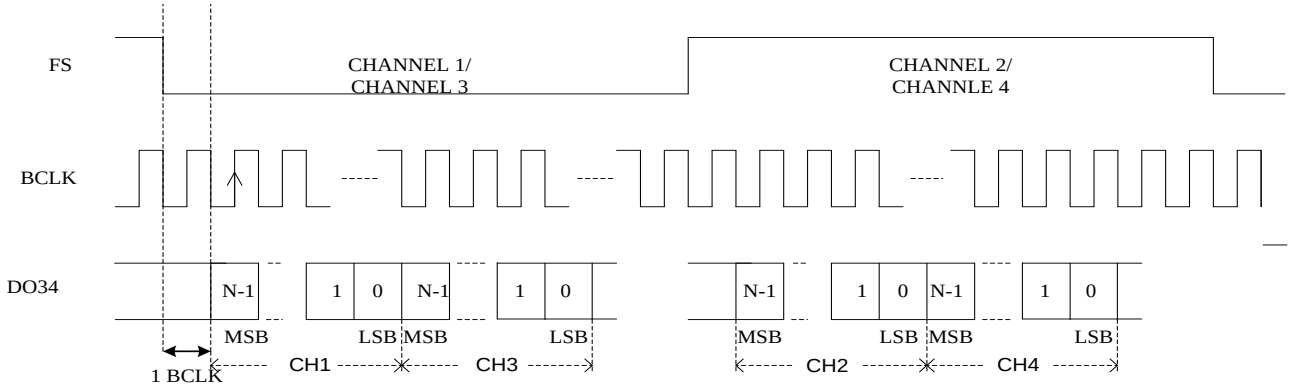



Figure 33: TDM I2S Audio Format

## 5.11 TDM PCM A Audio Data

In the PCM A mode, channel 1 data is transmitted first followed sequentially by channel 2, 3, and 4 immediately after. The channel 1 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in the figure below.

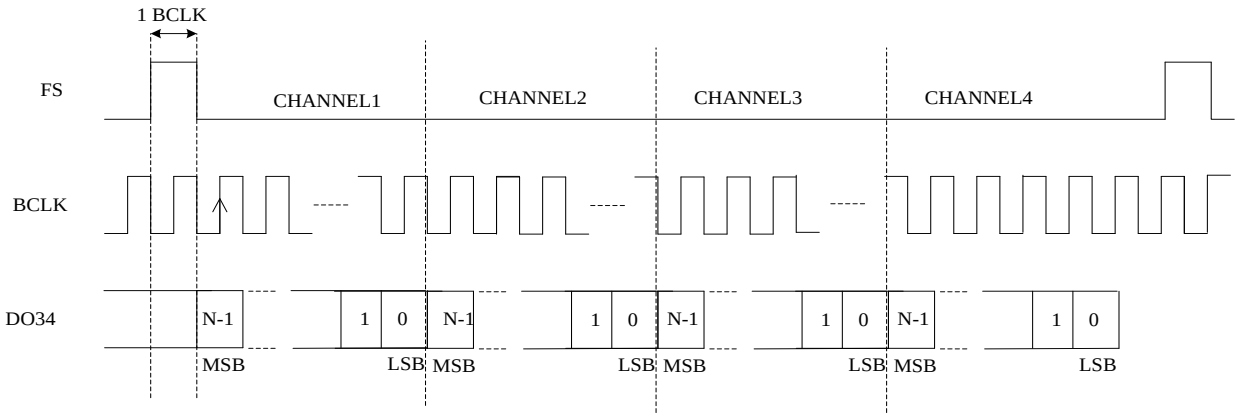



Figure 34: TDM PCM A Audio Format

## 5.12 TDM PCM B Audio Data

In the PCM B mode, channel 1 data is transmitted first followed sequentially by channel 2, 3, and 4 immediately after. The channel 1 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in the figure below.

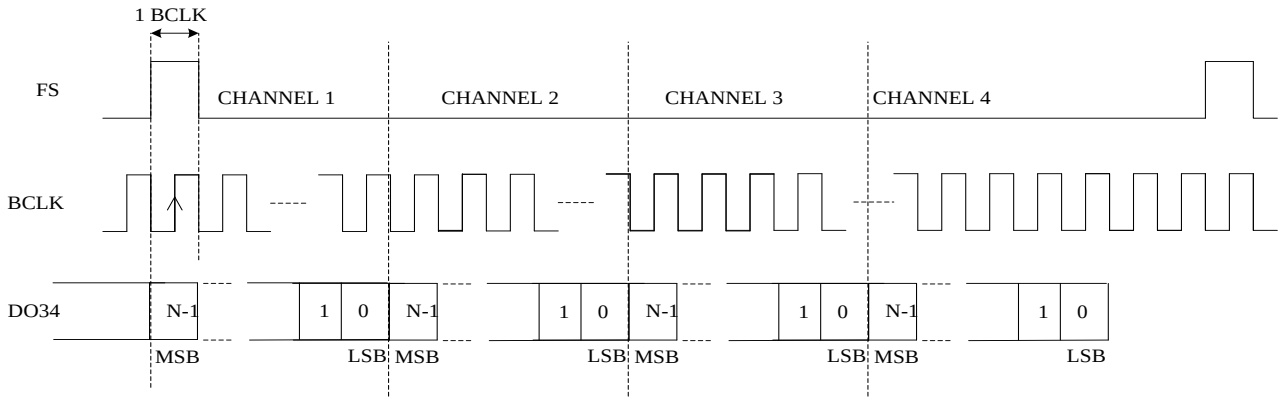



Figure 35: TDM PCM B Audio Format

## 5.13 TDM PCM Offset Audio Data

The PCM offset mode is used to delay the time at which the ADC data is clocked. This increases the flexibility of the NAU85L40B to be used in a wide range of system designs. One key application of this feature is to enable multiple NAU85L40B or other devices to share the audio data bus, thus enabling more than four channels of audio. This feature may also be used to swap channel data, or to cause multiple channels to use the same data.

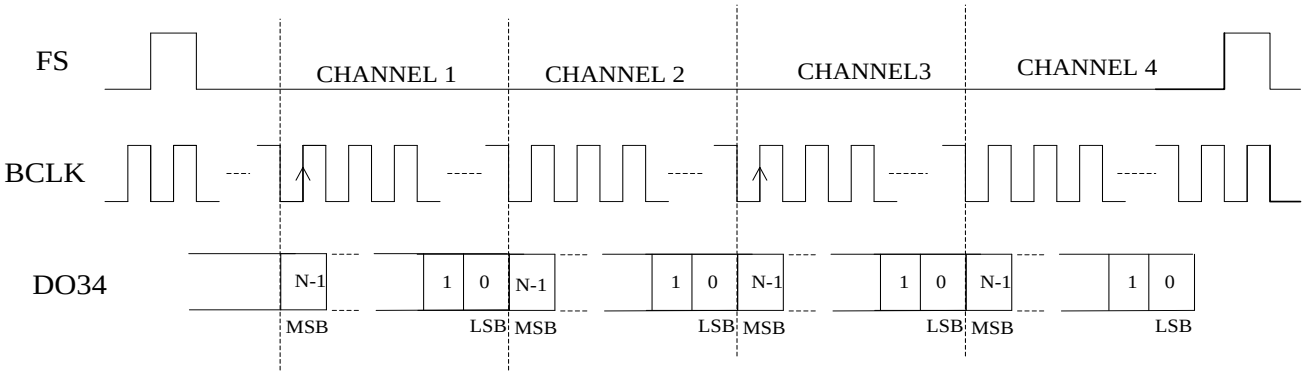



Figure 36: TDM PCM Offset Audio Format

# 6 Typical Application Diagram

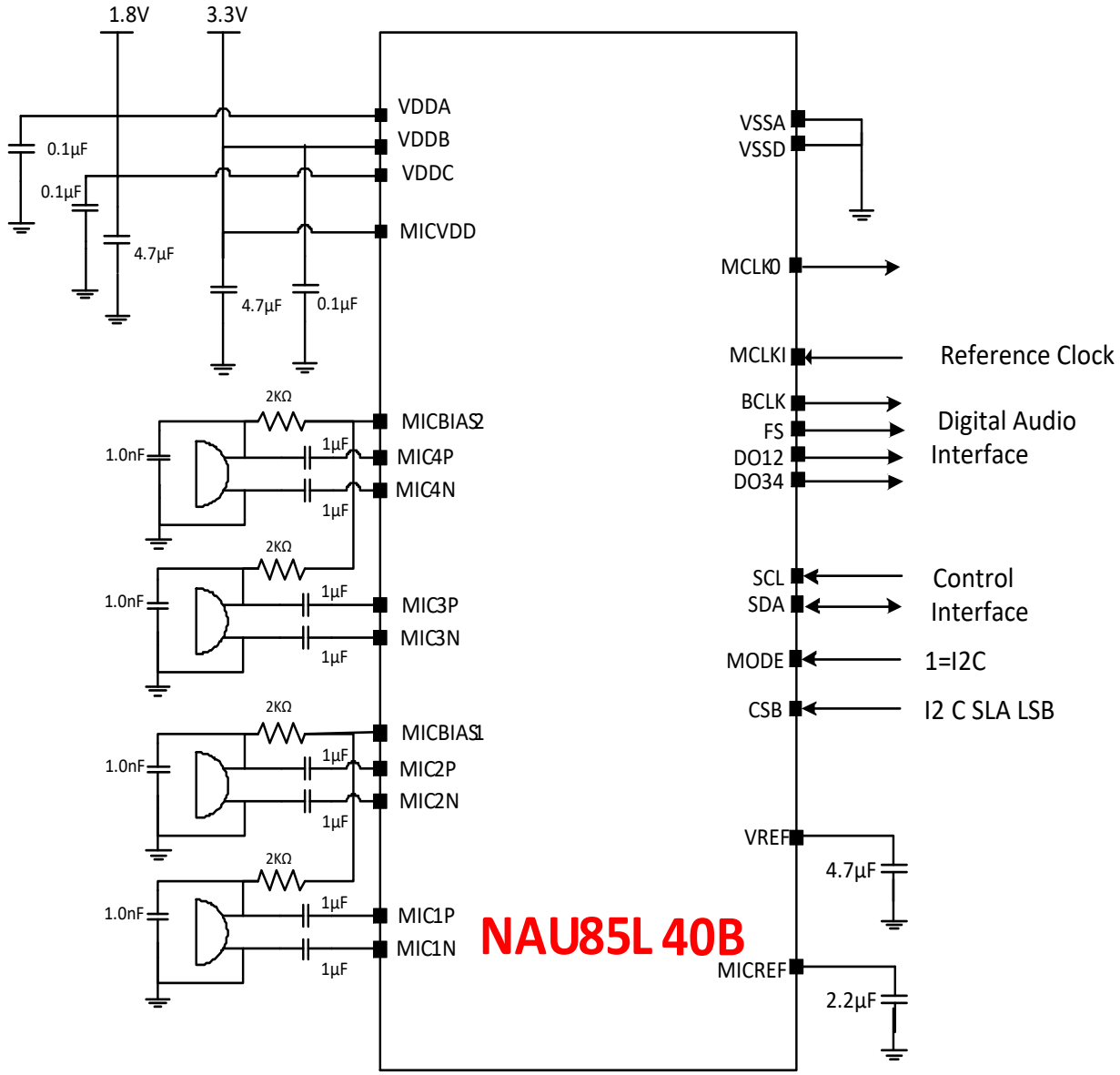



Figure 28: Typical Single-ended use Application Diagram

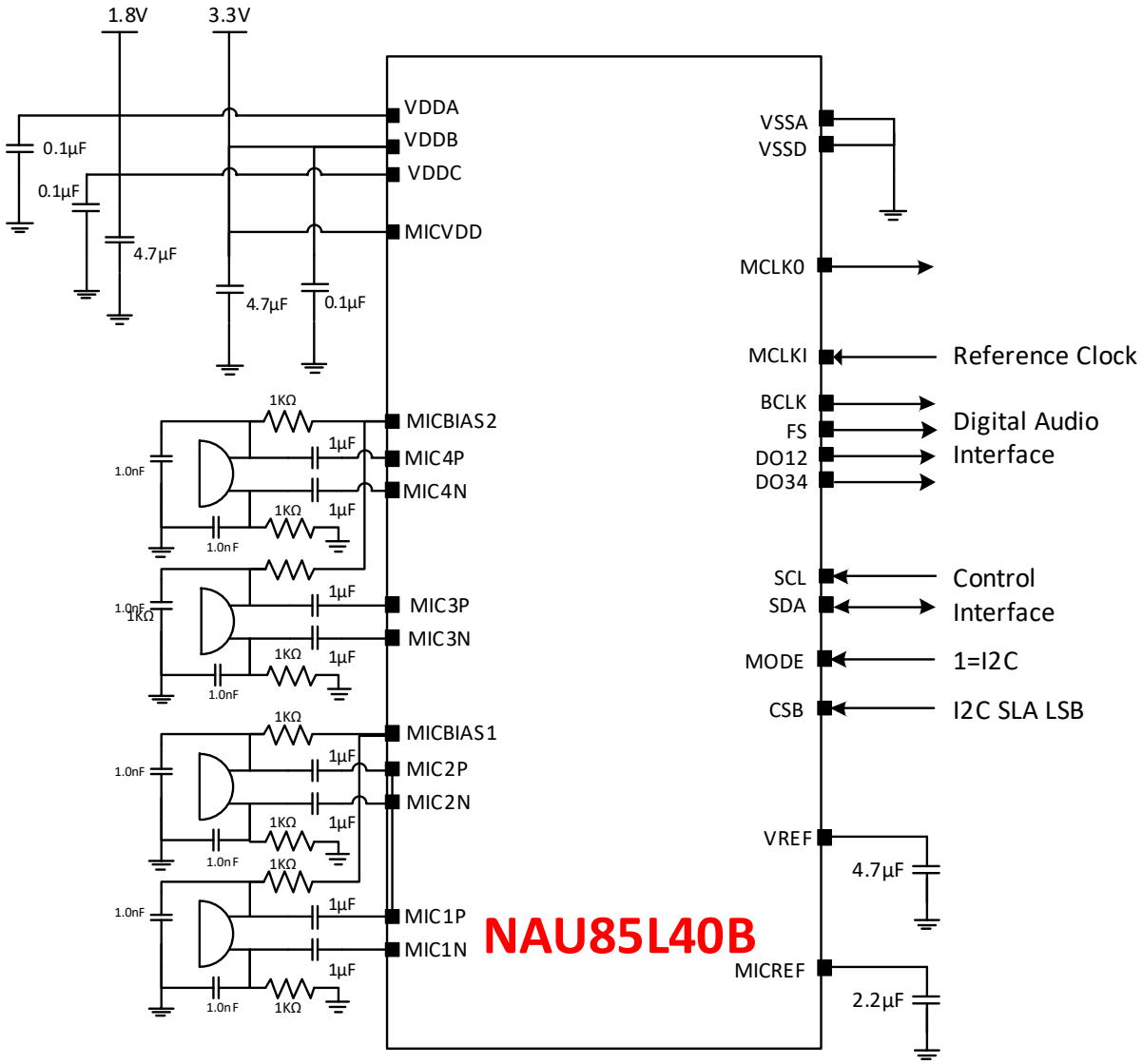
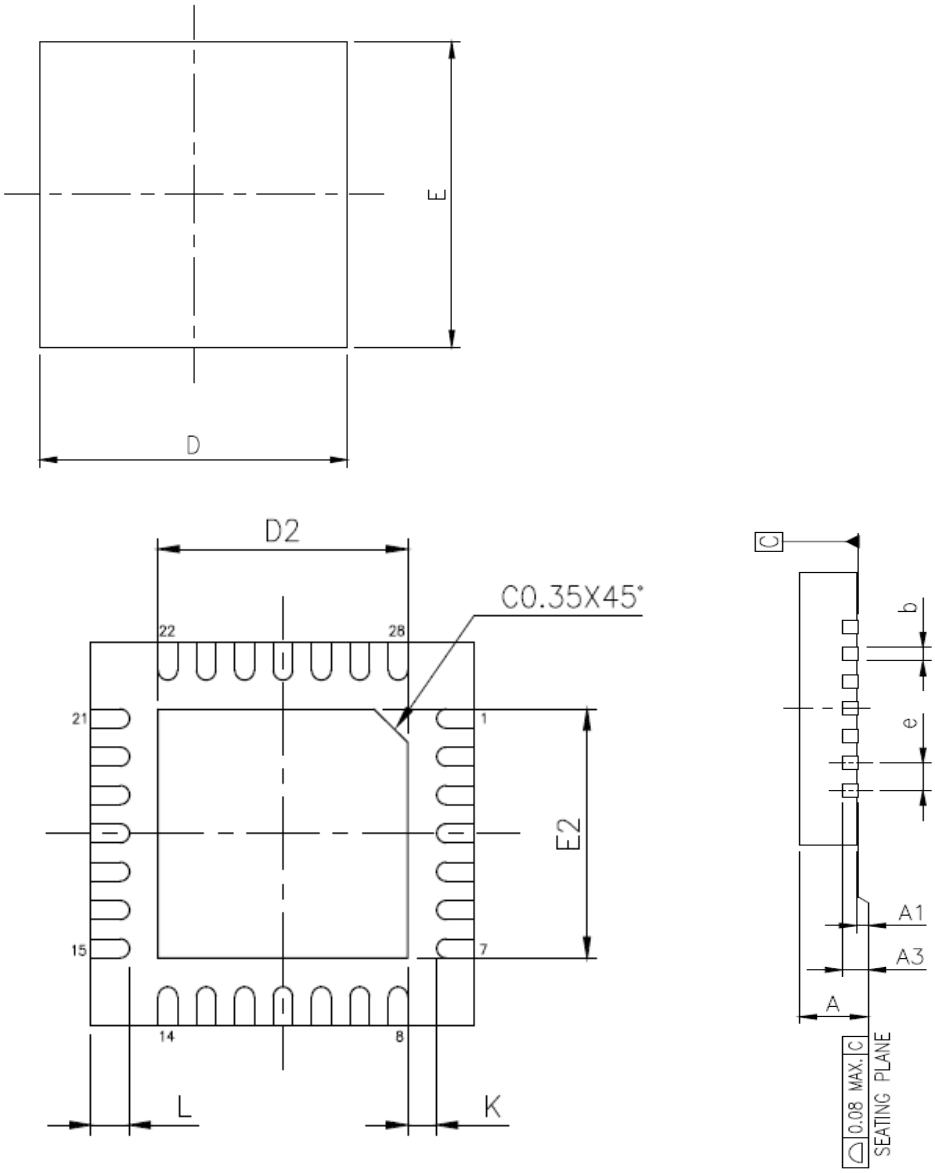



Figure 29: Typical Application Schematic for Differential Microphone Connection

# 7 Package Information

**QFN 28L 4X4 mm$^2$,Thickness:0.8 mm(Max), Pitch:0.40 mm EP SIZE 2.6X2.6 mm**



| PKG CODE | QFN 28L | | |
|---|---|---|---|
| SYMBOLS | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.203 REF. | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 4.00 BSC | | |
| E | 4.00 BSC | | |
| e | 0.40 BSC | | |
| K | 0.20 | — | — |
| D2 | 2.55 | 2.60 | 2.65 |
| E2 | 2.55 | 2.60 | 2.65 |
| L | 0.30 | 0.40 | 0.50 |

## 9.1 Version History

| VERSION | DATE | PAGE/ CHAP. | DESCRIPTION |
|---|---|---|---|
| 0.1 | 16 May 2014 | - | Initial Draft Release |
| 0.2 | | | Expand Clocking description<br>Expand register descriptions |
| 0.3 | 4 June 2014 | | MCLK_SRC register changed/expanded |
| 0.4 | June 30, 2014 | | Analog supply voltage updated<br>TDM Mode descriptions fixed<br>Expand register descriptions and lookup table |
| 1.0 | November, 05,2014 | | Updated AC/DC parameters |
| 1.1 | June 6, 2016 | **22**<br>**37 38**<br>**20**<br>**39**<br>**34**<br>**23,24** | Table 7, Figure 10 Corrected<br>Fig.9 changed<br>Added Note<br>Fig 11, FLL equation 1 &example change |
| 1.2 | February 16, 2017 | **18**<br>**40**<br>**32-35** | Sec 3.1 description error<br>Adding 6.7 audio Interface timing diagram |
| 1.3 | April 4, 2017 | **5** | Change to revision B, updated THD and SNR values<br>Changed pin “Mode” description |
| | | | |

# 8 ORDERING INFORMATION

Nuvoton Part Number Description