MT90826

Quad Digital Switch

Data Sheet

January 2006

Features

- 4,096 × 4,096 channel non-blocking switching at 8.192 or 16.384 Mbps
- Per-channel variable or constant throughput delay
- Accepts 32 ST-BUS streams of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps
- Split Rate mode provides a rate conversion option to convert data from one rate to another rate
- Automatic frame offset delay measurement for ST-BUS input streams
- Per-stream input delay programming
- Per-stream output advancement programming
- Per-channel high impedance output control
- Bit Error Monitoring on selected ST-BUS input and output channels.
- Per-channel message mode
- Connection memory block programming
- IEEE-1149.1 (JTAG) Test Port
- 3.3 V local I/O with 5 V tolerant inputs and TTL compatible outputs

Ordering Information

MT90826AL	160 Pin MQFP	Trays
MT90826AG	160 Ball PBGA	Trays
MT90826AV	144 Ball LBGA	Trays
MT90826AL1	160 Pin MQFP*	Trays
MT90826AG2	160 Ball PBGA**	Trays

*Pb Free Matte Tin

**Pb Free Tin/Silver/Copper

-40°C to +85°C

Applications

- Medium switching platforms
- CTI application
- Voice/data multiplexer
- Digital cross connects
- WAN access system
- Wireless base stations

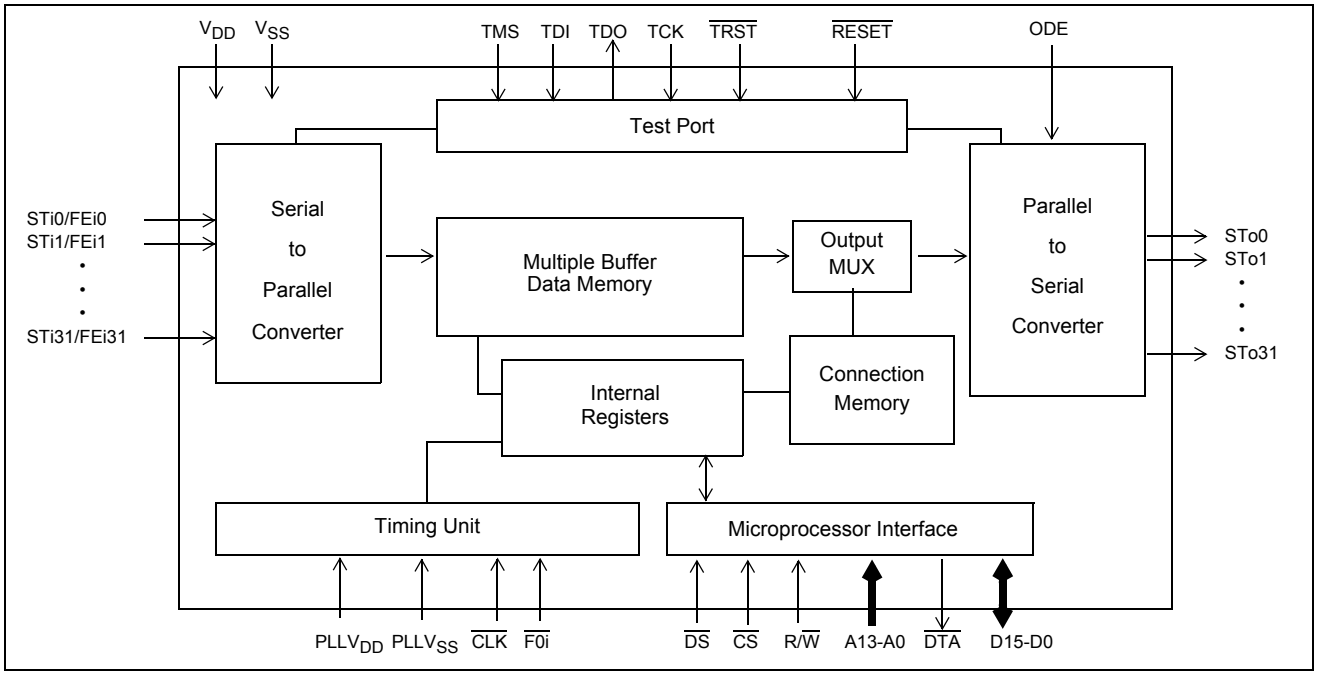

Figure 1 - Functional Block Diagram

Description

The MT90826 Quad Digital Switch has a non-blocking switch capacity of 4,096 x 4,096 channels at a serial bit rate of 8.192 Mbps or 16.384 Mbps, 2,048 x 2,048 channels at 4.096 Mbps and 1024 x 1024 channels at 2.048 Mbps. The device has many features that are programmable on a per stream or per channel basis, including message mode, input offset delay and high impedance output control.

The per stream input and output delay control is particularly useful for managing large multi-chip switches with a distributed backplane.

Operating in Split Rate mode allows rate conversion for switching between two groups of bit rate streams.

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Changes Summary

The following table captures the changes from the April 2005 issue.

Page	Item	Change
26	Figure 6 “Examples for Input Offset Delay Timing”	Clarified the mid-point sampling of the 16 Mbps input data.
30	Section 9.0 Initialization of the MT90826	Added the 600 µs waiting time needed for the APLL module to be stabilized before starting the next microprocessor port access cycle.
37	AC Electrical Characteristics - Serial Streams for ST-BUS.	Clarified the 16, 8, 4 and 2 Mbps Input Data Sampling timing.
37	Figure 8 “ST-BUS Timing for Stream rate of 16.384 Mbps”	Clarified the input data sampling position at 16 Mbps data rate.
38	Figure 9 “ST-BUS Timing for Stream rate of 8.192 Mbps when CLK = 16.384 MHz”	Added the input data sampling position at 8 Mbps data rate.
38	Figure 10 “ST-BUS Timing for Stream rate of 4.096 Mbps when CLK = 16.384 MHz”	Added the input data sampling position at 4 Mbps data rate.
39	Figure 12 “ST-BUS Timing for Stream rate of 2.048 Mbps when CLK = 16.384 MHz”	Added the input data sampling position at 2 Mbps data rate.

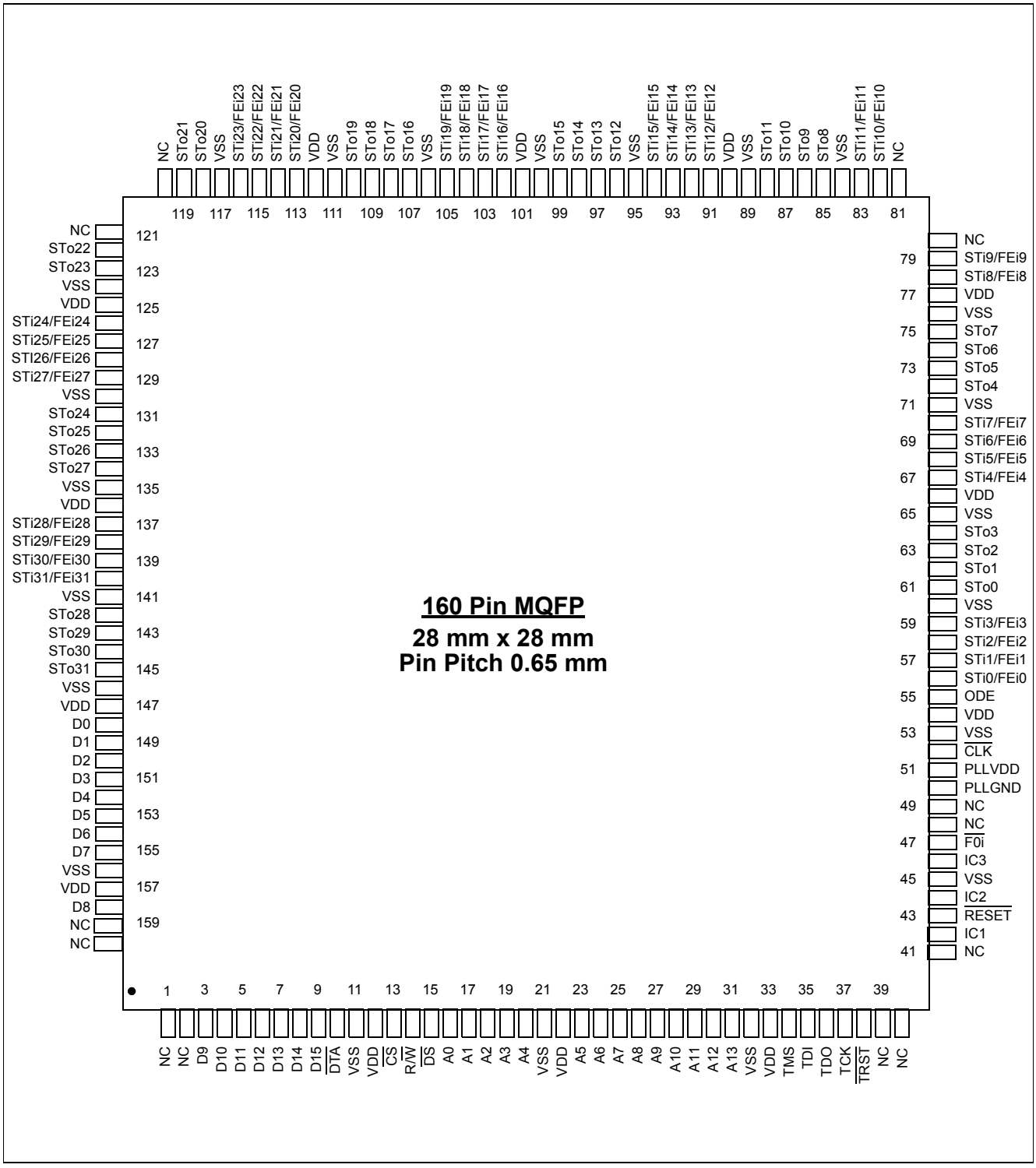


Figure 2 - 160-Pin MQFP Pin Connections

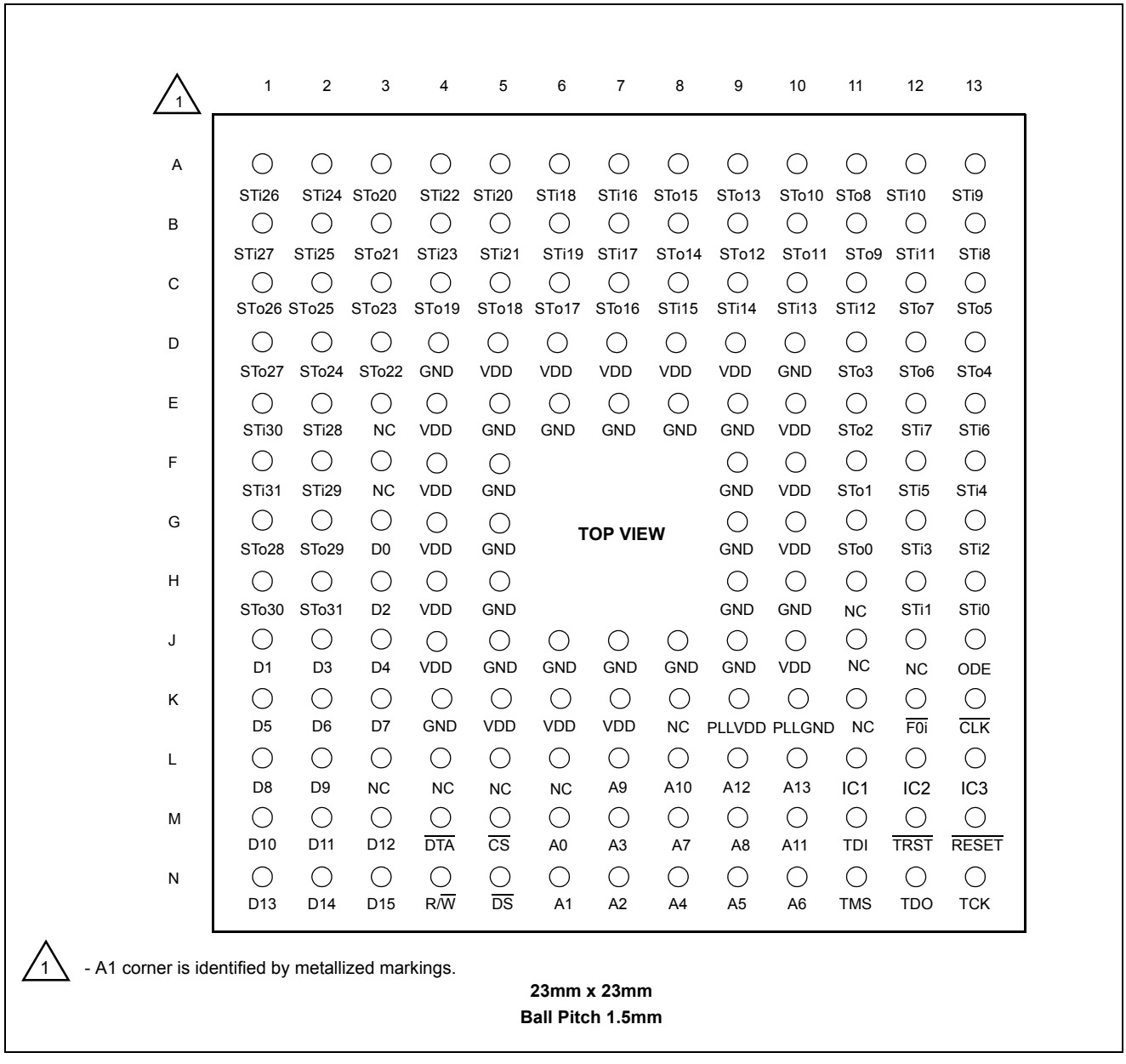


Figure 3 - 160 Ball PBGA Pin Connections

PINOUT DIAGRAM: (as viewed through top of package)

A1 corner identified by metallized marking, mould indent, ink dot or right-angled corner

	1	2	3	4	5	6	7	8	9	10	11	12
A	STo23	STo20	STi21	STi20	STi17	STi16	STo14	STo13	STo11	STo9	STi11	STi9
B	STo22	STo21	STi23	STi22	STi19	STi18	STo15	STo12	STo10	STo8	STI10	STi8
C	STi26	STi25	STo24	STo19	STo18	STo17	STo16	STi14	STi13	STi12	STo7	STo5
D	STi27	STi24	STo25	GND	VDD	VDD	VDD	STi15	GND	STo2	STo6	STo4
E	STi29	STi28	STo27	STo26	GND	GND	GND	GND	VDD	STo3	STi7	STi6
F	STi30	STi31	STo28	VDD	GND	GND	GND	GND	VDD	STo1	STi4	STi5
G	STo30	STo31	STo29	VDD	GND	GND	GND	GND	PLLVDD	STo0	STi3	STi2
H	D1	D2	D0	VDD	GND	GND	GND	GND	PLLGND	ODE	STi0	STi1
J	D3	D7	D4	GND	$\overline{DS}$	VDD	VDD	VDD	NC	NC	$\overline{FOi}$	$\overline{CLK}$
K	D5	D15	D11	D13	$\overline{CS}$	A2	A5	A8	A9	$\overline{RESET}$	IC1	IC3
L	D6	D8	D9	R/$\overline{W}$	A13	A1	A4	A10	A12	TCK	TDO	IC2
M	D10	D12	D14	$\overline{DTA}$	A0	A3	A6	A7	A11	TMS	TDI	$\overline{TRST}$

Figure 4 - 144 Ball LBGA Pin Connections

Pin Description

Pin # MQFP	Pin # PBGA	Pin # LBGA	Name	Description
12,22,33,54, 66,77,90,101, 112,125,136, 147,157	D5,D6,D7,D8,D9, E4,E10,F4, F10,G4,G10, H4,J4,J10,K5, K6,K7	D5,D6,D7,E9, F4,F9,G4,H4, J6,J7,J8	V_{DD}	**+3.3 Volt Power Supply.**
11,21,32,45, 53,60,65,71, 76,84,89,95, 100,106,111, 117,124,130, 135,141,146, 156	D4,D10,E5,E6, E7,E8,E9,F5, F9,G5,G9,H5, H9,H10,J5,J6, J7,J8,J9,K4	D4,D9,E5,E6, E7,E8,F5,F6, F7,F8,G5,G6, G7,G8,H5,H6, H7,H8,J4	V_{ss}	**Ground.**
34	N11	M10	TMS	**Test Mode Select (3.3 V Input with Internal pull-up).** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up when not driven.
35	M11	M11	TDI	**Test Serial Data In (3.3 V Input with Internal pull-up).** JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up when not driven.
36	N12	L11	TDO	**Test Serial Data Out (3.3 V Output).** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG scan is not enabled.
37	N13	L10	TCK	**Test Clock (5 V Tolerant Input).** Provides the clock to the JTAG test logic.
38	M12	M12	$\overline{\text{TRST}}$	**Test Reset (3.3 V Input with internal pull-up).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin is pulled by an internal pull-up when not driven. This pin should be pulsed low on power-up, or held low, to ensure that the device is in the normal functional mode.
42	L11	K11	IC1	**Internal Connection 1 (3.3 V Input with internal pull-down).** Connect to V_{SS} for normal operation.
43	M13	K10	$\overline{\text{RESET}}$	**Device Reset (5 V Tolerant Input).** This input (active LOW) puts the device in its reset state which clears the device internal counters and registers.

Pin Description (continued)

Pin # MQFP	Pin # PBGA	Pin # LBGA	Name	Description
44	L12	L12	IC2	**Internal Connection 2 (3.3 V Input with internal pull-down).** Connect to V_{SS} for normal operation.
46	L13	K12	IC3	**Internal Connection 3 (3.3 V Input with internal pull-down).** Connect to V_{SS} for normal operation.
47	K12	J11	$\overline{F0i}$	**Master Frame Pulse (5 V Tolerant Input).** This input accepts a 122 ns or 60 ns wide negative frame pulse. The CPLL bit in the control register determines the usage of the frame pulse width. See Table 6 for details.
50	K10	H9	PLLGND	**Phase Lock Loop Ground.**
51	K9	G9	PLLVDD	**Phase Lock Loop Power Supply. 3.3 V**
52	K13	J12	$\overline{CLK}$	**Master Clock (5 V Tolerant Input).** Serial clock for shifting data in/out on the serial streams. This pin accepts a clock frequency of 8.192 MHz or 16.384 MHz. The CPLL bit in the control register determines the usage of the clock frequency. See Table 6 for details.
55	J13	H10	ODE	**Output Drive Enable (5 V Tolerant Input).** This is the output-enable control pin for the STo0 to STo31 serial outputs. See Table 2 for details.
56 57 58 59 67-70 78,79 82,83 91-94 102-105 113-116 126-129 137-140	H13 H12 G13 G12 F13,F12,E13,E12 B13,A13 A12,B12 C11,C10,C9,C8 A7,B7,A6,B6 A5,B5,A4,B4 A2,B2,A1,B1 E2,F2,E1,F1	H11 H12 G12 G11 F11,F12,E12,E11 B12,A12 B11,A11 C10,C9,C8,D8 A6,A5,B6,B5, A4,A3,B4,B3 D2,C2,C1,D1 E2,E1,F1,F2	STi0/FEi0, STi1/FEi1 STi2/FEi2 STi3/FEi3 STi4-7/FEi4-7 STi8-9/FEi8-9 STi10-11/FEi10-11 STi12-15/FEi12-15 STi16-19/FEi16-19 STi20-23/FEi20-23 STi24-27/FEi24-27 STi28-31/FEi28-31	**Serial Input Streams 0 to 31 and Frame Evaluation Inputs 0 to 31 (5 V Tolerant Inputs).** Serial data input streams. These streams may have data rates of 2.048, 4.096, 8.192 or 16.384 Mbps, depending upon the value programmed at bits DR0 - DR2 in the control register. In the frame evaluation mode, they are used as the frame evaluation inputs.
61-64 72-75 85-88 96-99 107-110 118,119 122,123 131-134 142-145	G11,F11,E11,D11 D13,C13,D12,C12 A11,B11,A10,B10 B9,A9,B8,A8 C7,C6,C5,C4 A3,B3 D3,C3 D2,C2,C1,D1 G1,G2,H1,H2	G10,F10,D10,E10 D12,C12,D11,C11 B10,A10,B9,A9 B8,A8,A7,B7 C7,C6,C5,C4 A2,B2 B1,A1 C3,D3,E4,E3 F3,G3,G1,G2	STo0 - 3 STo4 - 7 STo8 - 11 STo12 - 15 STo16 - 19 STo20, STo21 STo22, STo23 STo24 - 27 STo28 - 31	**ST-BUS Output 0 to 31 (Three-state Outputs).** Serial data output streams. These streams may have data rates of 2.048, 4.096, 8.192, or 16.384 Mbps, depending upon the value programmed at bits DR0 - DR2 in the control register.

Pin Description (continued)

Pin # MQFP	Pin # PBGA	Pin # LBGA	Name	Description
148 - 153 154,155 158 3 - 7 8,9	G3,J1,H3,J2,J3,K1, K2,K3 L1 L2,M1,M2,M3,N1, N2,N3	H3,H1,H2,J1,J3,K1 L1,J2 L2 L3,M1,K3,M2,K4 M3,K2	D0 - 5, D6, D7 D8 D9 - 13 D14, D15	**Data Bus 0 to 15 (5 V Tolerant I/O).** These pins form the 16-bit data bus of the microprocessor port.
10	M4	M4	$\overline{DTA}$	**Data Transfer Acknowledgment (Three-state Output).** This output pulses low from tristate to indicate that a databus transfer is complete. A pull-up resistor is required to hold a HIGH level when the pin is tristated.
15	N5	J5	$\overline{DS}$	**Data Strobe (5 V Tolerant Input).** This active low input works in conjunction with $\overline{CS}$ to enable the read and write operations.
14	N4	L4	R/$\overline{W}$	**Read/$\overline{Write}$ (5 V Tolerant Input).** This input controls the direction of the data bus lines (D0-D15) during a microprocessor access.
13	M5	K5	$\overline{CS}$	**Chip Select (5 V Tolerant Input).** Active low input used by a microprocessor to activate the microprocessor port.
16 - 20 23 - 31	M6,N6,N7,M7,N8 N9,N10,M8,M9,L7 L8,M10,L9,L10	M5,L6,K6,M6,L7, K7,M7,M8,K8,K9, L8,M9,L9,L5	A0 - A4 A5 - A13	**Address 0 to 13 (5 V Tolerant Input).** These lines provide the A0 - A13 address lines when accessing the internal registers or memories.
1,2,39,40,41,48, 49,80,81,120, 121,159,160	E3,F3,H11,J11, J12,K8,K11, L3,L4,L5,L6.	J9,J10	NC	**No Connect.** These pins have to be left unconnected.

1.0 Device Overview

The MT90826 Quad Digital Switch is capable of switching up to 4,096 × 4,096 channels. The MT90826 is designed to switch 64 Kbps PCM or N x 64 Kbps data. The device maintains frame integrity in data applications and minimum throughput delay for voice applications on a per channel basis.

The serial input streams of the MT90826 can have a bit rate of 2.048, 4.096, 8.192 or 16.384 Mbps and are arranged in 125 µs wide frames, which contain 32, 64,128 or 256 channels, respectively. The data rates on input and output streams match. All inputs and outputs may be programmed to 2.048, 4.096 or 8.192 Mbps. STi0-15 and STo0-15 may be set to 16.384 Mbps. Combinations of two bit rates, *N* and *2N* are provided. See Table 1.

By using Zarlink's message mode capability, the microprocessor can access input and output timeslots on a per channel basis. This feature is useful for transferring control and status information for external circuits or other ST-BUS devices.

To correct for backplane delays, the MT90826 has a frame offset calibration function which allows users to measure the frame delay on any of the input streams, This information can then be used to program the input offset dealy for each individual stream. Refer to Table 7, 8, and 9 and Figure 6. In addition, the MT90826 allow users to advance

the output data position up to 45ns to compensate for the output delay caused by excessive output loading conditions. See Figure 7 “Examples for Frame Output Offset Timing”.

Serial Interface Mode	Input Stream	Input Data Rate	Output Stream	Output Data Rate
8 Mbps	STi0-31	8 Mbps	STo0-31	8 Mbps
16 Mbps	STi0-15	16 Mbps	STo0-15	16 Mbps
4 Mbps and 8 Mbps	STi0-15	4 Mbps	STo0-15	4 Mbps
	STi15-31	8 Mbps	STo16-31	8 Mbps
16 Mbps and 8 Mbps	STi0-11	16 Mbps	STo0-11	16 Mbps
	STi12-19	8 Mbps	STo12-19	8 Mbps
4 Mbps	STi0-31	4 Mbps	STo0-31	4 Mbps
2 Mbps and 4 Mbps	STi0-15	2 Mbps	STo0-15	2 Mbps
	STi16-31	4 Mbps	STo16-31	4 Mbps
2 Mbps	STi0-31	2 Mbps	STo0-31	2 Mbps

Table 1 - Stream Usage under Various Operation Modes

ODE pin	OSB bit in Control register	OE bit in Connection Memory	ST-BUS Output Driver
0	0	X	High-Z
X	X	0	Per Channel High-Z
1	0	1	Enable
0	1	1	Enable
1	1	1	Enable

Table 2 - Output High Impedance Control

The microport interface is compatible with Motorola non-multiplexed buses. Connection memory locations may be directly written to or read from; data memory locations may be directly read from. A $\overline{\text{DTA}}$ signal is provided to hold the bus until the asynchronous microport operation is queued into the device.

A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Location
0	0	0	0	0	0	0	0	0	0	0	0	0	0	Control Register, CR
0	0	0	0	0	0	0	0	0	0	0	0	0	1	Frame Alignment Register, FAR
0	0	0	0	0	0	0	0	0	0	0	0	1	0	Input Offset Selection Register 0, DOS0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	Input Offset Selection Register 1, DOS1
0	0	0	0	0	0	0	0	0	0	0	1	0	0	Input Offset Selection Register 2, DOS2
0	0	0	0	0	0	0	0	0	0	0	1	0	1	Input Offset Selection Register 3, DOS3
0	0	0	0	0	0	0	0	0	0	0	1	1	0	Input Offset Selection Register 4, DOS4

Table 3 - Address Map for Registers (A13 = 0)

A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Location
0	0	0	0	0	0	0	0	0	0	0	1	1	1	Input Offset Selection Register 5, DOS5
0	0	0	0	0	0	0	0	0	0	1	0	0	0	Input Offset Selection Register 6, DOS6
0	0	0	0	0	0	0	0	0	0	1	0	0	1	Input Offset Selection Register 7, DOS7
0	0	0	0	0	0	0	0	0	0	1	0	1	0	Frame Output Offset Register, FOR0
0	0	0	0	0	0	0	0	0	0	1	0	1	1	Frame Output Offset Register, FOR1
0	0	0	0	0	0	0	0	0	0	1	1	0	0	Frame Output Offset Register, FOR2
0	0	0	0	0	0	0	0	0	0	1	1	0	1	Frame Output Offset Register, FOR3
0	0	0	0	0	0	0	0	0	0	1	1	1	0	Unused
0	0	0	0	0	0	0	0	0	0	1	1	1	1	Unused
0	0	0	0	0	0	0	0	0	1	0	0	0	0	Unused
0	0	0	0	0	0	0	0	0	1	0	0	0	1	Bit Error Input Selection Register, BISR
0	0	0	0	0	0	0	0	0	1	0	0	1	0	Bit Error Count Register, BECR

Table 3 - Address Map for Registers (A13 = 0) (continued)

2.0 Functional Description

A functional Block Diagram of the MT90826 is shown in Figure 1.

2.1 Data and Connection Memory

For all data rates, the received serial data is converted to parallel format by internal serial-to-parallel converters and stored sequentially in the data memory. Depending upon the selected operation programmed in the control register, the usable data memory may be as large as 4,096 bytes. The sequential addressing of the data memory is performed by an internal counter, which is reset by the input 8 kHz frame pulse ($\overline{F0i}$) to mark the frame boundaries of the incoming serial data streams.

Data to be output on the serial streams may come from either the data memory or connection memory. Locations in the connection memory are associated with particular ST-BUS output channels. When a channel is due to be transmitted on an ST-BUS output, the data for this channel can be switched either from an ST-BUS input in connection mode, or from the lower half of the connection memory in message mode. Data destined for a particular channel on a serial output stream is read from the data memory or connection memory during the previous channel timeslot. This allows enough time for memory access and parallel-to-serial conversion.

2.2 Connection and Message Modes

In the connection mode, the addresses of the input source data for all output channels are stored in the connection memory. The connection memory is mapped in such a way that each location corresponds to an output channel on the output streams. For details on the use of the source address data (CAB and SAB bits), see Table 14. Once the source address bits are programmed by the microprocessor, the contents of the data memory at the selected address are transferred to the parallel-to-serial converters and then onto an ST-BUS output stream.

By having several output channels connected to the same input source channel, data can be broadcast from one input channel to several output channels.

In message mode, the microprocessor writes data to the connection memory locations corresponding to the output stream and channel number. The lower half (8 least significant bits) of the connection memory content is

transferred directly to the parallel-to-serial converter. This data will be output on the ST-BUS streams in every frame until the data is changed by the microprocessor.

The three most significant bits of the connection memory controls the following for an output channel: message or connection mode, constant or variable delay mode, enables/tristate the ST-BUS output drivers and bit error test pattern enable. If an output channel is set to a high-impedance state by setting the OE bit to zero in the connection memory, the ST-BUS output will be in a high impedance state for the duration of that channel. In addition to the per-channel control, all channels on the ST-BUS outputs can be placed in a high impedance state by pulling the ODE input pin low and programming the output stand by (OSB) bit in the control register to low. This action overrides the individual per-channel programming by the connection memory bits. See Table 2 for detail.

The connection memory data can be accessed via the microprocessor interface through the D0 to D15 pins. The addressing of the device internal registers, data and connection memories is performed through the address input pins and the Memory Select (MS) bit of the control register.

2.3 Clock Timing Requirements

The master clock ($\overline{CLK}$) frequency must be either at 8.192 MHz or 16.384 MHz for serial data rate of 2.048, 4.096, 8.192 and 16.384 Mbps; see Table 6 for the selections of the master clock frequency.

3.0 Switching Configurations

The MT90826 maximum non-blocking switching configurations is determined by the data rates selected for the serial inputs and outputs. The switching configuration is selected by three DR bits in the control register. See Table 5 and Table 6.

8 Mbps mode (DR2=0, DR1=0, DR0=0)

When the 8 Mbps mode is selected, the device is configured with 32-input/32-output data streams each having 128 64 Kbps channels. This mode allows a maximum non-blocking capacity of 4,096 x 4,096 channels. Table 1 summarizes the switching configurations and the relationship between different serial data rates and the master clock frequencies.

16 Mbps mode (DR2=0, DR1=0, DR0 =1)

When the 16 Mbps mode is selected, the device is configured with 16-input/16-output data streams each having 256 64 Kbps channels. This mode allows a maximum non-blocking capacity of 4,096 x 4,096 channels.

4 Mbps and 8 Mbps mode (DR2=0, DR1=1, DR0=0)

When the 4 Mbps and 8 Mbps mode is selected, the device is configured with 32-input/32-output data streams. STi0-15/STo0-15 have a data rate of 4 Mbps and STi16-31/STo16-31 have a data rate of 8 Mbps. This mode allows a maximum non-blocking capacity of 3,072 x 3,072 channels. The MT90826 is capable of rate conversion, allowing 4 Mbps input to be converted to 8 Mbps output and vice versa.

16 Mbps and 8 Mbps mode (DR2=0, DR1=1, DR0=1)

When the 16 Mbps and 8 Mbps mode is selected, the device is configured with 20-input/20-output data streams. STi0-11/STo0-11 have a data rate of 16 Mbps and STi12-19/STo12-19 have a data rate of 8 Mbps. This mode allows a maximum non-blocking capacity of 4,096 x 4,096 channels. The MT90826 is capable of rate conversion, allowing 16 Mbps input to be converted to 8 Mbps output and vice versa.

4 Mbps mode (DR2=1, DR1=0, DR0=0)

When the 4 Mbps mode is selected, the device is configured with 32-input/32-output data streams each having 64 64 Kbps channels. This mode allows a maximum non-blocking capacity of 2,048 x 2,048 channels.

2 Mbps and 4 Mbps mode (DR2=1, DR1=0, DR0=1)

When the 2 Mbps and 4 Mbps mode is selected, the device is configured with 32-input/32-output data streams. STi0-15/STo0-15 have a data rate of 2 Mbps and STi16-31/STo16-31 have a data rate of 4 Mbps. This mode allows a maximum non-blocking capacity of 1,536 x 1,536 channels. The MT90826 is capable of rate conversion, allowing 2 Mbps input to be converted to 4 Mbps output and vice versa.

2 Mbps mode (DR2=1, DR1=1, DR0 =0)

When the 2 Mbps mode is selected, the device is configured with 32-input/32-output data streams each having 32 64 Kbps channels. This mode allows a maximum non-blocking capacity of 1,024 x 1,024 channels.

3.1 Serial Input Frame Alignment Evaluation

The MT90826 provides the frame evaluation inputs, FEi0 to FEi31, to determine different data input delays with respect to the frame pulse $\overline{F0i}$. By using the frame evaluation input select bits (FE0 to FE4) of the frame alignment register (FAR), users can select one of the thirty-two frame evaluation inputs for the frame alignment measurement.

The internal master clock, which has a fixed relationship with the $\overline{CLK}$ and $\overline{F0i}$ depending upon the mode of operation, is used as the reference timing signal to determine the input frame delays. See Figure 5 for the signal alignments between the internal and the external master clocks.

A measurement cycle is started by setting the start frame evaluation (SFE) bit low for at least one frame. Then the evaluation starts when the SFE bit in the control register is changed from low to high. Two frames later, the complete frame evaluation (CFE) bit of the frame alignment register changes from low to high to signal that a valid offset measurement is ready to be read from bits 0 to 9 of the FAR register. The SFE bit must be set to zero before a new measurement cycle started.

The falling edge of the frame measurement signal (FEi) is evaluated against the falling edge of the frame pulse ($\overline{F0i}$). See Table 7 for the description of the frame alignment register.

3.2 Input Frame Offset Selection

Input frame offset selection allows the channel alignment of individual input streams, which operate at 4.096 Mbps, 8.192 Mbps or 16.384 Mbps, to be shifted against the input frame pulse ($\overline{F0i}$). The input offset selection is not available for streams operated at 2.048 Mbps. This feature is useful in compensating for variable path delays caused by serial backplanes of variable lengths, which may be implemented in large centralized and distributed switching systems.

Each input stream has its own delay offset value programmed by the input delay offset registers. Each delay offset register can control 4 input streams. There are eight delay offset registers (DOS0 to DOS7) to control 32 input streams. Possible adjustment can range up to +4.5 internal master clock periods forward with resolution of 0.5 internal master clock period. See Table 8 and Table 9 for frame input delay offset programming.

3.3 Output Advance Offset Selection

The MT90826 allows users to advance individual output streams up to 45 ns with a resolution of 15 ns when the device is in 8 Mbps, 16 Mbps, 4 and 8 Mbps or 16 and 8 Mbps mode. The output delay adjustment is useful in compensating for variable output delays caused by various output loading conditions. The frame output offset registers (FOR0 & FOR3) control the output offset delays for each output streams via the programming of the OFn bits.

See Table 10 and Table 11 for the frame output offset programming.

A13	Stream Address (ST0-31)						Channel Address (Ch0-255)								
	A12	A11	A10	A9	A8	Stream Location	A7	A6	A5	A4	A3	A2	A1	A0	Channel Location
1	0	0	0	0	0	Stream 0	0	0	0	0	0	0	0	0	Ch 0
1	0	0	0	0	1	Stream 1	0	0	0	0	0	0	0	1	Ch 1
1	0	0	0	1	0	Stream 2	.	.	.	.	.	.	.	.	.
1	0	0	0	1	1	Stream 3	.	.	.	.	.	.	.	.	.
1	0	0	1	0	0	Stream 4	0	0	0	1	1	1	1	0	Ch 30
1	0	0	1	0	1	Stream 5	0	0	0	1	1	1	1	1	Ch 31 (Note 2)
1	0	0	1	1	0	Stream 6	0	0	1	0	0	0	0	0	Ch 32
1	0	0	1	1	1	Stream 7	0	0	1	0	0	0	0	1	Ch 33
1	0	1	0	0	0	Stream 8	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	0	0	1	1	1	1	1	0	Ch 62
.	.	.	.	.	.	.	0	0	1	1	1	1	1	1	Ch 63 (Note 3)
1	1	0	1	1	0	Stream 22	0	1	0	0	0	0	0	0	Ch 64
1	1	0	1	1	1	Stream 23	0	1	0	0	0	0	0	1	Ch 65
1	1	1	0	0	0	Stream 24	.	.	.	.	.	.	.	.	.
1	1	1	0	0	1	Stream 25	0	1	1	1	1	1	1	0	Ch 126
1	1	1	0	1	0	Stream 26	0	1	1	1	1	1	1	1	Ch 127 (Note 4)
1	1	1	0	1	1	Stream 27	1	0	0	0	0	0	0	0	Ch 128
1	1	1	1	0	0	Stream 28	1	0	0	0	0	0	0	1	Ch 129
1	1	1	1	0	1	Stream 29	.	.	.	.	.	.	.	.	.
1	1	1	1	1	0	Stream 30	1	1	1	1	1	1	1	0	Ch 254
1	1	1	1	1	1	Stream 31	1	1	1	1	1	1	1	1	Ch 255 (Note 5)

1. Bit A13 must be high for access to data and connection memory positions. Bit A13 must be low for access to registers.
2. Channels 0 to 31 are used when serial stream is at 2Mbps.
3. Channels 0 to 63 are used when serial stream is at 4Mbps
4. Channels 0 to 127 are used when serial stream is at 8Mbps
5. Channels 0 to 255 are used when serial stream is at 16Mbps

Table 4 - Address Map for Memory Locations (A13 = 1)

3.4 Memory Block Programming

The MT90826 provides users with the capability of initializing the entire connection memory block in two frames. Bits 13 to 15 of every connection memory location will be programmed with the pattern stored in bits 13 to 15 of the control register.

The block programming mode is enabled by setting the memory block program (MBP) bit of the control register high. When the block programming enable (BPE) bit of the control register is set to high, the block programming data will be loaded into the bits 13 to 15 of every connection memory location. The other connection memory bits (bit 0 to 12) are loaded with zeros. When the memory block programming is complete, the device resets the BPE bit to zero.

3.5 Bit Error Rate Monitoring

The MT90826 allows users to perform bit error rate monitoring by sending a pseudo random pattern to a selected ST-BUS output channel and receiving the pattern from a selected ST-BUS input channel. The pseudo random pattern is internally generated by the device with the polynomial of 2^{15} -1.

Users can select the pseudo random pattern to be presented on a ST-BUS channel by programming the TM0 and TM1 bits in the connection memory. When TM0 and TM1 bits are high, the pseudo random pattern is output to the selected ST-BUS output channel. The pseudo random pattern is then received by a ST-BUS input channel which is selected using the BSA and BCA bits in the bit error rate input selection register (BISR). An internal bit error counter keeps track of the error counts which is then stored in the bit error count register (BECR).

The bit error test is enabled and disabled by the SBER bit in the control register. Setting the bit from zero to one initiates the bit error test and enables the internal bit error counter. When the bit is programmed from one to zero,

the device stops the bit error rate test and the internal bit error counter and transfers the error counts to the bit error count register.

In the control register, a zero to one transition of the CBER bit resets the bit error count register and the internal bit error counter.

The MT90826 does not recognize an input of all 1s as an error. If all 1s are being fed into the input stream and channel, the BERT on chip BECR does not increment. This test is performed by sending defined data through the message mode to ensure there is proper connectivity, and then running the BER test normally.

4.0 Delay Through the MT90826

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform timeslot interchange functions with different throughput delay capabilities on the per-channel basis. For voice application, select variable throughput delay to ensure minimum delay between input and output data. In wideband data applications, select constant throughput delay to maintain the frame integrity of the information through the switch.

The delay through the device varies according to the type of throughput delay selected by the TM bits in the connection memory.

4.1 Variable Delay Mode (TM1=0, TM0=0)

The delay in this mode is dependent only on the combination of source and destination channels and is independent of input and output streams. The delay through the switch can vary from 3 channels to 1 frame + 3 channels. The Variable delay is only available for odd number output streams but not for the even number output streams. Avoid programming the TM0 and TM1 bits to zero in the connection memory when the destination output streams are STo0, 2, 4, ..., 28 and 30.

4.2 Constant Delay Mode (TM1=1, TM0=0)

In this mode, frame integrity is maintained in all switching configurations by making use of a multiple data memory buffer. The delay through the switch is always two frames. The constant delay mode is available for all output streams.

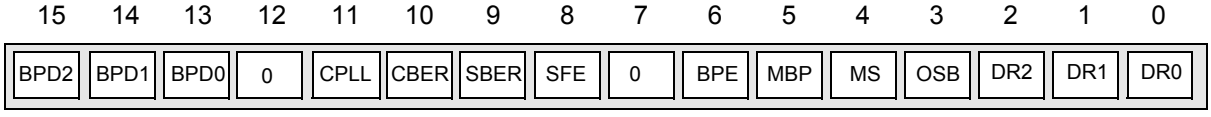
5.0 Microprocessor Interface

The MT90826 provides a parallel microprocessor interface for non-multiplexed bus structures. This interface is compatible with Motorola non-multiplexed buses. The required microprocessor signals are the 16-bit data bus (D0-D15), 14-bit address bus (A0-A13) and 4 control lines ($\overline{CS}$, $\overline{DS}$, R/$\overline{W}$ and $\overline{DTA}$). See Figure 16 for Motorola non-multiplexed microport timing.

The MT90826 microport provides access to the internal registers, connection and data memories. All locations provide read/write access except for the data memory and BECR registers which are read only.

For data memory read operations, two consecutive microprocessor cycles are required. The read address (A0-A13) should remain the same for the two consecutive read cycles. The data memory content from the first read cycle should be ignored.

Read/Write Address: 0000_H,
Reset Value: 0000_H.



Bit	Name	Description
15 - 13	BPD2-0	**Block Programming Data.** These bits carry the value to be loaded into the connection memory block whenever the memory block programming feature is activated. After the MBP bit is set to 1 and the BPE bit is set to 1, the contents of the bits BPD2- 0 are loaded into bit 15 to bit 13 of the connection memory. Bit 12 to bit 0 of the connection memory are set to 0.
12	Unused	**Must be zero for normal operation**.
11	CPLL	**PLL Input Frequency Select.** When zero or one, the $\overline{CLK}$ input is 16.384 MHz and the $\overline{F0i}$ input is 60 ns wide. When one, the $\overline{CLK}$ input is 8.192 MHz and the $\overline{F0i}$ input is 122 ns wide. See Table 6 for the usage of the clock frequency.
10	CBER	**Clear Bit Error Rate Register**. A zero to one transition in this bit resets the internal bit error counter and the bit error count register to zero.
9	SBER	**Start Bit Error Rate Test**. A zero to one transition in this bit starts the bit error rate test. The bit error test result is kept in the bit error count register. A one to zero transition stops the bit error rate test and the internal bit error counter.
8	SFE	**Start Frame Evaluation.** A zero to one transition in this bit starts the frame evaluation procedure. When the CFE bit in the frame alignement (FAR) register changes from zero to one, the evaluation procedure stops. To start another frame evaluation cycle, set this bit to zero.
7	Unused	Must be zero for normal operation.
6	BPE	**Begin Block programming Enable.** A zero to one transition of this bit enables the memory block programming function. The BPE and BPD2-0 bits have to be defined in the same write operation. Once the BPE bit is set high, the device requires two frames to complete the block programming. After the programming function has finished, the BPE bit returns to zero to indicate the operation is completed. When the BPE = 1, the BPE or MBP can be set to 0 to abort the programming operation. When BPE = 1, the other bits in the control register must not be changed for two frames to ensure proper operation.
5	MBP	**Memory Block Program.** When 1, the connection memory block programming feature is ready to program Bit13 to Bit15 of the connection memory. When 0, feature is disabled.

Table 5 - Control Register Bits

Read/Write Address: 0000_H,
Reset Value: 0000_H.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BPD2	BPD1	BPD0	0	CPLL	CBER	SBER	SFE	0	BPE	MBP	MS	OSB	DR2	DR1	DR0

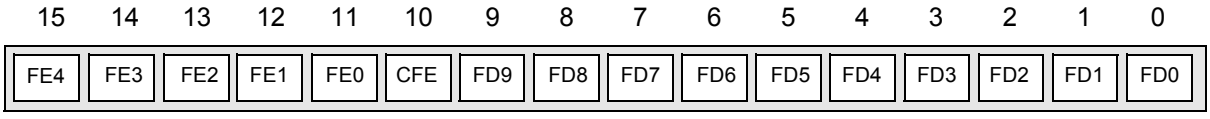
Bit	Name	Description
4	MS	**Memory Select.** When 0, connection memory is selected for read or write operations. When 1, the data memory is selected for read operations and connection memory is selected for write operations. (No microprocessor write operation is allowed for the data memory.) For data memory read operations, two consecutive microprocessor cycles are required. The read address should remain the same for the two consecutive read cycles. The data memory content from the first read cycle should be ignored. The correct data memory content will be presented to the data bus on the second read cycle.
3	OSB	**Output Stand By.** This bit controls the device output drivers. OSB bit / ODE pin / OE bit / STo0 - 31 0 / 1 / 1 / Enable 1 / 0 / 1 / Enable 1 / 1 / 1 / Enable 0 / 0 / X / High impedance state X / X / 0 / Per-channel high impedance
2 - 0	DR2-0	**Data Rate Select.** Input/Output data rate selection. See next table (Table 6) for detailed programming.

Table 5 - Control Register Bits (continued)

DR2	DR1	DR0	Serial Interface Mode	CLK (CPLL=0)	CLK (CPLL=1)
0	0	0	8 Mbps	16.384 MHz	16.384 MHz
0	0	1	16 Mbps		
0	1	0	4 and 8 Mbps		
0	1	1	16 and 8 Mbps		
1	0	0	4 Mbps	16.384 MHz	8.192 MHz
1	0	1	2 and 4 Mbps		
1	1	0	2 Mbps	16.384 MHz	8.192 MHz

Table 6 - Serial Data Rate Selections and External Clock Rates

Read/Write Address: 0001_H,
Reset Value: 0000_H.



Bit	Name	Description
15 - 11	FE4-0	**Frame Evaluation Input Select.** The binary value expressed in these bits refers to the frame evaluation inputs, FEi0 to FEi31.
10	CFE	**Complete Frame Evaluation.** When CFE = 1, the frame evaluation is completed and FD9 to FD0 bits contains a valid frame alignment offset. This bit is reset to zero, when SFE bit in the control register is changed from 1 to 0.
9	FD9	**Frame Delay Bit 9.** The falling edge of FEi input is sampled during the internal master clock high phase (FD9 = 1) or during the low phase (FD9 = 0). This bit allows the measurement resolution to 1/2 internal master clock cycle. See Figure 5 for clock signal alignment. Internal Master Clock — Operation Mode C8i — 2 Mbps C16i — 4 Mbps, 2&4 Mbps C32i — 8 Mbps, 16 Mbps, 4&8 Mbps, 16&8 Mbps
8 - 0	FD8-0	**Frame Delay Bits.** The binary value expressed in these bits refers to the measured input offset value. These bits are reset to zero when the SFE bit of the control register changes from 1 to 0. (FD8 = MSB, FD0 = LSB)

Table 7 - Frame Alignment (FAR) Register Bits

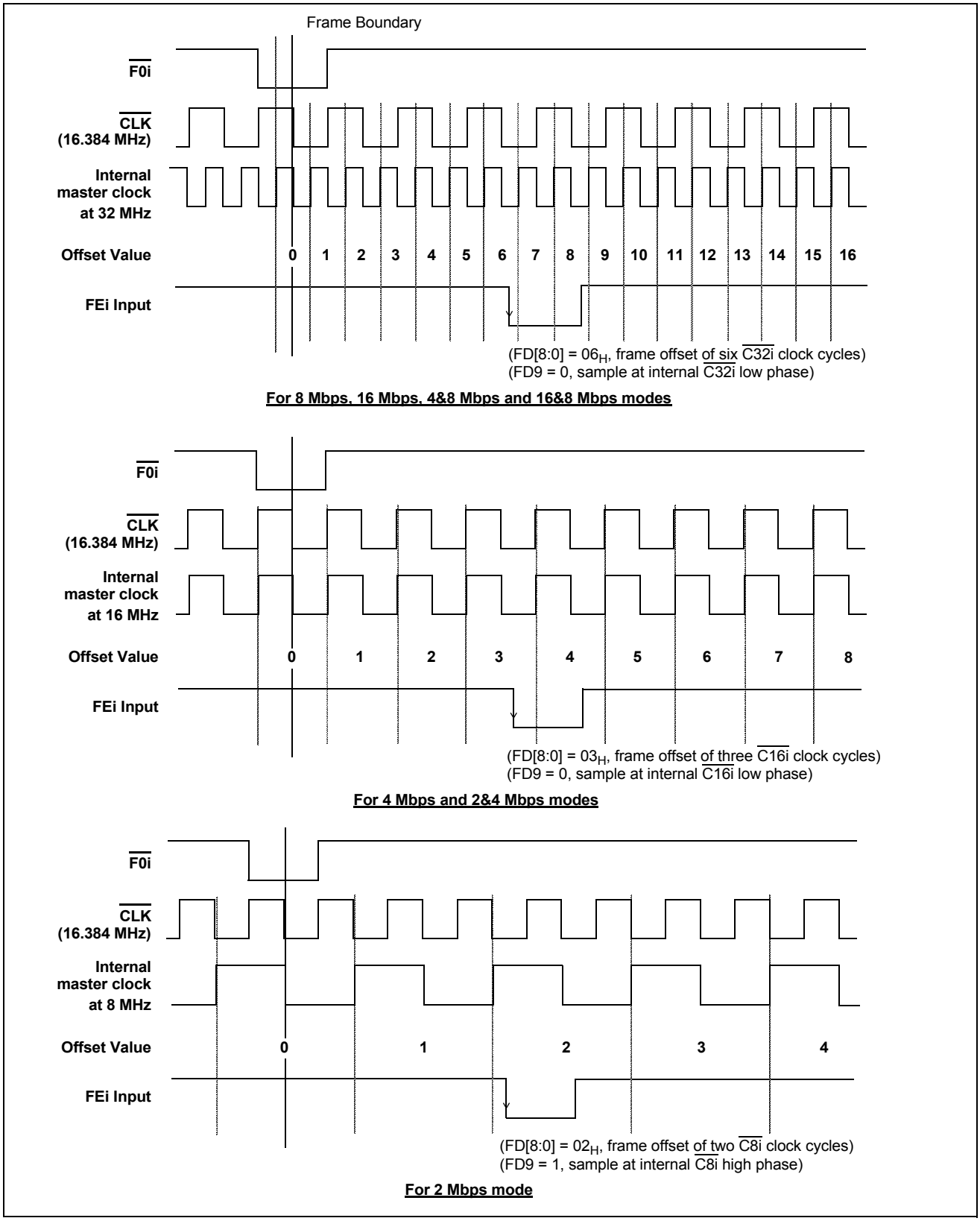
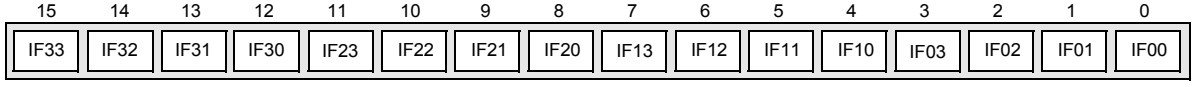


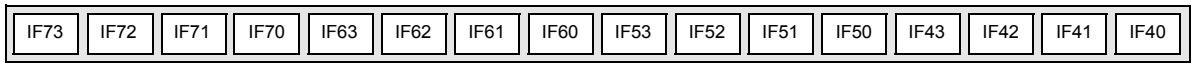
Figure 5 - Example for Frame Alignment Measurement

Read/Write Address: 02_H for DOS0 register, 03_H for DOS1 register,
04_H for DOS2 register, 05_H for DOS3 register,
06_H for DOS4 register, 07_H for DOS5 register,
08_H for DOS6 register, 09_H for DOS7 register,

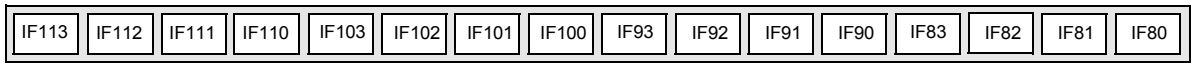
Reset value: 0000_H for all DOS registers.



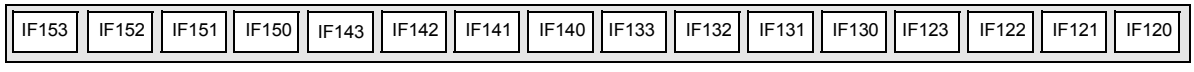
DOS0 register



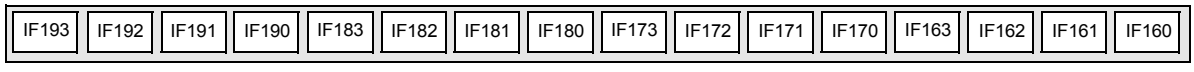
DOS1 register



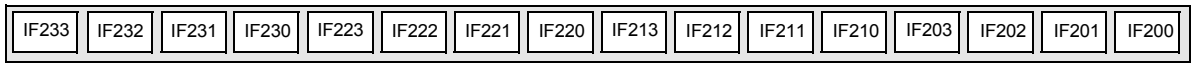
DOS2 register



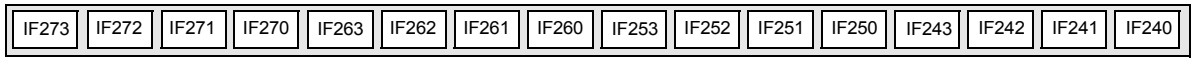
DOS3 register



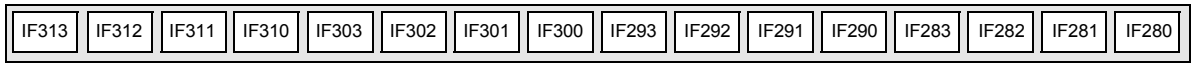
DOS4 register



DOS5 register



DOS6 register



DOS7 register

Name (Note 1)	Description
IFn3-0	**Input Offset Bits 3,2,1 & 0.** These four bits define how long the serial interface receiver takes to recognize and store bit 0 from the STi pin: i.e., to start a new frame. The input frame offset can be selected to +2.25 external clock periods (or 4.50 internal clock ___ cycles) from the point where the external frame pulse input signal is applied to the $\overline{F0i}$ inputs of the device. See Table 9. When the STi pin has a stream rate of 2.048 Mbps, the input offset cannot be adjusted and the input offset bits have to be set to zero.

Table 8 - Frame Delay Offset Register (DOS) Bits

Read/Write Address: 02_H for DOS0 register, 03_H for DOS1 register,
04_H for DOS2 register, 05_H for DOS3 register,
06_H for DOS4 register, 07_H for DOS5 register,
08_H for DOS6 register, 09_H for DOS7 register,

Reset value: 0000_H for all DOS registers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF33	IF32	IF31	IF30	IF23	IF22	IF21	IF20	IF13	IF12	IF11	IF10	IF03	IF02	IF01	IF00

DOS0 register

IF73	IF72	IF71	IF70	IF63	IF62	IF61	IF60	IF53	IF52	IF51	IF50	IF43	IF42	IF41	IF40

DOS1 register

IF113	IF112	IF111	IF110	IF103	IF102	IF101	IF100	IF93	IF92	IF91	IF90	IF83	IF82	IF81	IF80

DOS2 register

IF153	IF152	IF151	IF150	IF143	IF142	IF141	IF140	IF133	IF132	IF131	IF130	IF123	IF122	IF121	IF120

DOS3 register

IF193	IF192	IF191	IF190	IF183	IF182	IF181	IF180	IF173	IF172	IF171	IF170	IF163	IF162	IF161	IF160

DOS4 register

IF233	IF232	IF231	IF230	IF223	IF222	IF221	IF220	IF213	IF212	IF211	IF210	IF203	IF202	IF201	IF200

DOS5 register

IF273	IF272	IF271	IF270	IF263	IF262	IF261	IF260	IF253	IF252	IF251	IF250	IF243	IF242	IF241	IF240

DOS6 register

IF313	IF312	IF311	IF310	IF303	IF302	IF301	IF300	IF293	IF292	IF291	IF290	IF283	IF282	IF281	IF280

DOS7 register

Name (Note 1)	Description
Note 1: n denotes a STi stream number from 0 to 31.	

Table 8 - Frame Delay Offset Register (DOS) Bits (continued)

Input Stream Offset	Measurement Result from Frame Delay Bits				Corresponding Input Offset Bits			
	FD9	FD2	FD1	FD0	IFn3	IFn2	IFn1	IFn0
No internal master clock shift (Default)	1	0	0	0	0	0	0	0
+ 0.5 internal master clock shift	0	0	0	0	0	0	0	1
+ 1.0 internal master clock shift	1	0	0	1	0	0	1	0
+ 1.5 internal master clock shift	0	0	0	1	0	0	1	1
+ 2.0 internal master clock shift	1	0	1	0	0	1	0	0
+ 2.5 internal master clock shift	0	0	1	0	0	1	0	1
+ 3.0 internal master clock shift	1	0	1	1	0	1	1	0
+ 3.5 internal master clock shift	0	0	1	1	0	1	1	1
+ 4.0 internal master clock shift	1	1	0	0	1	0	0	0
+ 4.5 internal master clock shift	0	1	0	0	1	0	0	1

Table 9 - Frame delay Bits (FD9, FD2-0) and Input Offset Bits (IFn3-0)

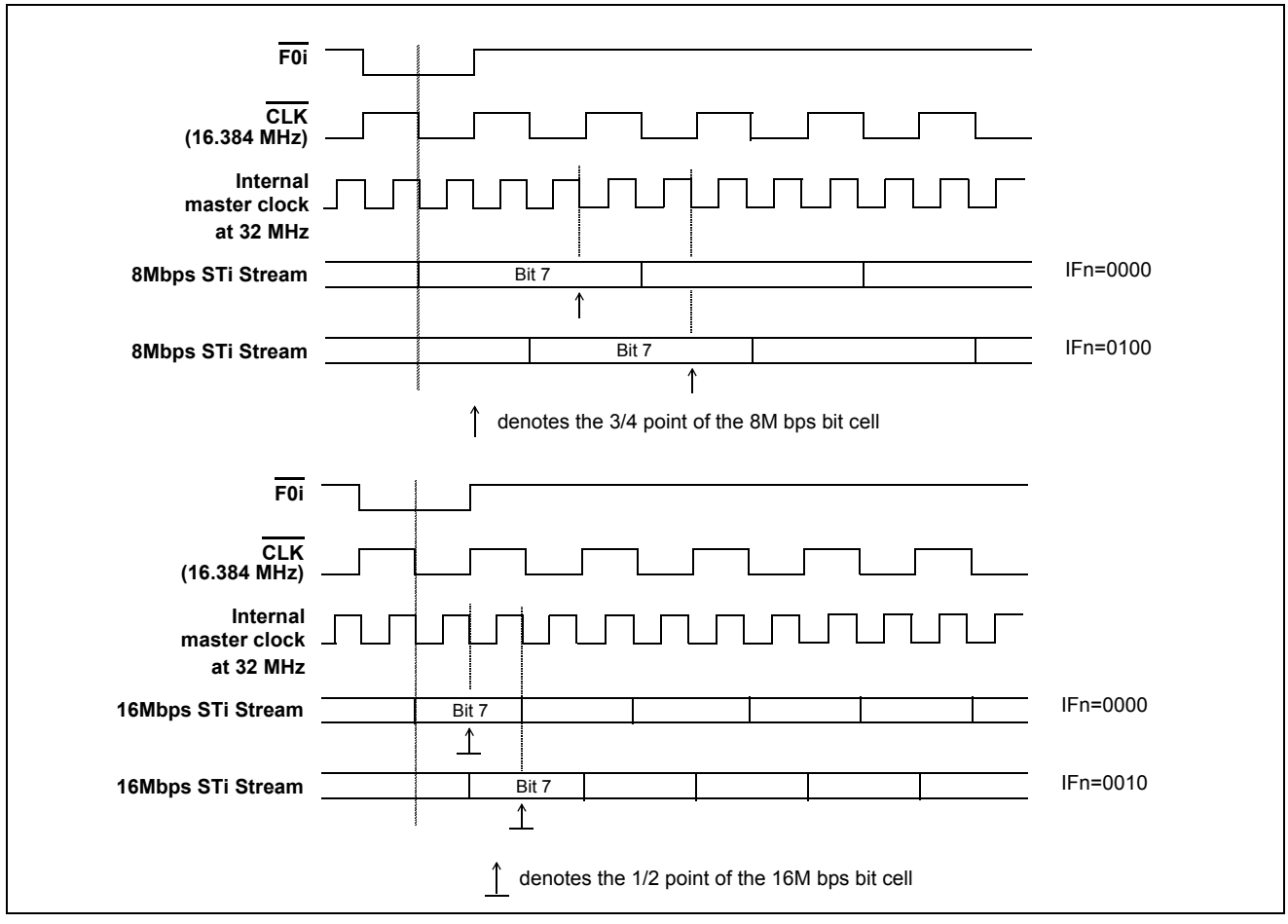
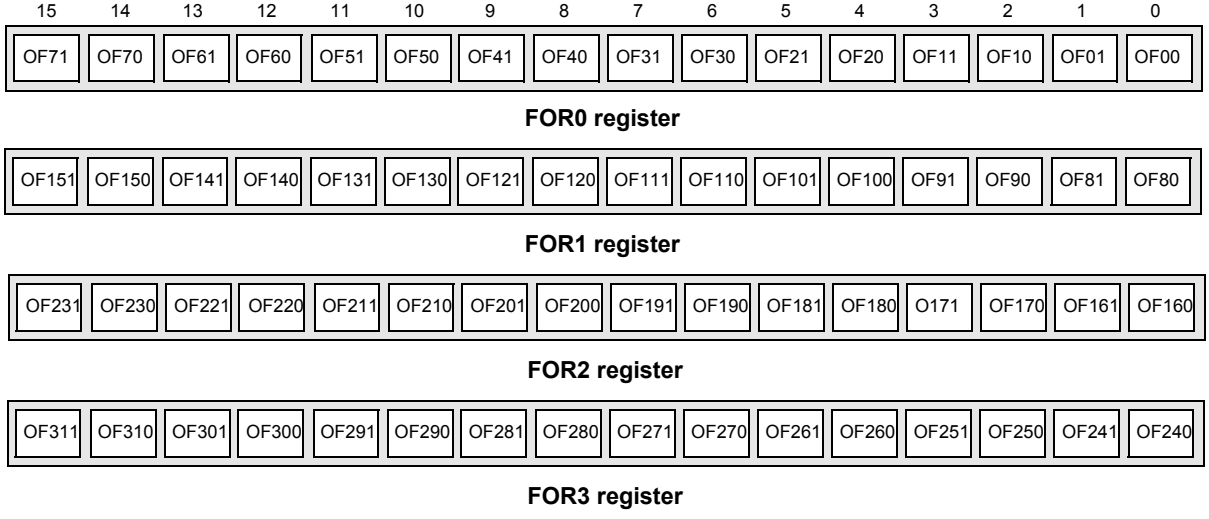


Figure 6 - Examples for Input Offset Delay Timing

Read/Write Address: $000A_H$ for FOR0 register,
$000B_H$ for FOR1 register,
$000C_H$ for FOR2 register,
$000D_H$ for FOR3 register,

Reset value: 0000_H for all FOR registers.



Name (Note 1)	Description
OFn1, OFn0 (n = 0 to 31)	**Output Offset Bits 1 - 0.** These two bits define how soon the serial interface transmitter output the bit 0 from the STo pin. The output stream offset can be selected to -45 ns from the point where the external frame pulse input signal is applied to the F0i inputs of the device. See Table 11 and Figure 6.

Table 10 - Frame Output Offset (FOR) Register Bits

Corresponding Output Offset Bits		Output Stream Offset for 8 Mbps, 16 Mbps, 4&8 Mbps and 16&8 Mbps modes (Not available for 2 Mbps, 4 Mbps and 2&4 Mbps modes)
OFn1	OFn0	
0	0	0 ns
0	1	-15 ns
1	0	-30 ns
1	1	-45 ns

Table 11 - Output Offset Bits (FD9, FD2-0)

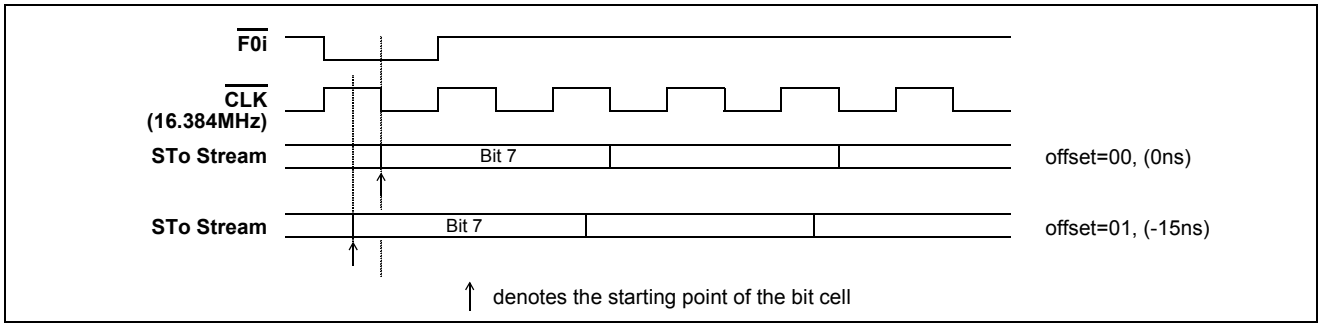


Figure 7 - Examples for Frame Output Offset Timing

Read/Write Address: 0011_H for BISR register,
Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	BSA4	BSA3	BSA2	BSA1	BSA0	BCA7	BCA6	BCA5	BCA4	BCA3	BCA2	BCA1	BCA0

Bit	Name	Description
12 - 8	BSA4 - BSA0	**BER Input Stream Address Bits.** The number expressed in binary notation on these bits refers to the input data stream which receives the pseudo random pattern.
7 - 0	BCA7 - BCA0	**BER Input Channel Address Bits.** The number expressed in binary notation on these bits refers to the input channel which receives the pseudo random pattern.

Table 12 - Bit Error Input Selection (BISR) Register Bits

Read Address: 0012_H for BECR register,

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BER15	BER14	BER13	BER12	BER11	BER10	BER9	BER8	BER7	BER6	BER5	BER4	BER3	BER2	BER1	BER0

Bit	Name	Description
15 - 0	BER15 - BER0	**Bit Error Rate Count Bits.** The number expressed in binary notation on these bits refers to the bit error counts. The register content can be cleared by programming the CBER bit in the control register from zero to one.

Table 13 - Bit Error Count (BECR) Register Bits

The correct data memory content will be presented to the data bus (D0-D15) on the second read cycle.

6.0 Memory Mapping

The address bus on the microprocessor interface selects the internal registers and memories of the MT90826. If the A13 address input is low, then the registers are addressed by A12 to A0 according to Table 3.

If the A13 is high, the remaining address input lines are used to select location in the data or connection memory depending upon MS bit in the control register. For data memory reads, the serial inputs are selected. For connection memory writes, the serial outputs are selected. The destination stream address bits and channel address bits are defined by A12 to A8 and A7 to A0 respectively. See Table 4 for the memory address mapping.

The control register controls all the major functions of the device. It selects the internal memory locations that specify the input and output channels selected for switching and should be programmed immediately after system power-up to establish the desired switching configuration as explained in the Switching Configurations sections.

The data in the control register consists of the block programming (BPD0-2), the DPLL control (CPLL), the clear BER test (CBER), the start BER test (SBER), the start frame evaluation (SFE), the block programming enable (BPE), the memory block programming bit (MBP), the memory select bits (MS), the output stand by bit (OSB) and the data rate selection (DR0-2) bits. See Table 5 for the description of the control register bits.

7.0 Connection Memory Control

The connection memory controls the switching configuration of the device. Locations of the connection memory are associated with particular STo output streams.

The TM0 and TM1 bits of each connection memory location allows the selection of Variable throughput delay, Constant throughput delay, Message or Bit error test mode for all STo channels.

When the variable or constant throughput delay mode is selected, (TM1=0/1, TM0=0), the contents of the stream address bit (SAB) and the channel address bit (CAB) of the connection memory defines the source information (stream and channel) of the timeslot that will be switched to the STo streams.

When the message mode is selected, (TM1=0, TM0=1) , only the lower half byte (8 least significant bits) of the connection memory is transferred to the associated STo output channel.

When the bit error test mode is selected, (TM1=1, TM0=1), the pseudo random pattern will be output on the associated STo output channel.

See Table 14 for the description of the connection memory bits.

8.0 $\overline{\text{DTA}}$ Data Transfer Acknowledgment Pin

The $\overline{\text{DTA}}$ pin is driven LOW by internal logic, to indicate to the CPU that a data bus transfer is complete. When the read or write cycle ends, this pin changes to the high-impedance state.

9.0 Initialization of the MT90826

During power up, the $\overline{\text{TRST}}$ pin should be pulsed low, or held low continuously, to ensure that the MT90826 is in the normal functional mode. A 5 K pull-down resistor can be connected to the $\overline{\text{TRST}}$ pin so that the device will not enter the JTAG test mode during power up.

An external RC network with a time constant of five times the power supply rise time should be connected to the $\overline{\text{RESET}}$ pin to ensure that the device is properly reset after power up.

After power up, the contents of the connection memory can be in any state. The ODE pin should be held low after power up to keep all serial outputs in a high impedance state until the microprocessor has initialized the switching matrix. This procedure prevents two serial outputs from driving the same stream simultaneously.

Wait for 600 μs for the APLL module to be stabilized before starting the microprocessor initialization routine.

During the microprocessor initialization routine, the microprocessor should program the desired active paths through the switch. Users can also consider using the memory block programming feature to quickly initialize the OE, TM0 and TM1 bits in the connection memory. When this process is complete, the microprocessor controlling the matrices can either bring the ODE pin high or enable the OSB bit in control register to relinquish the high impedance state control.

10.0 JTAG Support

The MT90826 JTAG interface conforms to the Boundary-Scan standard IEEE1149.1. This standard specifies a design-for-testability technique called Boundary-Scan test (BST). The operation of the boundary-scan circuitry is controlled by an external test access port (TAP) Controller.

10.1 Test Access Port (TAP)

The Test Access Port (TAP) provides access to the many test functions of the MT90826. It consists of three input pins and one output pin. The following pins are from the TAP.

- Test Clock Input (TCK)
  TCK provides the clock for the test logic. The TCK does not interfere with any on-chip clock and thus remain independent. The TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.
- Test Mode Select Input (TMS)
  The logic signals received at the TMS input are interpreted by the TAP Controller to control the test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to Vdd when it is not driven from an external source.
- Test Data Input (TDI)
  Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. Both registers are described in a subsequent section. The received input data is sampled at the rising edge of TCK pulses. This pin is internally pulled to Vdd when it is not driven from an external source.
- Test Data Output (TDO)
  Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or data register are serially shifted out towards the TDO. The data out of the TDO is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDO driver is set to a high impedance state.
- Test Reset ($\overline{\text{TRST}}$)
  Resets the JTAG scan structure. This pin is internally pulled to VDD.

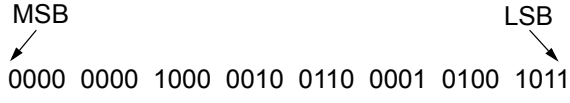
10.2 Instruction Register

In accordance with the IEEE 1149.1 standard, the MT90826 uses public instructions. The JTAG Interface contains a three-bit instruction register. Instructions are serially loaded into the instruction register from the TDI when the TAP Controller is in its shifted-IR state. Subsequently, the instructions are decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current, and to define the serial test data register path, which is used to shift data between TDI and TDO during data register scanning.

Test Data Register

As specified in IEEE 1149.1, the MT90826 JTAG Interface contains three test data registers:

- The Boundary-Scan register
  The Boundary-Scan register consists of a series of Boundary-Scan cells arranged to form a scan path around the boundary of the MT90826 core logic.
- The Bypass Register
  The Bypass register is a single stage shift register that provides a one-bit path from TDI to its TDO.
- The Device Identification Register
  The device identification register is a 32-bit register with the register contain of:



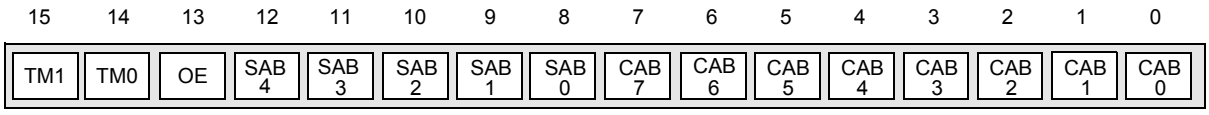
  The LSB bit in the device identification register is the first bit clock out.

The MT90826 scan register contains 165 bits.

Device Pin	Boundary Scan Bit 0 to Bit 165		
	Tri-state Control	Output Scan Cell	Input Scan Cell
$\overline{F0i}$			0
CLK			1
ODE			2
STi0			3
STi1			4
STi2			5
STi3			6
STo0	7	8	
STo1	9	10	
STo2	11	12	
STo3	13	14	
STi4			15
STi5			16
STi6			17
STi7			18
STo4	19	20	
STo5	21	22	
STo6	23	24	
STo7	25	26	
STi8			27
STi9			28
STi10			29
STi11			30
STo8	31	32	
STo9	33	34	
STo10	35	36	
STo11	37	38	
STi12			39
STi13			40
STi14			41
STi15			42
STo12	43	44	
STo13	45	46	
STo14	47	48	
STo15	49	50	
STi16			51
STi17			52
STi18			53
STi19			54
STo16	55	56	
STo17	57	58	
STo18	69	60	
STo19	61	62	
STi20			63
STi21			64
STi22			65
STi23			66
STo20	67	68	
STo21	69	70	
STo22	71	72	
STo23	73	74	
STi24			75
STi25			76
STi26			77
STi27			78
STo24	79	80	
STo25	81	82	
STo26	83	84	
STo27	85	86	

Device Pin	Boundary Scan Bit 0 to Bit 165		
	Tri-state Control	Output Scan Cell	Input Scan Cell
STi28			87
STi29			88
STi30			89
STi31			90
STo28	91	92	
ST029	93	94	
ST030	95	96	
STo31	97	98	
D0	99	100	101
D1	102	103	104
D2	105	106	107
D3	108	109	110
D4	111	112	113
D5	114	115	116
D6	117	118	119
D7	120	121	122
D8	123	124	125
D9	126	127	128
D10	129	130	131
D11	132	133	134
D12	135	136	137
D13	138	139	140
D14	141	142	143
D15	144	145	146
$\overline{DTA}$[1]	147	147	
$\overline{CS}$			148
R/$\overline{W}$			149
$\overline{DS}$			150
A0			151
A1			152
A2			153
A3			154
A4			155
A5			156
A6			157
A7			158
A8			159
A9			160
A10			161
A11			162
A12			163
A13			164
RESETb			165

Note 1: $\overline{DTA}$ is an open drain output and it requires a pull-up resistor. Safe for $\overline{DTA}$ = 0. $\overline{DTA}$ cell = 1 will produce active LOW.



Bit	Name	Description
15-14	TM1-0	Mode Select Bits. TM1 TM0 Mode Selection 0 0 Variable Throughput Delay mode (Note 1) 1 0 Constant Throughput Delay mode (Note 2) 0 1 Message mode; the contents of the connection memory are output on the corresponding output channel and stream. Only the lower byte (bit 7 - bit 0) will be output to the ST-BUS output pins. 1 1 Bit Error Test mode; the pseudo random test pattern will be output on the output channel and stream associated with this location.
13	OE	**Output Enable.** This bit enables the drivers of STo pins on a per-channel basis. When 1, the STo output driver functions normally. When 0, the STo output driver is in a high-impedance state.
12-8	SAB4-0	**Source Stream Address Bits.** The binary value is the number of the data stream for the source of the connection.
7-0	CAB7-0	**Source Channel Address Bits.** The binary value is the number of the channel for the source of the connection. When the message mode is enabled, these entire 8 bits are output on the output channel and stream associated with this location.

Note 1: The Variable delay is only available for odd number output streams but not for the even number output streams. Avoid programming the TM0 and TM1 bits to zero in the connection memory when the destination output streams are STo0, 2, 4, ... , 28 and 30.
Note 2: The constant delay mode is available for all output streams.

Table 14 - Connection Memory Bits

Data Rate	SAB4 to SAB0 Bits Used to Determine the Source Stream of the connection	CAB Bits Used to Determine the Source Channel of the Connection
8 Mbps	SAB4 to SAB0 (STi0 to STi31)	CAB6 to CAB0 (128 channel/frame)
16 Mbps	SAB3 to SAB0 (STi0 to STi15)	CAB7 to CAB0 (256 channel/frame)
4 Mbps & 8 Mbps	SAB4 to SAB0 (STi0 to STi31)	CAB6 to CAB0 (64 or 128 channel/frame)
16 Mbps & 8 Mbps	SAB4 to SAB0 (STi0 to STi19)	CAB7 to CAB0 (128 or 256 channel/frame)
4 Mbps	SAB4 to SAB0 (STi0 to STi31)	CAB5 to CAB0 (64 channel/frame)
2 Mbps & 4 Mbps	SAB4 to SAB0 (STi0 to STi31)	CAB5 to CAB0 (32 or 64 channel/frame)
2 Mbps	SAB4 to SAB0 (STi0 to STi31)	CAB4 to CAB0 (32 channel/frame)

Table 15 - SAB and CAB Bits Programming for Various Interface Mode

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	V_{DD}	-0.3	5.0	V
2	Voltage on any 3.3 V tolerant pin I/O (other than supply pins)	V_I	V_{SS} - 0.3	V_{DD} + 0.3	V
3	Voltage on any 5 V tolerant pin I/O (other than supply pins)	V_I	V_{SS} - 0.3	5.0	V
4	Continuous Current at digital outputs	I_o		20	mA
5	Package power dissipation	P_D		1	W
6	Storage temperature	T_S	- 65	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied

Recommended Operating Conditions - Voltages are with respect to ground (V_{ss}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		+85	°C	
2	Positive Supply	V_{DD}	3.0		3.6	V	
3	Input High Voltage	V_{IH}	$0.7V_{DD}$		V_{DD}	V	
4	Input High Voltage on 5 V Tolerant Inputs	V_{IH}			5.5	V	
5	Input Low Voltage	V_{IL}	V_{SS}		$0.3V_{DD}$	V	

DC Electrical Characteristics - Voltages are with respect to ground (V_{ss}) unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	INPUTS	Supply Current	I_{DD}		64	100	mA	Output unloaded
2		Input High Voltage	V_{IH}	$0.7V_{DD}$			V	
3		Input Low Voltage	V_{IL}			$0.3V_{DD}$	V	
4		Input Leakage (input pins) Input Leakage (with pull-up or pull-down)	I_{IL} I_{BL}			15 50	µA µA	$0 \leq < V \leq V_{DD}$ See Note 1
5		Input Pin Capacitance	C_I			10	pF	
6	OUTPUTS	Output High Voltage	V_{OH}	$0.8V_{DD}$			V	I_{OH} = 10mA
7		Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 10mA
8		High Impedance Leakage	I_{OZ}			5	µA	$0 < V < V_{DD}$ See Note 1
9		Output Pin Capacitance	C_O			10	pF	

Note 1: Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (V)

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold Voltage	V_{TT}	$0.5V_{DD}$	V	
2	CMOS Rise/Fall Threshold Voltage High	V_{HM}	$0.7V_{DD}$	V	
3	CMOS Rise/Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD}$	V	

AC Electrical Characteristics - Frame Pulse and $\overline{CLK}$

	Characteristic	Sym.	Min.	Typ.	Max.	Units	$\overline{CLK}$
1	Frame pulse width	t_{FPW}	55		65	ns	16.384 MHz
2	Frame Pulse Setup time before $\overline{CLK}$ falling	t_{FPS}	5			ns	
3	Frame Pulse Hold Time from $\overline{CLK}$ falling	t_{FPH}	10			ns	
4	$\overline{CLK}$ Period	t_{CP}	55		70	ns	
5	$\overline{CLK}$ Pulse Width High	t_{CH}	20		40	ns	
6	$\overline{CLK}$ Pulse Width Low	t_{CL}	20		40	ns	
7	Frame pulse width	t_{FPW8}	115		145	ns	8.192 MHz
8	Frame Pulse Setup time before $\overline{CLK}$ falling	t_{FPS8}	5			ns	
9	Frame Pulse Hold Time from $\overline{CLK}$ falling	t_{FPH8}	10			ns	
10	$\overline{CLK}$ Period	t_{CP8}	110		150	ns	
11	$\overline{CLK}$ Pulse Width High	t_{CH8}	50		75	ns	
12	$\overline{CLK}$ Pulse Width Low	t_{CL8}	50		75	ns	
13	Clock Rise/Fall Time	t_r, t_f	0		+10	ns	

AC Electrical Characteristics - Serial Streams for ST-BUS

	Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Input Data Sample Point (Data rate of 16 Mbps)	t_{IDS_16}		30		ns	
2	Input Data Sample Point (Data rate of 8 Mbps)	t_{IDS_8}		91		ns	
3	Input Data Sample Point (Data rate of 4 Mbps)	t_{IDS_4}		183		ns	
4	Input Data Sample Point (Data rate of 2 Mbps)	t_{IDS_2}		366		ns	
5	STi Set-up Time (Data rate of 16 Mbps)	t_{SIS_16}	0			ns	
6	STi Hold Time (Date rate of 16 Mbps)	t_{SIH_16}	8			ns	
7	STi Set-up Time (Date rate of 2, 4 or 8 Mbps)	t_{SIS}	0			ns	
8	STi Hold Time (Date rate of 2, 4 or 8 Mbps)	t_{SIH}	8			ns	
9	STo Delay - Active to Active	t_{SOD}	8 11		30 43	ns	C_L=30pF C_L=200pF
10	Output Driver Enable (ODE) Delay	t_{ODE}			35	ns	R_L=1K, C_L=200pF, See Note 1
11	STo delay - Active to High-Z - High-Z to Active	t_{DZ}, t_{ZD}			35	ns	R_L=1K, C_L=200pF, See Note 1

Note: 1. High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L

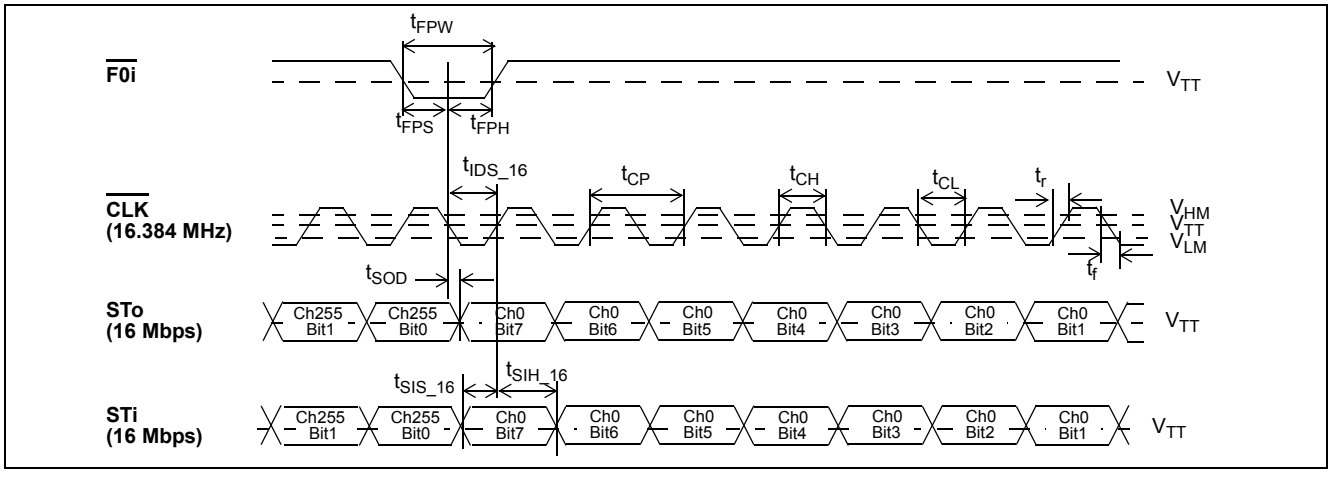


Figure 8 - ST-BUS Timing for Stream rate of 16.384 Mbps

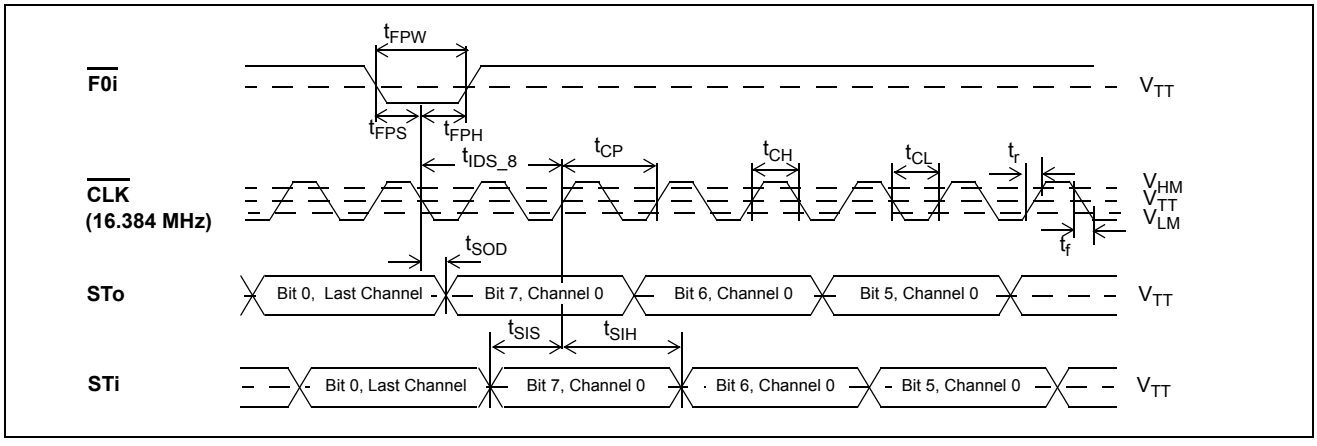


Figure 9 - ST-BUS Timing for Stream rate of 8.192 Mbps when $\overline{\text{CLK}}$ = 16.384 MHz

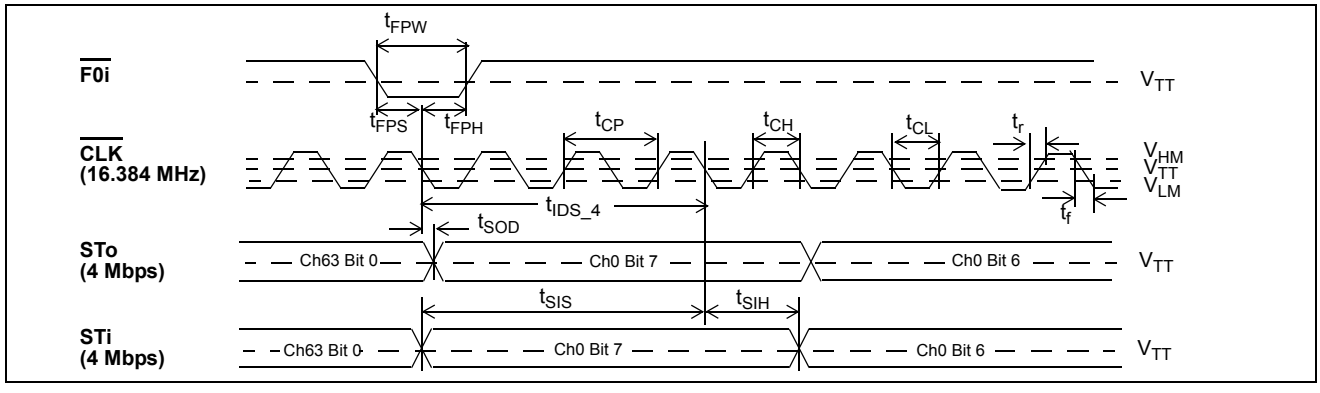


Figure 10 - ST-BUS Timing for Stream rate of 4.096 Mbps when $\overline{\text{CLK}}$ = 16.384 MHz

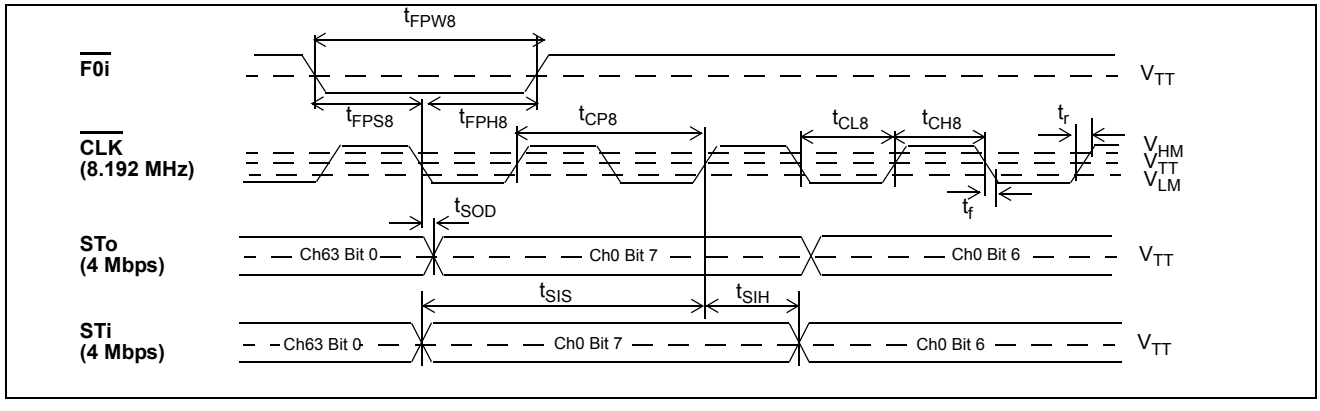


Figure 11 - ST-BUS Timing for Stream rate of 4.096 Mbps when $\overline{\text{CLK}}$ = 8.192 MHz

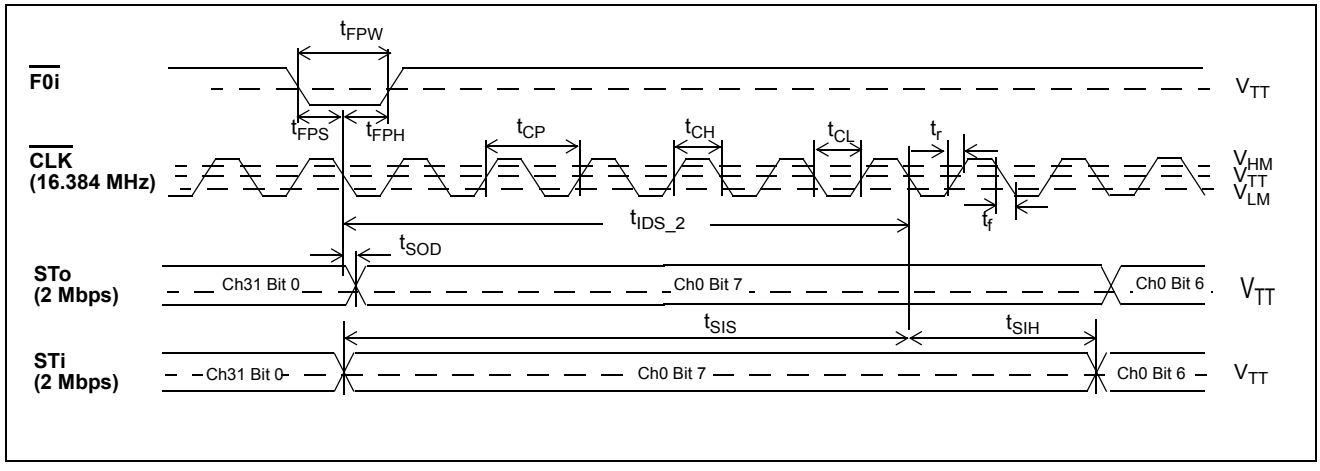


Figure 12 - ST-BUS Timing for Stream rate of 2.048 Mbps when CLK = 16.384 MHz

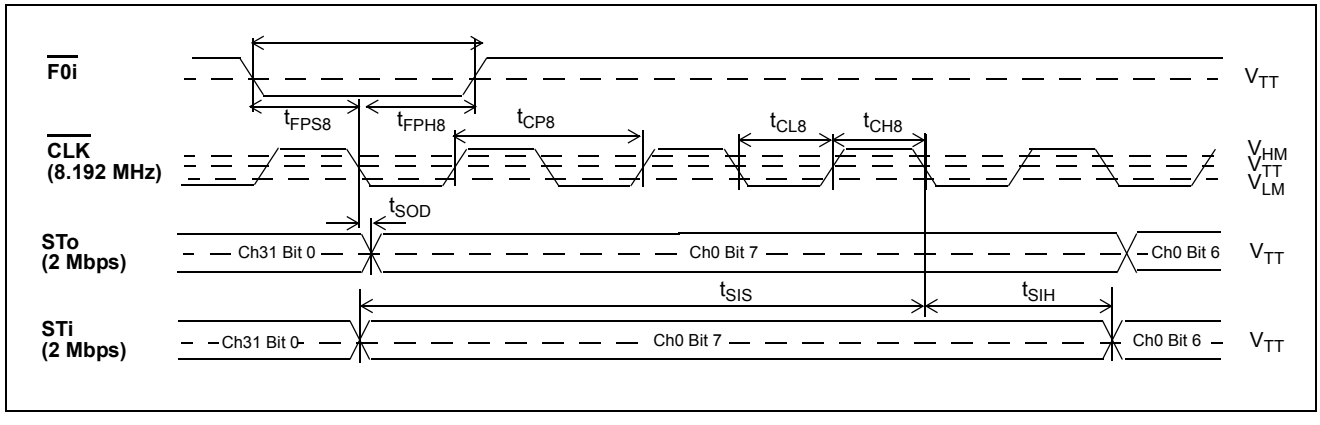


Figure 13 - -BUS Timing for Stream rate of 2.048 Mbps when CLK = 8.192 MHz

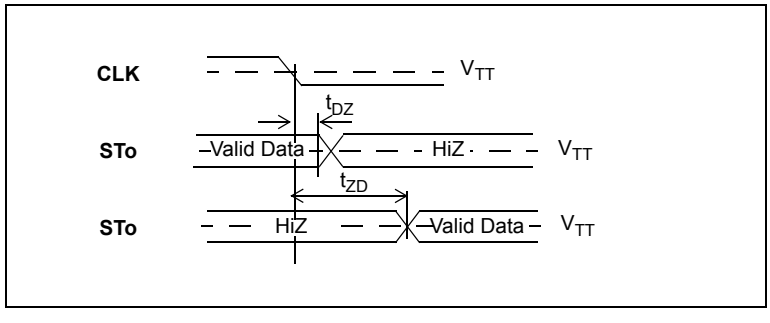


Figure 14 - Serial Output and External Control

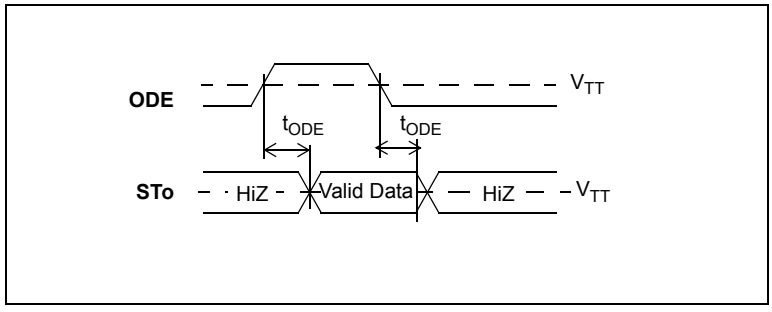


Figure 15 - Output Driver Enable (ODE)

AC Electrical Characteristics - Motorola Non-Multiplexed Bus Mode

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	$\overline{CS}$ setup from $\overline{DS}$ falling	t_{CSS}	0			ns	
2	R/$\overline{W}$ setup from $\overline{DS}$ falling	t_{RWS}	10			ns	
3	Address setup from $\overline{DS}$ falling	t_{ADS}	2			ns	
4	$\overline{CS}$ hold after $\overline{DS}$ rising	t_{CSH}	0			ns	
5	R/$\overline{W}$ hold after $\overline{DS}$ rising	t_{RWH}	2			ns	
6	Address hold after $\overline{DS}$ rising	t_{ADH}	10			ns	
7	Data setup from $\overline{DTA}$ Low on Read	t_{DDR}	27			ns	C_L=150pF
8	Data hold on read	t_{DHR}	12		20	ns	C_L=150pF, R_L=1K Note 1
9	Data setup on write (register write[2])	t_{DSW}	0			ns	
10	Valid Data Delay on write (memory write[3]) For 16 Mbps, 16&8 Mbps, 8 Mbps, 4&8 Mbps modes For 4 Mbps, 4&2 Mbps modes For 2 Mbps mode	t_{SWD}			 50 85 185	 ns ns ns	
11	Data hold on write	t_{DHW}	13			ns	
12a	Acknowledgment Delay: Register RD or WR	t_{AKD}			55	ns	C_L=150pF
12b	Acknowledgment Delay: Memory RD or WR For 16 Mbps, 16&8 Mbps, 8 Mbps, 4&8 Mbps modes For 4 Mbps, 4&2 Mbps modes For 2 Mbps mode	t_{AKD}			 100 140 240	 ns ns ns	C_L=150pF
13	Acknowledgment Hold Time	t_{AKH}			24	ns	C_L=150pF, R_L=1K, Note 1

Note:
1. High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.
2. Register write timing refers to the rising edge of $\overline{DS}$ at the end of the write cycle.
3. Memory write timing refers to the falling edge of $\overline{DS}$ at the beginning of the write cycle.

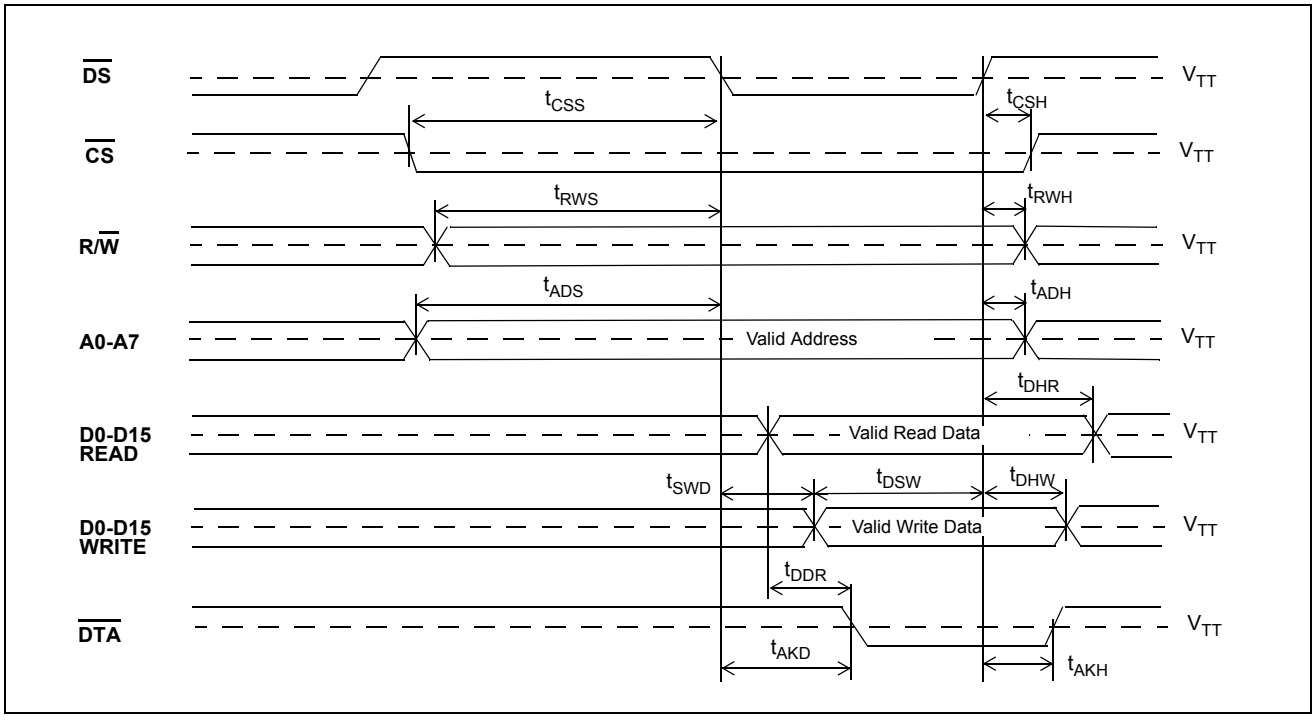
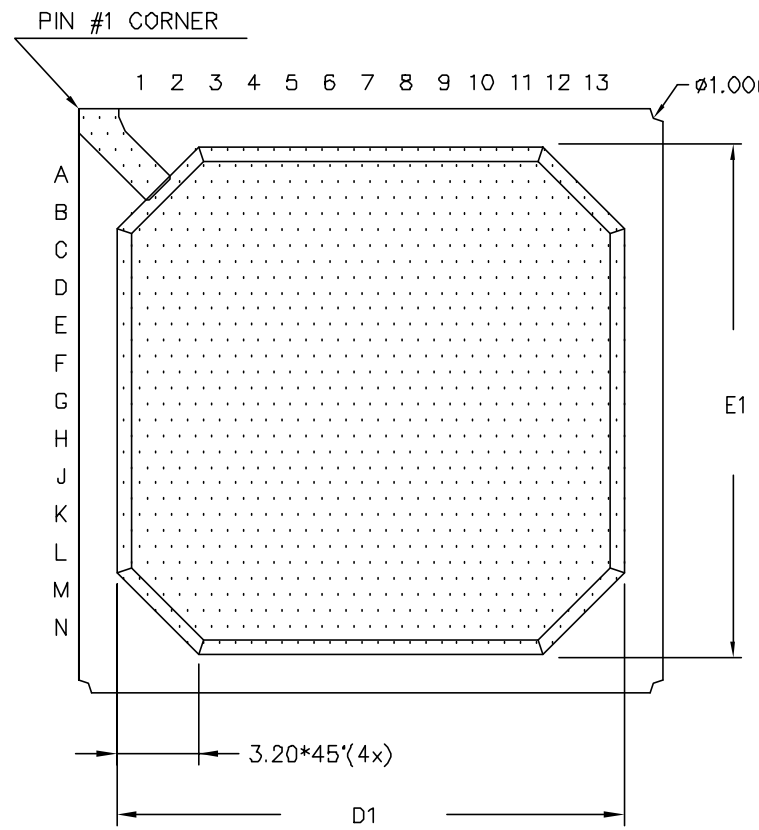
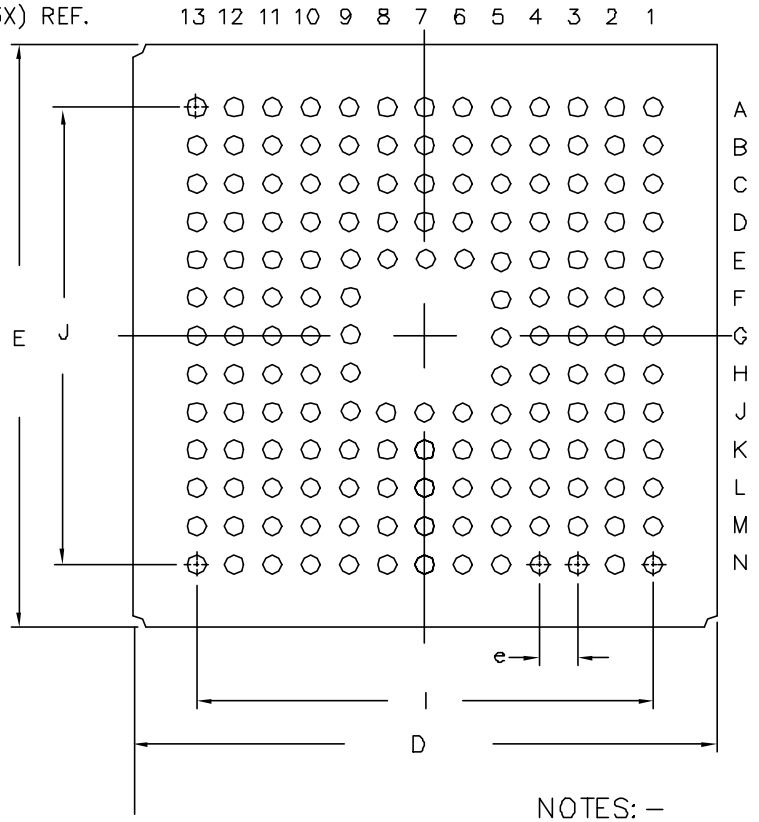


Figure 16 - Motorola Non-Multiplexed Bus Timing

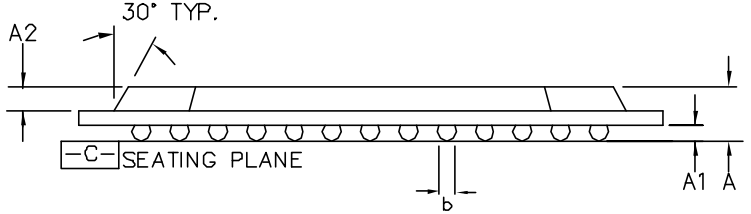
TOP VIEW



BOTTOM VIEW



DIMENSION	MIN	MAX
A	2.00	2.26
A1	0.50	0.70
A2	0.97 REF	
D	22.80	23.20
D1	20.00 REF	
E	22.80	23.20
E1	20.00 REF	
b	0.60	0.90
e	1.5	
N	160	
I	18.00	
J	18.00	
Substrate Layers: 2		
Reference spec: JEDEC MS-034		



SIDE VIEW

NOTES: –
1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crown of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.56 MM REF.

ISSUE	1			
ACN	213936			
DATE	20Jan03			
APPRD.				

ZARLINK SEMICONDUCTOR

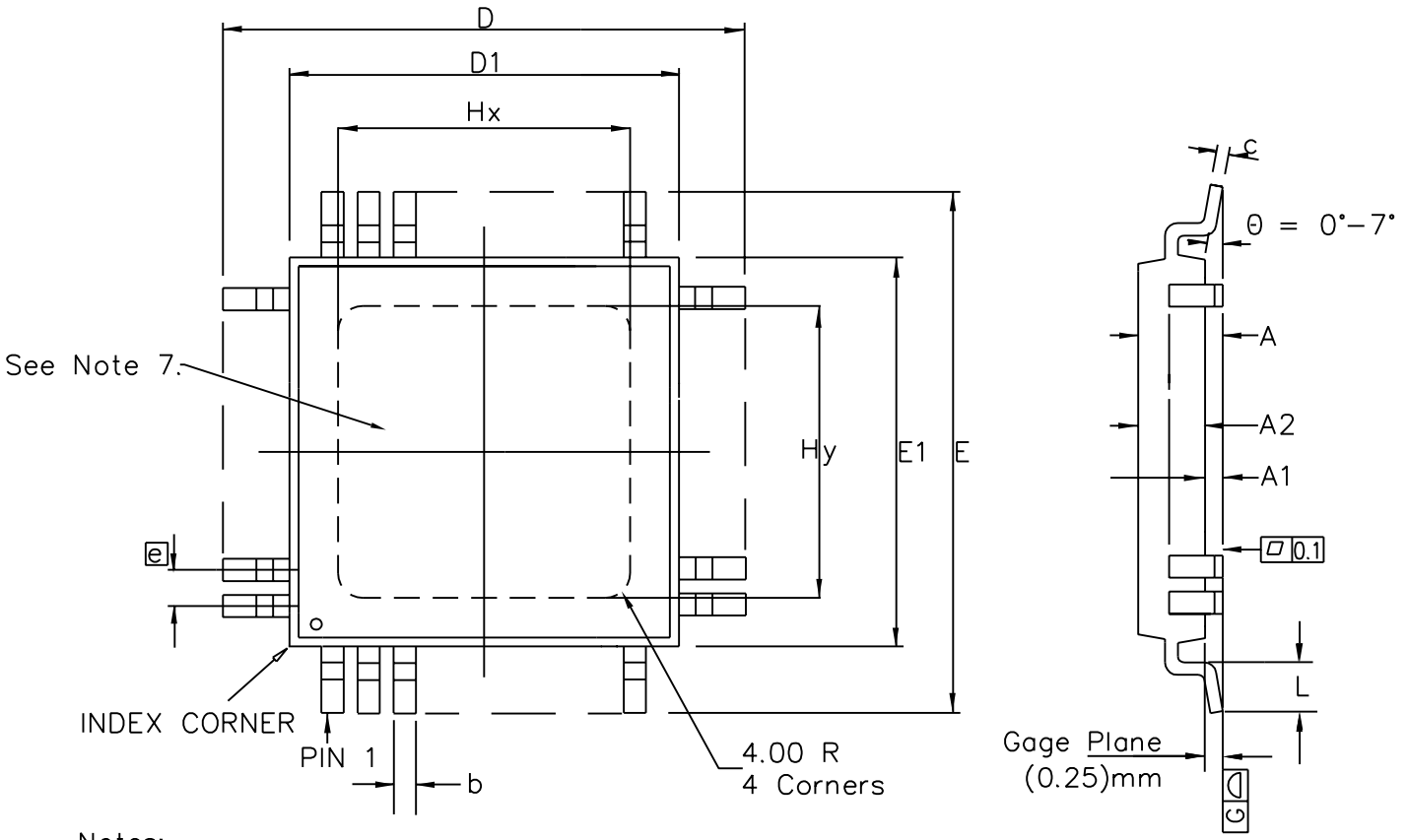
Previous package codes:

BP/G

Package Code : GA

Package Outline for
160Ball PBGA
23x23x2.13mm

GPD00822



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	–	4.10		–	0.161
A1	0.25	0.50		0.010	0.020
A2	3.20	3.60		0.126	0.142
D	31.20 BSC			1.228 BSC	
D1	28.00 BSC			1.102 BSC	
E	31.20 BSC			1.228 BSC	
E1	28.00 BSC			1.102 BSC	
Hx	21.00 REF.			0.827 REF.	
Hy	21.00 REF.			0.827 REF.	
L	0.73	1.03		0.029	0.041
e	0.65 BSC.			0.026 BSC.	
b	0.22	0.40		0.009	0.016
c	0.11	0.23		0.004	0.009
	Pin features				
N	160				
ND	40				
NE	40				
NOTE	SQUARE				

Conforms to JEDEC MS-022 DD-1 Iss. B

Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.20 mm.
4. Dimension D1 and E1 do not include mould protrusion.
5. Dimension b does not include dambar protrusion.
6. Coplanarity, measured at seating plane G, to be 0.10 mm max.
7. Dashed area represents Heat Sink – Relevant to PowerQuad Packages only. Finish = Ni, min. 1.27um thick.

ISSUE	1	2	3	4
ACN	202051	207067	209116	213268
DATE	20Feb97	1Jul99	30Jun00	15Aug02
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

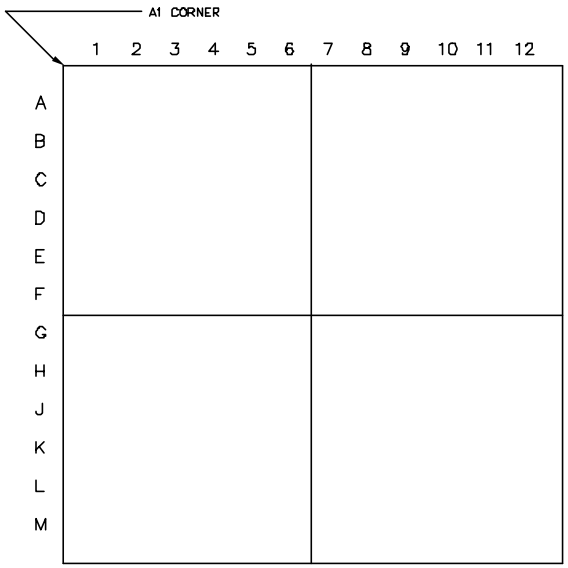
GP / L

Package Code QB

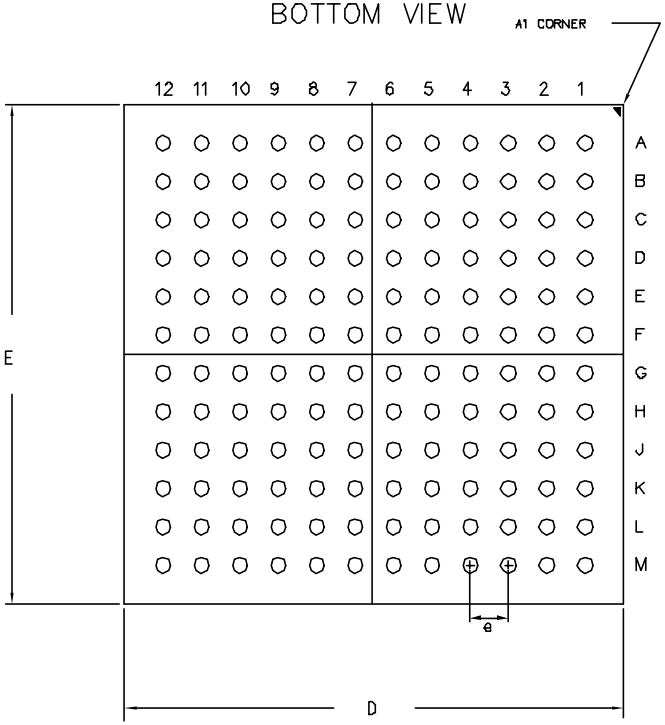
Package Outline for 160 lead MQFP & PQuad2 – stnd. (28x28x3.4mm) 3.2mm Footprint

GPD00302

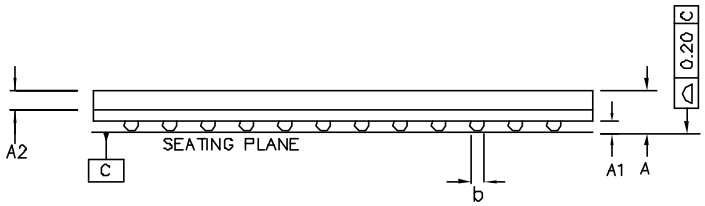
TOP VIEW



BOTTOM VIEW



DIMENSION	MIN	MAX
A	–	1.25
A1	0.25	0.35
A2	0.53 REF	
D	12.95	13.05
E	12.95	13.05
b	0.35	0.45
e	1.00	
N	144	
Conforms to JEDEC MO-192		



SIDE VIEW

NOTES: –
1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crown of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.36 MM.

ISSUE	1	2		
ACN	213740	213834		
DATE	15Nov02	11Dec02		
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

Package Code GD

Package Outline for
144Ball LBGA
13x13x1.25mm

GPD00805

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TECHNICAL DOCUMENTATION - NOT FOR RESALE