STH272N6F7-6AG

Automotive-grade N-channel 60 V, 0.95 mΩ typ., 180 A STripFET™ F7 Power MOSFET in H²PAK-6 package

Datasheet - production data

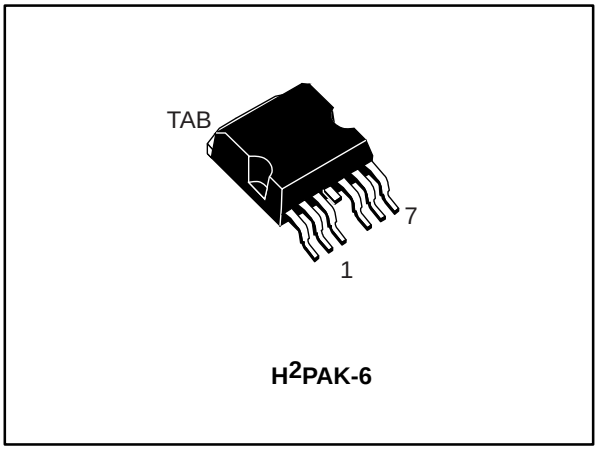
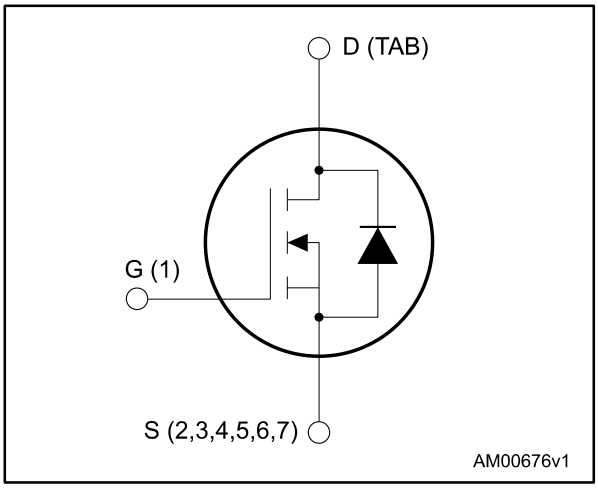


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STH272N6F7-6AG	60 V	1.5 mΩ	180 A

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STH272N6F7-6AG	272N6F7	H²PAK-6	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	±20	V
I_D(1)	Drain current (continuous) at T_{case} = 25 °C	180	A
	Drain current (continuous) at T_{case} = 100 °C	180	
I_{DM}(2)	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	333	W
E_{AS}(3)	Single pulse avalanche energy	1.9	J
T_{stg}	Storage temperature range	-55 to 175	°C
T_j	Operating junction temperature range		

Notes:

(1) Current is limited by package, the current capability of the silicon is 346 A at 25 °C.

(2) Pulse width is limited by safe operating area.

(3) $T_j \leq 175$ °C, I_{AV}=90A

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.45	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	35	

Notes:

(1) When mounted on a 1-inch² FR-4 board, 2oz Cu.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 60 V			10	µA
		V_{GS} = 0 V, V_{DS} = 60 V, T_{case} = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 90 A		0.95	1.5	mΩ

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	11000	-	pF
C_{oss}	Output capacitance		-	4870	-	
C_{rss}	Reverse transfer capacitance		-	220	-	
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 180 A, V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	170	-	nC
Q_{gs}	Gate-source charge		-	65	-	
Q_{gd}	Gate-drain charge		-	57	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 90 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"*)	-	55	-	ns
t_r	Rise time		-	390	-	
$t_{d(off)}$	Turn-off delay time		-	146	-	
t_f	Fall time		-	96	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		180	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 90 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 180 A, di/dt = 100 A/µs, V_{DD} = 48 V, T_j = 25 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	85.5		ns
Q_{rr}	Reverse recovery charge		-	163		nC
I_{RRM}	Reverse recovery current		-	3.8		A

Notes:

(1) Current is limited by package, the current capability of the silicon is 346 A at 25 °C

(2) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

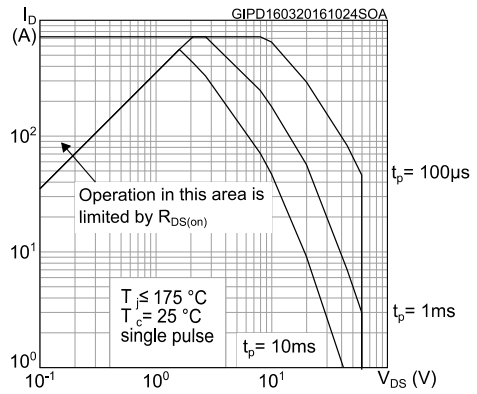


Figure 3: Thermal impedance

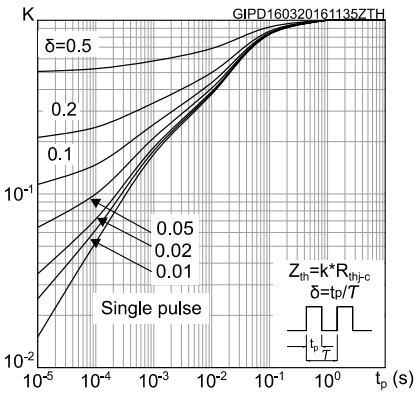


Figure 4: Output characteristics

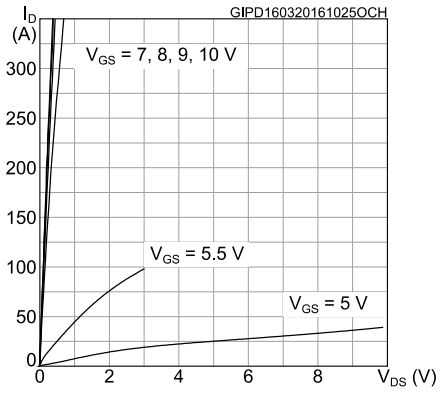


Figure 5: Transfer characteristics

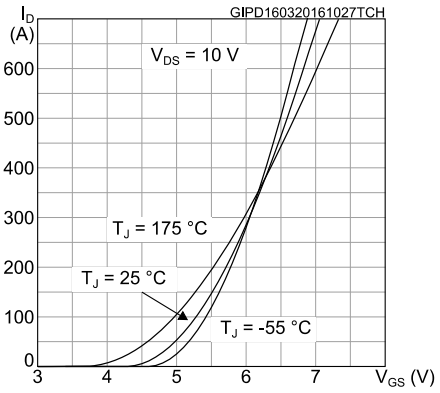


Figure 6: Gate charge vs gate-source voltage

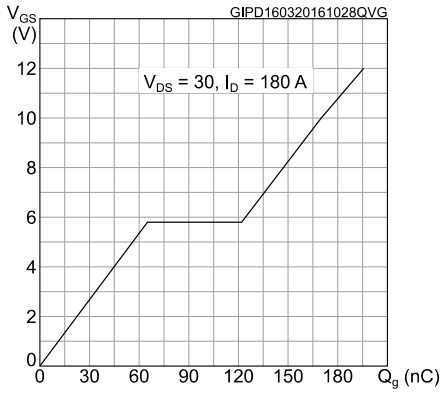


Figure 7: Static drain-source on-resistance

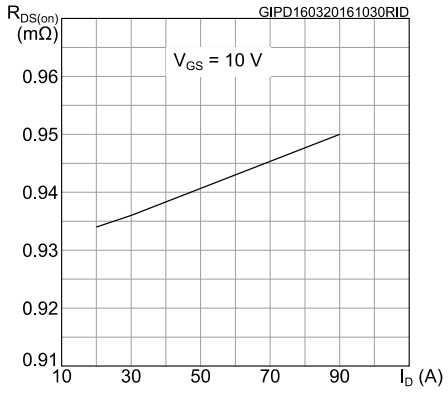


Figure 8: Capacitance variations

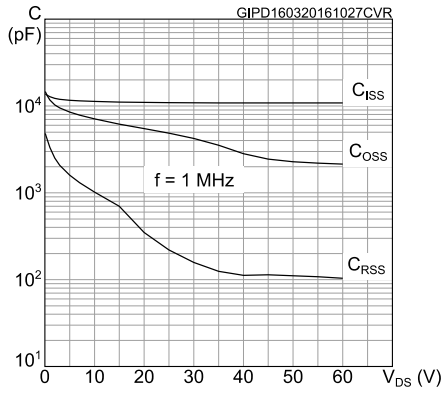


Figure 9: Normalized gate threshold voltage vs temperature

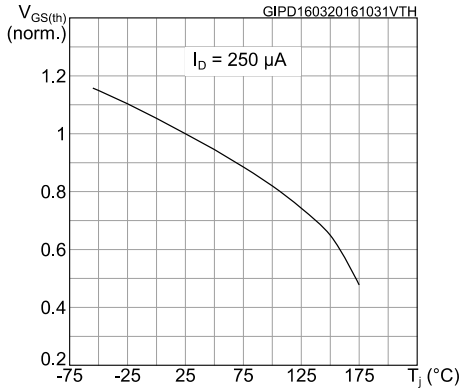


Figure 10: Normalized on-resistance vs temperature

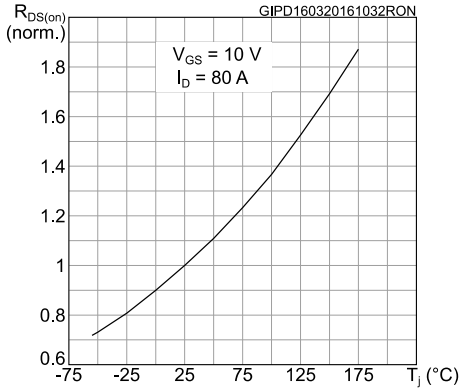


Figure 11: Normalized V(BR)DSS vs temperature

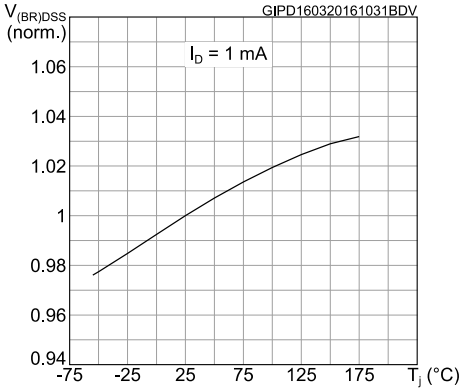
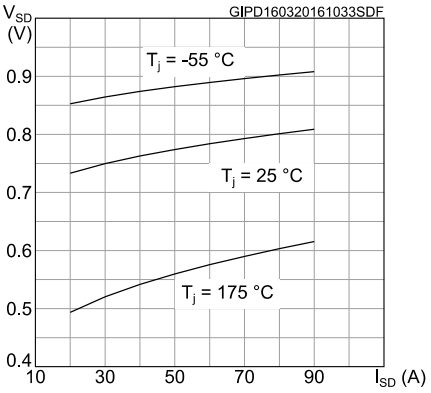


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

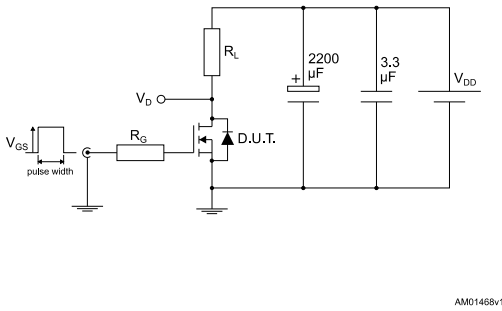


Figure 14: Test circuit for gate charge behavior

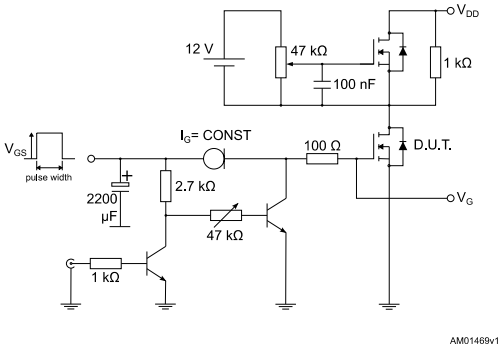


Figure 15: Test circuit for inductive load switching and diode recovery times

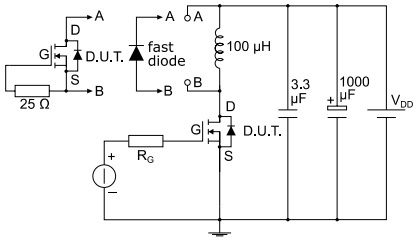


Figure 16: Unclamped inductive load test circuit

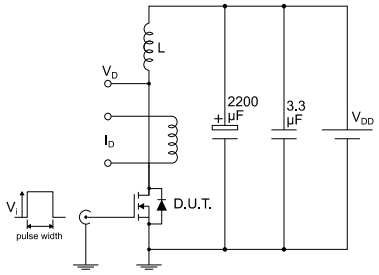


Figure 17: Unclamped inductive waveform

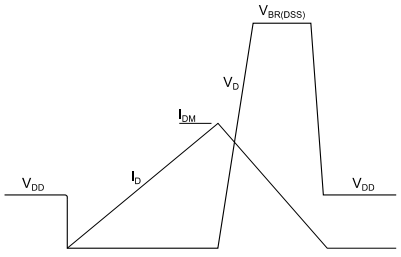
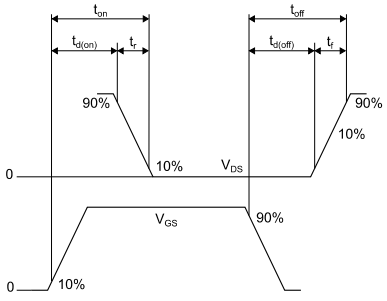


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 H²PAK-6 package mechanical data

Figure 19: H²PAK-6 package outline

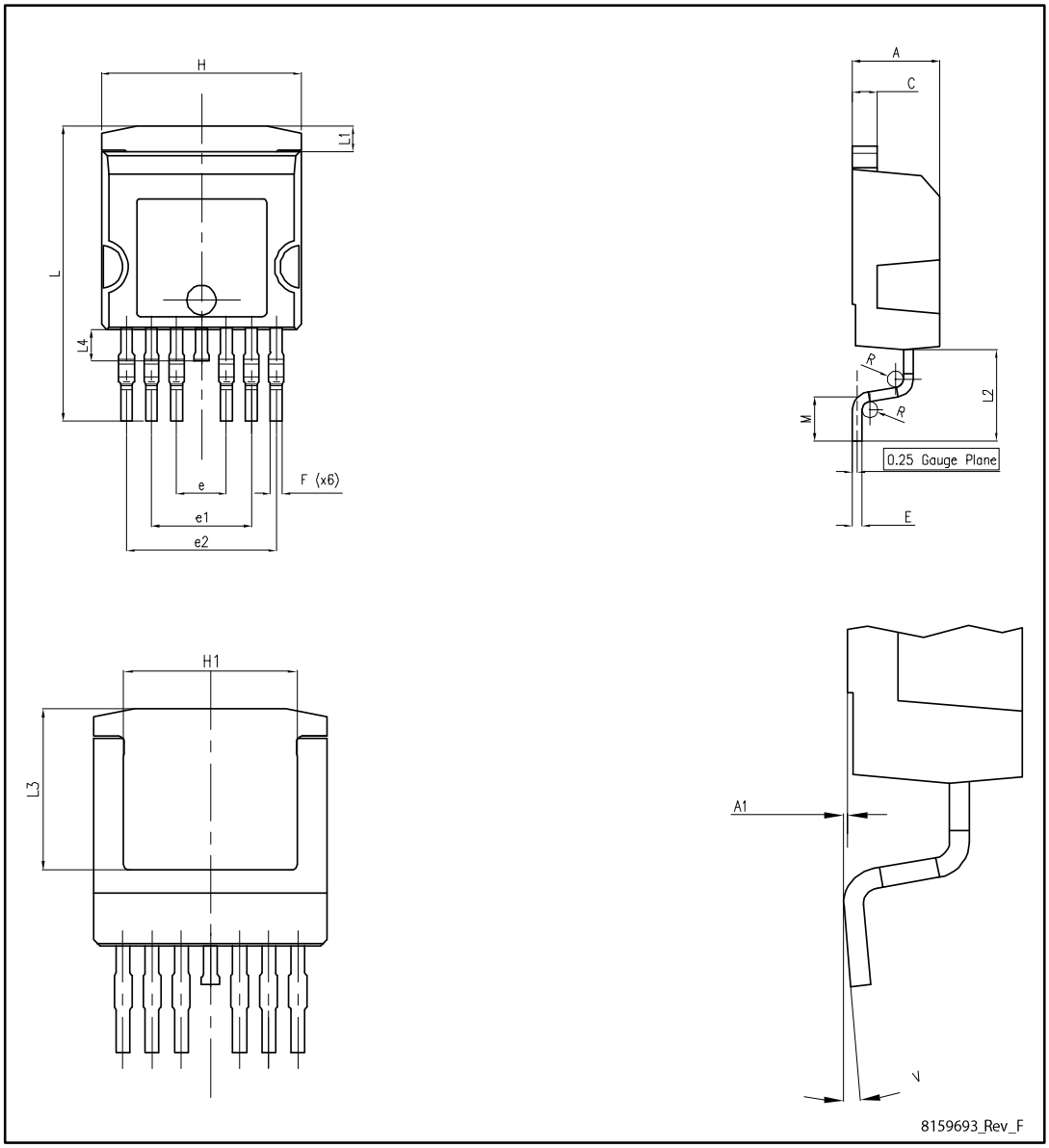
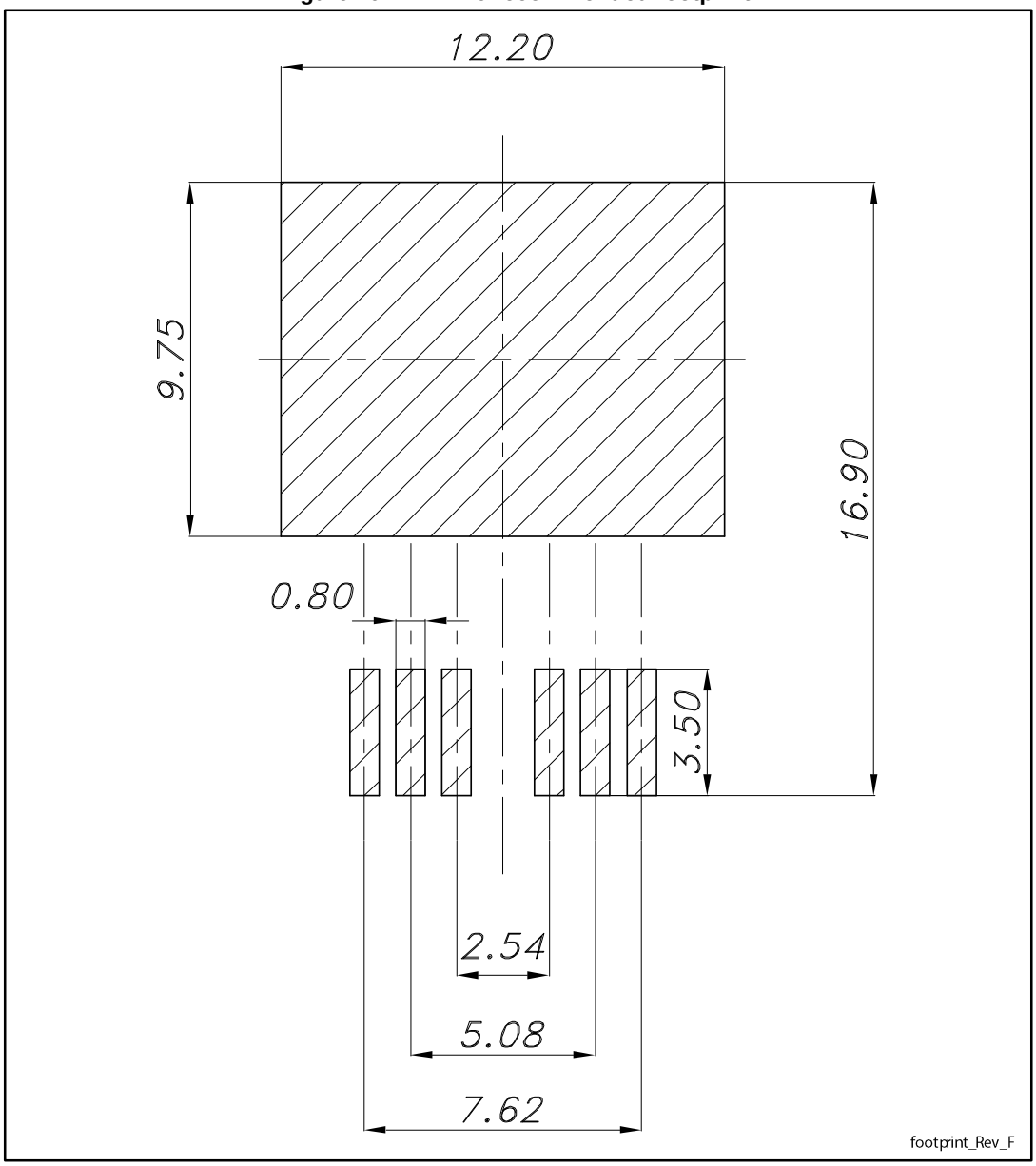


Table 8: H²PAK-6 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.80
A1	0.03		0.20
C	1.17		1.37
e	2.34		2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.5		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 20: H²PAK-6 recommended footprint



Dimensions are in mm.

4.2 H²PAK-6 packing information

Figure 21: Tape outline

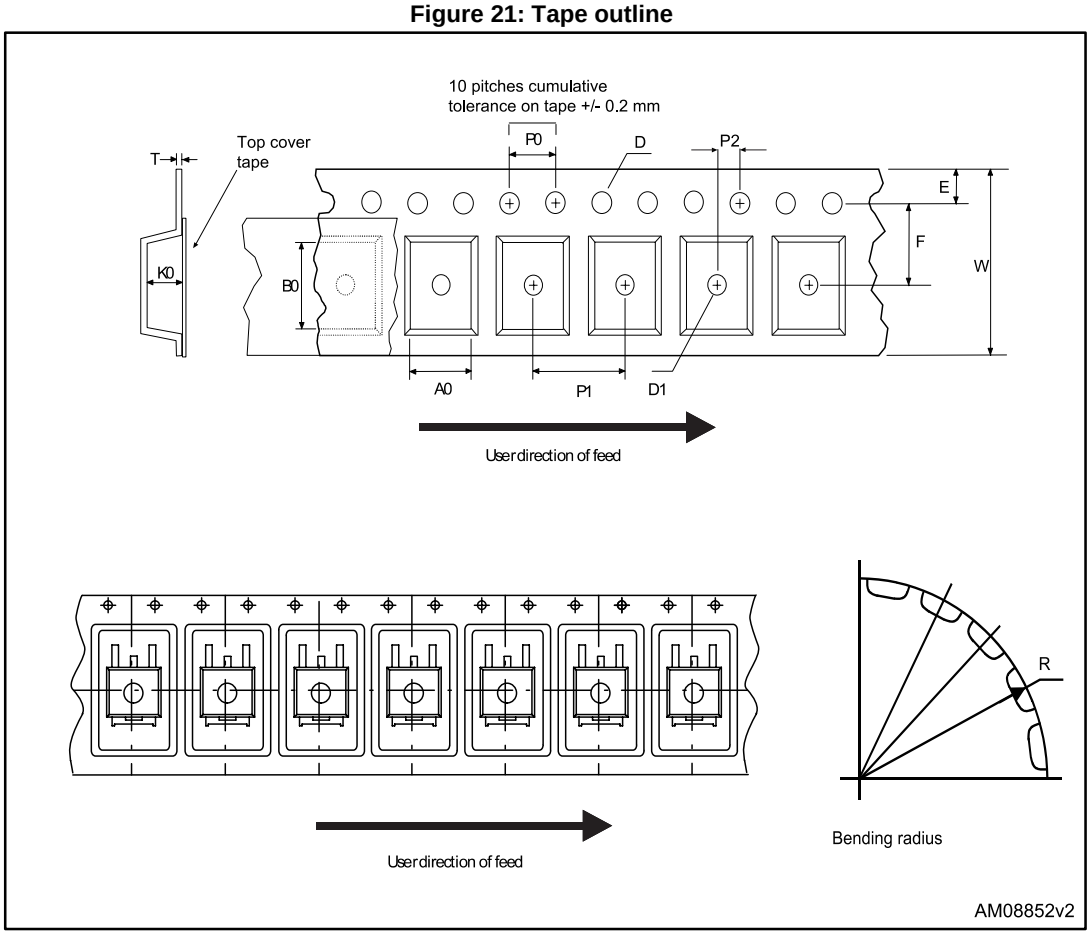


Figure 22: Reel outline

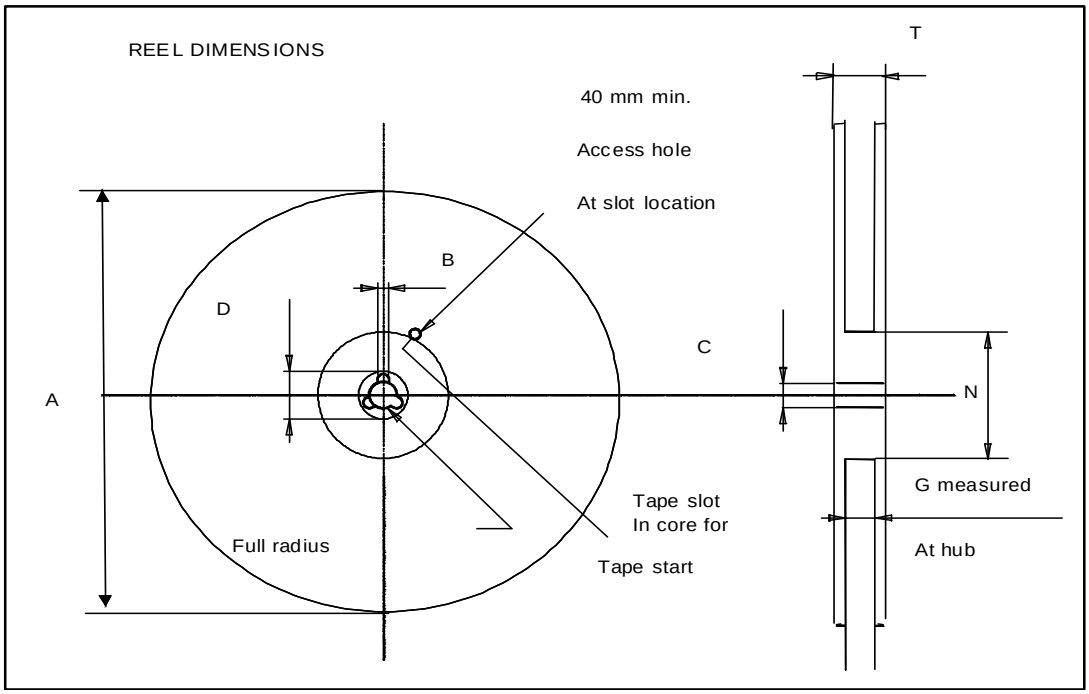


Table 9: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
17-Mar-2016	1	First release.

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