

LC717A00AR

Capacitance-Digital-Converter LSI for Electrostatic Capacitive Touch Sensors

Overview

The LC717A00AR is a high-performance, low-cost capacitance-digital-converter LSI for electrostatic capacitive touch sensor, especially focused on usability. It has 8 channels capacitance-sensor input. The built-in logic circuit can detect the state (ON/OFF) of each input and output the result. This makes it ideal for various switch applications.

The calibration function is automatically performed by the built-in logic circuit during power activation or whenever there are environmental changes. In addition, since initial settings of parameters, such as gain, are configured, LC717A00AR can operate as stand-alone when the recommended switch pattern is applied.

Also, since LC717A00AR has a serial interface compatible with I²C™ and SPI bus, parameters can be adjusted using external devices whenever necessary. Moreover, outputs of the 8-input capacitance data can be detected and measured as 8-bit data.

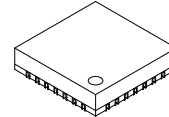
Features

- Detection System: Differential Capacitance Detection (Mutual Capacitance Type)
- Input Capacitance Resolution: Can Detect Capacitance Changes in the Femto Farad Order
- Measurement Interval (8 Differential Inputs):
 - ◆ 18 ms (Typ) (at Initial Configuration)
 - ◆ 3 ms (Typ) (at Minimum Interval Configuration)
- External Components for Measurement: Not Required
- Current Consumption:
 - ◆ 320 μA (Typ) (V_{DD} = 2.8 V)
 - ◆ 740 μA (Typ) (V_{DD} = 5.5 V)
- Supply Voltage: 2.6 V to 5.5 V
- Detection Operations: Switch
- Packages: VCT28
- Interface: I²C Compatible Bus or SPI Selectable



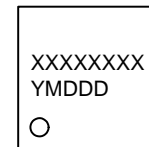
ON Semiconductor®

www.onsemi.com



VCT28
CASE 601AE

MARKING DIAGRAM



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

LC717A00AR

Specifications

Table 1. ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Ratings | Unit | Remarks |
|----------------------|--------------------|------------------------|------------------|--------------------------------------------------------------|
| Supply Voltage | V_{DD} | -0.3 to +6.5 | V | |
| Input Voltage | V_{IN} | -0.3 to $V_{DD} + 0.3$ | V | (Note 1) |
| Output Voltage | V_{OUT} | -0.3 to $V_{DD} + 0.3$ | V | (Note 2) |
| Power Dissipation | $P_{d\text{ max}}$ | 160 | mW | $T_A = +105^\circ\text{C}$, Mounted on a substrate (Note 3) |
| Peak Output Current | I_{OP} | ± 8 | mA | Per terminal, 50% Duty ratio (Note 2) |
| Total Output Current | I_{OA} | ± 40 | mA | Output total value of LSI, 25% Duty ratio |
| Storage Temperature | T_{stg} | -55 to +125 | $^\circ\text{C}$ | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Apply to C_{in0} to 7, C_{ref} , $nRST$, SCL , SDA , SA , SCK , SI , nCS , $GAIN$.
2. Apply to C_{drv} , P_{out0} to 7, SDA , SO , $ERROR$, $INTOUT$.
3. 4-layer glass epoxy board ($40 \times 50 \times 0.8\text{ mm}$).

Table 2. RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | Remarks |
|--------------------------|-----------|------------|-----|-----|----------|------------------|----------|
| Operating Supply Voltage | V_{DD} | | 2.6 | - | 5.5 | V | |
| Supply Ripple + Noise | V_{PP} | | - | - | ± 20 | mV | (Note 4) |
| Operating Temperature | T_{opr} | | -40 | 25 | 105 | $^\circ\text{C}$ | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Inserting a high-valued capacitor and a low-valued capacitor in parallel between V_{DD} and V_{SS} is recommended. In this case, the small-valued capacitor should be at least $0.1\ \mu\text{F}$, and is mounted near the LSI.

Table 3. ELECTRICAL CHARACTERISTICS

($V_{SS} = 0\text{ V}$, $V_{DD} = 2.6$ to 5.5 V , $T_A = -40$ to $+105^\circ\text{C}$, Unless otherwise specified, the C_{drv} drive frequency is $f_{CDRV} = 143\text{ kHz}$.)

Not tested at low temperature before shipment.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | Remarks |
|---------------------------------------------------|----------------|---------------------------|------|-----------|-----------|---------------|--------------|
| Capacitance Detection Resolution | N | | - | - | 8 | bit | |
| Output Noise RMS | N_{RMS} | Minimum gain setting | - | - | ± 1.0 | LSB | (Notes 5, 7) |
| Input Offset Capacitance Adjustment Range | $C_{offRANGE}$ | | - | ± 8.0 | - | pF | (Notes 5, 7) |
| Input Offset Capacitance Adjustment Resolution | $C_{offRESO}$ | | - | 8 | - | bit | |
| C_{in} Offset Drift | $C_{inDRIFT}$ | Minimum gain setting | - | - | ± 8 | LSB | (Note 5) |
| C_{in} Detection Sensitivity | $C_{inSENSE}$ | Minimum gain setting | 0.04 | - | 0.12 | LSB/fF | (Note 6) |
| C_{in} Pin Leak Current | I_{Cin} | $C_{in} = Hi-Z$ | - | ± 25 | ± 500 | nA | |
| C_{in} Allowable Parasitic Input Capacitance | C_{inSUB} | C_{in} against V_{SS} | - | - | 30 | pF | (Notes 5, 7) |
| C_{drv} Drive Frequency | f_{CDRV} | | 100 | 143 | 186 | kHz | |
| C_{drv} Pin Leak Current | I_{CDRV} | $C_{drv} = Hi-Z$ | - | ± 25 | ± 500 | nA | |
| $nRST$ Minimum Pulse Width | t_{NRST} | | 1 | - | - | μs | |
| Power-on Reset Time | t_{POR} | | - | - | 20 | ms | |
| Power-on Reset Operation Condition: Hold Time | t_{POROP} | | 10 | - | - | ms | (Note 5) |
| Power-on Reset Operation Condition: Input Voltage | V_{POROP} | | - | - | 0.1 | V | (Note 5) |

LC717A00AR

Table 3. ELECTRICAL CHARACTERISTICS (continued)

($V_{SS} = 0\text{ V}$, $V_{DD} = 2.6\text{ to }5.5\text{ V}$, $T_A = -40\text{ to }+105^\circ\text{C}$, Unless otherwise specified, the Cdrv drive frequency is $f_{CDRV} = 143\text{ kHz}$.
Not tested at low temperature before shipment.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | Remarks |
|---------------------------------------------------------------|-----------------|-------------------------------------------------------------------------------|--------------|-----|--------------|---------------|--------------|
| Power-on Reset Operation Condition: Power Supply Rise Rate | t_{VDD} | 0 V to V_{DD} | 1 | – | – | V/ms | (Note 5) |
| Pin Input Voltage | V_{IH} | High input | $0.8 V_{DD}$ | – | – | V | (Notes 5, 8) |
| | V_{IL} | Low input | – | – | $0.2 V_{DD}$ | | |
| Pin Output Voltage | V_{OH} | High output ($I_{OH} = +3\text{ mA}$) | $0.8 V_{DD}$ | – | – | V | (Note 9) |
| | V_{OL} | Low output ($I_{OL} = -3\text{ mA}$) | – | – | $0.2 V_{DD}$ | | |
| SDA Pin Output Voltage | $V_{OL}^{I^2C}$ | SDA Low output ($I_{OL} = -3\text{ mA}$) | – | – | 0.4 | V | |
| Pin Leak Current | I_{LEAK} | | – | – | ± 1 | μA | (Note 10) |
| Current Consumption | I_{DD} | When stand-alone configuration and non-touch $V_{DD} = 2.8\text{ V}$ | – | 320 | 390 | μA | (Notes 5, 7) |
| | | When stand-alone configuration and non-touch $V_{DD} = 5.5\text{ V}$ | – | 740 | 900 | | |
| | I_{STBY} | During Sleep process | – | – | 1 | μA | (Note 7) |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Design-guaranteed values (not tested before shipment).
6. Measurements conducted using the test mode in the LSI.
7. $T_A = +25^\circ\text{C}$.
8. Apply to nRST, SCL, SDA, SA, SCK, SI, nCS, GAIN.
9. Apply to Cdrv, Pout0 to 7, SO, ERROR, INTOUT.
10. Apply to nRST, SCL, SDA, SA, SCK, SI, nCS, GAIN.

LC717A00AR

Table 4. I²C COMPATIBLE BUS TIMING CHARACTERISTICS

(V_{SS} = 0 V, V_{DD} = 2.6 to 5.5 V, T_A = -40 to +105°C, Not tested at low temperature before shipment.)

| Parameter | Symbol | Pin Name | Conditions | Min | Typ | Max | Unit | Remarks |
|-------------------------------------|---------------------------------|----------|------------|-----|-----|-----|------|-----------|
| SCL Clock Frequency | f _{SCL} | SCL | | – | – | 400 | kHz | |
| START Condition Hold Time | t _{HD;STA} | SCL, SDA | | 0.6 | – | – | μs | |
| SCL Clock Low Period | t _{LOW} | SCL | | 1.3 | – | – | μs | |
| SCL Clock High Period | t _{HIGH} | SCL | | 0.6 | – | – | μs | |
| Repeated START Condition Setup Time | t _{SU;STA} | SCL, SDA | | 0.6 | – | – | μs | (Note 11) |
| Data Hold Time | t _{HD;DAT} | SCL, SDA | | 0 | – | 0.9 | μs | |
| Data Setup Time | t _{SU;DAT} | SCL, SDA | | 100 | – | – | ns | (Note 11) |
| SDA, SCL Rise/Fall Time | t _r / t _f | SCL, SDA | | – | – | 300 | ns | (Note 11) |
| STOP Condition Setup Time | t _{SU;STO} | SCL, SDA | | 0.6 | – | – | μs | |
| STOP-to-START Bus Release Time | t _{BUF} | SCL, SDA | | 1.3 | – | – | μs | (Note 11) |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

11. Design-guaranteed values (not tested before shipment).

Table 5. SPI BUS TIMING CHARACTERISTICS

(V_{SS} = 0 V, V_{DD} = 2.6 to 5.5 V, T_A = -40 to +105°C, Not tested at low temperature before shipment.)

| Parameter | Symbol | Pin Name | Conditions | Min | Typ | Max | Unit | Remarks |
|------------------------------------------|---------------------------------|--------------|------------|-----|-----|-----|------|-----------|
| SCK Clock Frequency | f _{SCK} | SCK | | – | – | 5 | MHz | |
| SCK Clock Low Time | t _{LOW} | SCK | | 90 | – | – | ns | (Note 12) |
| SCK Clock High Time | t _{HIGH} | SCK | | 90 | – | – | ns | (Note 12) |
| Input Signal Rise/Fall Time | t _r / t _f | nCS, SCK, SI | | – | – | 300 | ns | (Note 12) |
| nCS Setup Time | t _{SU;NCS} | nCS, SCK | | 90 | – | – | ns | (Note 12) |
| SCK Clock Setup Time | t _{SU;SCK} | nCS, SCK | | 90 | – | – | ns | (Note 12) |
| Data Setup Time | t _{SU;SI} | SCK, SI | | 20 | – | – | ns | (Note 12) |
| Data Hold Time | t _{HD;SI} | SCK, SI | | 30 | – | – | ns | (Note 12) |
| nCS Hold Time | t _{HD;NCS} | nCS, SCK | | 90 | – | – | ns | (Note 12) |
| SCK Clock Hold Time | t _{HD;SCK} | nCS, SCK | | 90 | – | – | ns | (Note 12) |
| nCS Standby Pulse Width | t _{CPH} | nCS | | 90 | – | – | ns | (Note 12) |
| Output High Impedance Time from nCS | t _{CHZ} | nCS, SO | | – | – | 80 | ns | (Note 12) |
| Output Data Determination Time | t _v | SCK, SO | | – | – | 80 | ns | (Note 12) |
| Output Data Hold Time | t _{HD;SO} | SCK, SO | | 0 | – | – | ns | (Note 12) |
| Output Low Impedance Time from SCK Clock | t _{CLZ} | SCK, SO | | 0 | – | – | ns | (Note 12) |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

12. Design-guaranteed values (not tested before shipment).

LC717A00AR

Power-On Reset (POR)

When power is turned on, power-on reset is enabled inside the LSI and its state is released after a certain power-on reset time, t_{POR} . Power-on reset operation condition: Power supply rise rate t_{VDD} must be at least 1 V/ms.

Since INTOUT pin changes from “High” to “Low” at the same time as the released of power-on reset state, it is possible to verify the t_{POR} externally.

During power-on reset state, C_{in} , C_{ref} and P_{out} are unknown.

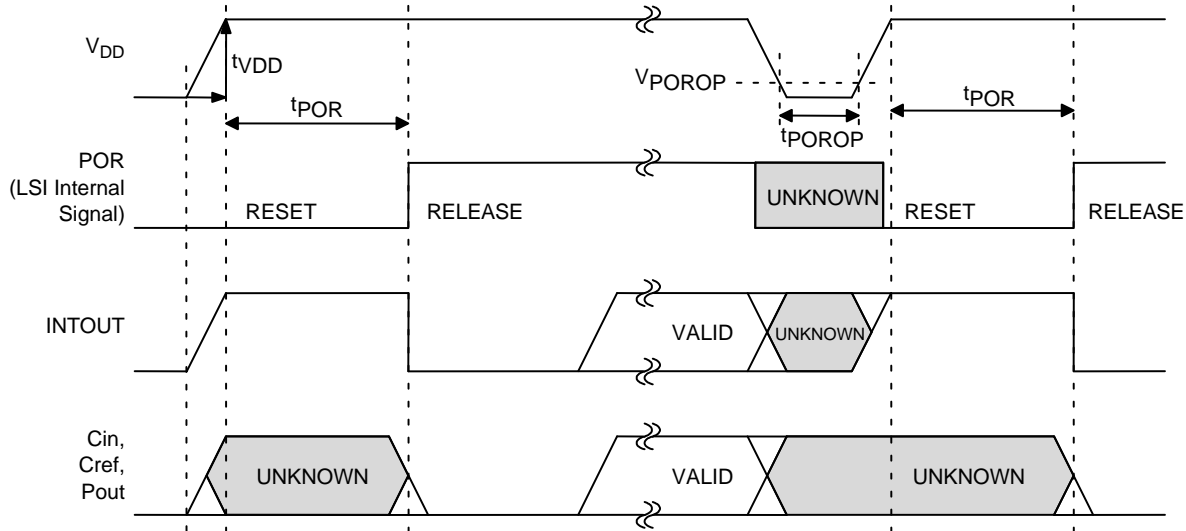


Figure 1.

I²C Compatible Bus Data Timing

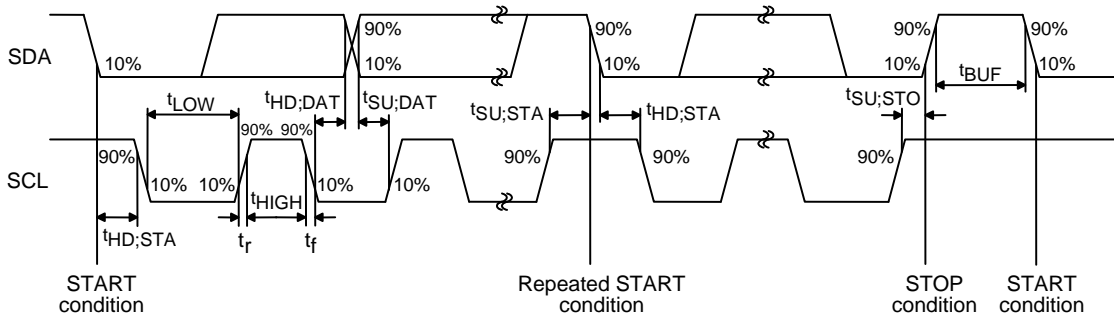


Figure 2.

I²C Compatible Bus Communication Formats

- Write format (data can be written into sequentially incremented addresses)



Figure 3.

- Read format (data can be read from sequentially incremented addresses)



Figure 4.

LC717A00AR

I²C Compatible Bus Slave Address

Selection of two kinds of addresses is possible through the SA terminal.

Table 6.

| SA Pin Input | 7-bit Slave Address | Binary Notation | 8-bit Slave Address |
|--------------|---------------------|-------------------|---------------------|
| Low | 0x16 | 00101100b (Write) | 0x2C |
| | | 00101101b (Read) | 0x2D |
| High | 0x17 | 00101110b (Write) | 0x2E |
| | | 00101111b (Read) | 0x2F |

SPI Data Timing (SPI Mode 0 / Mode 3)

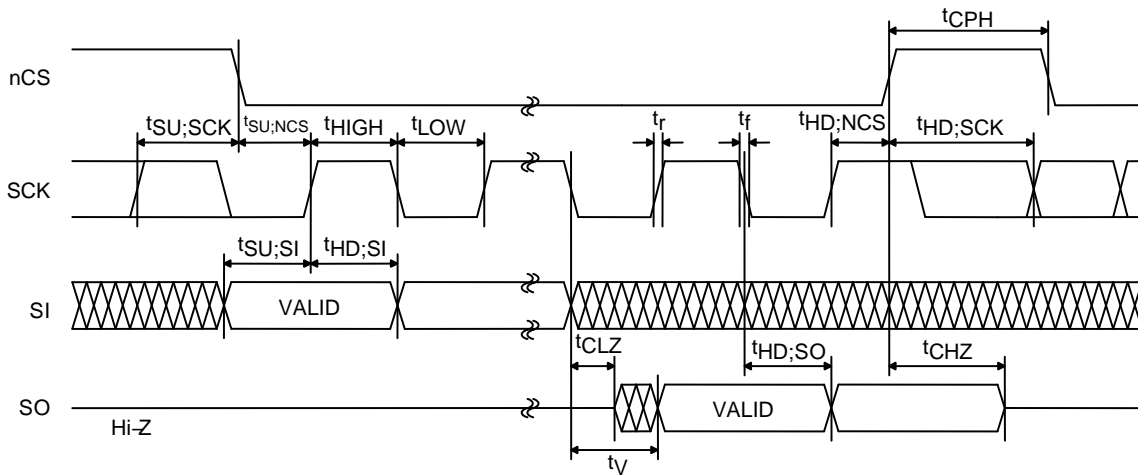


Figure 5.

SPI Communication Formats (Example of Mode 0)

- Write format (data can be written into sequentially incremented addresses while holding nCS = L)

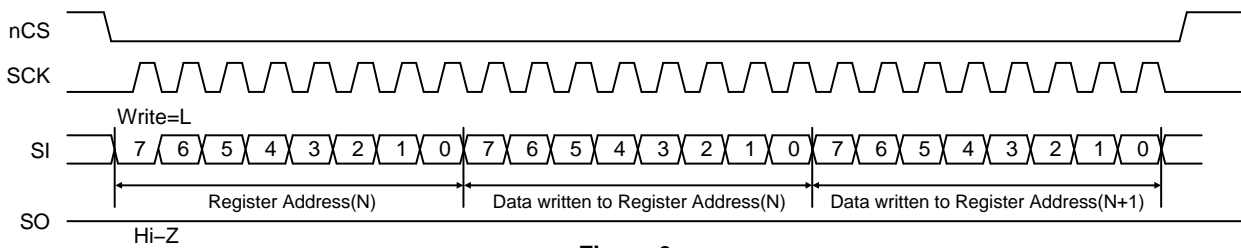


Figure 6.

- Read format (data can be read from sequentially incremented addresses while holding nCS = L)

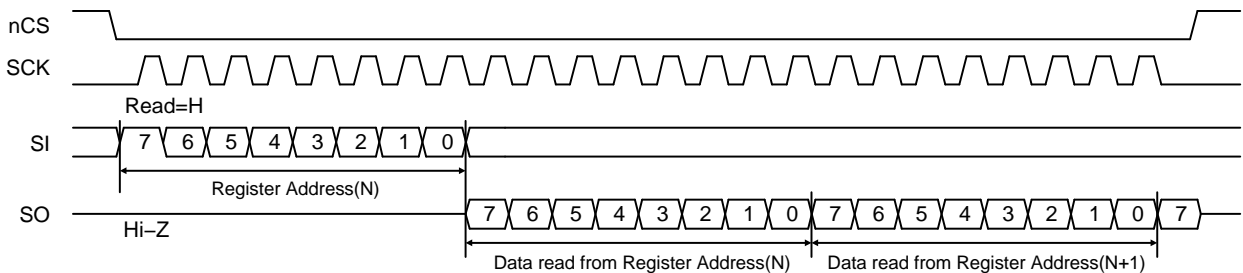


Figure 7.

LC717A00AR

Block Diagram

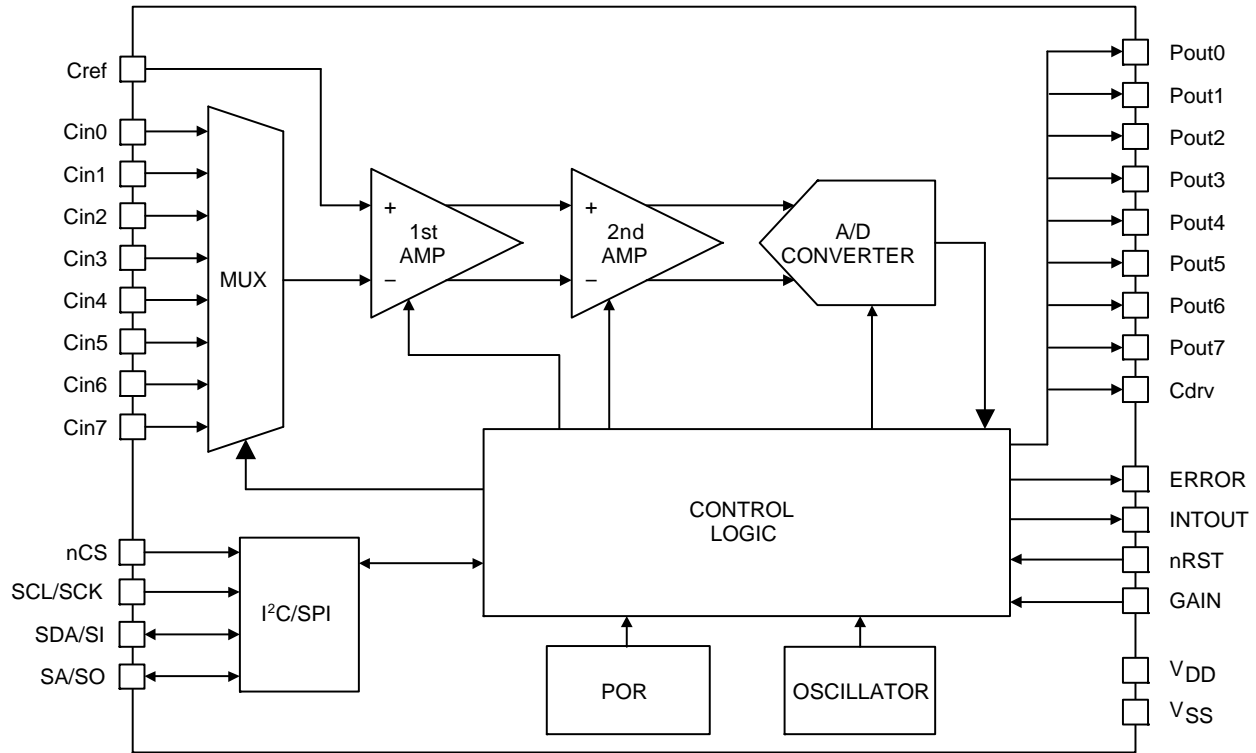


Figure 8. Block Diagram

LC717A00AR is capacitance-digital-converter LSI capable of detecting changes in capacitance in the femto Farad order. It consists of an oscillation circuit that generates the system clock, a power-on reset circuit that resets the system when the power is turned on, a multiplexer that selects the input channels, a two-stage amplifier that detects

the changes in the capacitance and outputs analog-amplitude values, a A/D converter that converts the analog-amplitude values into digital data, and a control logic that controls the entire chip. Also, it has an I²C compatible bus or SPI that enables serial communication with external devices as necessary.

LC717A00AR

Pin Assignment

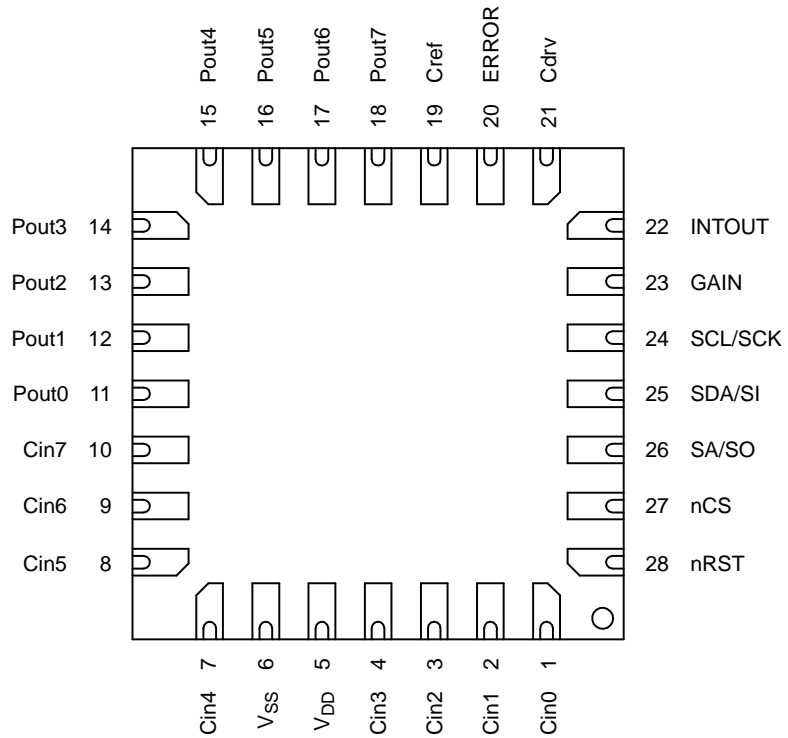


Figure 9. Pin Assignment

Table 7. PIN ASSIGNMENT

| Pin No. | Pin Name | Pin No. | Pin Name |
|---------|-----------------|---------|----------|
| 1 | Cin0 | 15 | Pout4 |
| 2 | Cin1 | 16 | Pout5 |
| 3 | Cin2 | 17 | Pout6 |
| 4 | Cin3 | 18 | Pout7 |
| 5 | V _{DD} | 19 | Cref |
| 6 | V _{SS} | 20 | ERROR |
| 7 | Cin4 | 21 | Cdrv |
| 8 | Cin5 | 22 | INTOUT |
| 9 | Cin6 | 23 | GAIN |
| 10 | Cin7 | 24 | SCL/SCK |
| 11 | Pout0 | 25 | SDA/SI |
| 12 | Pout1 | 26 | SA/SO |
| 13 | Pout2 | 27 | nCS |
| 14 | Pout3 | 28 | nRST |

LC717A00AR

Table 8. PIN FUNCTION

| Pin Name | I/O | Pin Functions | Pin Type |
|----------|-----|-----------------------------------------------------------------|----------|
| Cin0 | I/O | Capacitance sensor input | |
| Cin1 | I/O | Capacitance sensor input | |
| Cin2 | I/O | Capacitance sensor input | |
| Cin3 | I/O | Capacitance sensor input | |
| Cin4 | I/O | Capacitance sensor input | |
| Cin5 | I/O | Capacitance sensor input | |
| Cin6 | I/O | Capacitance sensor input | |
| Cin7 | I/O | Capacitance sensor input | |
| Cref | I/O | Reference capacitance input | |
| Pout0 | O | Cin0 judgment result output | |
| Pout1 | O | Cin1 judgment result output | |
| Pout2 | O | Cin2 judgment result output | |
| Pout3 | O | Cin3 judgment result output | |
| Pout4 | O | Cin4 judgment result output | |
| Pout5 | O | Cin5 judgment result output | |
| Pout6 | O | Cin6 judgment result output | |
| Pout7 | O | Cin7 judgment result output | |
| ERROR | O | Error occurrence status output | |
| Cdrv | O | Output for capacitance sensors drive | |
| INTOUT | O | Interrupt output | |
| SCL/SCK | I | Clock input (I ² C) / Clock input (SPI) | |
| GAIN | I | Selection pin of the initial value of gain of the 2nd-amplifier | |
| nCS | I | Interface selection / Chip select inverting input (SPI) | |
| nRST | I | External reset signal inverting input | |
| SDA/SI | I/O | Data input and output (I ² C) / Data input (SPI) | |

Table 8. PIN FUNCTION (continued)

| Pin Name | I/O | Pin Functions | Pin Type |
|-----------------|-----|-------------------------------------------------------------------|----------|
| SA/SO | I/O | Slave address selection (I ² C) / Data output (SPI) | |
| V _{DD} | | Power supply (2.6 V to 5.5 V) (Note 13) | |
| V _{SS} | | Ground (Earth) (Notes 13, 14) | |

13. Inserting a high-valued capacitor and a low-valued capacitor in parallel between V_{DD} and V_{SS} is recommended. In this case, the small-valued capacitor should be at least 0.1 μF, and is mounted near the LSI.

14. When V_{SS} terminal is not grounded in battery-powered mobile equipment, detection sensitivity may be degraded.

Details of Pin Functions

Cin0 to Cin7

These are the capacitance-sensor-input pins. These pins are used by connecting them to the touch switch pattern. Cin and the Cdrv wire patterns should be close to each other. By doing so, Cdrv and Cin patterns are capacitively coupled. Therefore, LSI can detect capacitance change near each pattern as 8-bit digital data.

However, if the shape of each pattern or the capacitively coupled value of Cdrv is not appropriate, it may not be able to detect the capacitance change correctly.

In this LSI, there is a two-stage amplifier that detects the changes in the capacitance and outputs analog-amplitude values. Cin0 to Cin7 are connected to the inverting input of the 1st amplifier in the LSI.

During measurement process, channels other than the one being measured are all in “Low” condition.

Leave the unused terminals open.

Cref

It is the reference-capacitance-input pin. It is used by connecting to the wire pattern like Cin pins or is used by connecting any capacitance between this pin and Cdrv pin.

In this LSI, there is a two-stage amplifier that detects the changes in the capacitance and outputs analog-amplitude values. Cref is connected to the non-inverting input of the 1st amplifier in the LSI.

Due to the parasitic capacitance generated in the wire connections of Cin pins and their patterns, as well as the one generated between the wire patterns of Cin and Cdrv pins, Cref may not detect capacitance change of each Cin pin accurately. In this case, connect an appropriate capacitance between Cref and Cdrv to detect capacitance change accurately.

However, if the difference between the parasitic capacitance of each Cin pin is extremely large, it may not detect capacitance change in each Cin pin correctly.

Pout0 to Pout7

These are the detection-result-output pins. The capacitance detection results of Cin0 to Cin7 are compared with the threshold of the LSI. The pin outputs a “High” or a “Low” depending on the result.

ERROR

It is the error-occurrence-status-output pin. It outputs “Low” during normal operation. If there is a calibration error or a system error, it outputs “High” to indicate that an error occurred.

Cdrv

It is the output pin for capacitance sensors drive. It outputs the pulse voltage which is needed to detect capacitance at Cin0 to Cin7.

Cdrv and Cin wire patterns should be close to each other so that they are capacitively coupled.

INTOUT

It is the interrupt-output pin. It outputs “High” when a measurement process is completed.

Connect to a main microcomputer if necessary, and use as interrupt signal.

Leave the terminal open if not in used.

SCL/SCK

Clock input (I²C)/Clock input (SPI). It is the clock input pin of the I²C compatible bus or the SPI depending on the mode of operation.

If interface is not to be used, fix the pin to “High”. However, even if interface is not to be used, providing a communication terminal on board is still recommended.

LC717A00AR

GAIN

In this LSI, there is a two-stage amplifier that detects the changes in the capacitance and outputs analog-amplitude values. It is the selection pin of the initial value of gain of the 2nd amplifier.

Even if this LSI is used alone, gain setting can still be selected through this terminal. At initialization of the LSI, it is set to 7-times higher than the minimum setting when GAIN pin is “Low”, and is set to 14-times higher than the minimum setting when GAIN pin is “High”.

nCS

Interface selection/Chip-select-inverting input (SPI). Selection of I²C compatible bus mode or SPI mode is through this terminal. After initialization, the LSI is automatically in I²C compatible bus mode. To continually use I²C compatible bus mode, fix nCS pin to “High”. To switch to SPI mode after LSI initialization, change the nCS input “High” → “Low”. The nCS pin is used as the chip-select-inverting input pin of SPI, and SPI mode is kept until LSI is again initialized.

If interface is not to be used, fix the pin to “High”.

nRST

It is the external-reset-signal-inverting-input pin. When nRST pin is “Low”, LSI is in the reset state.

Each pin (Cin0 to 7, Cref, Pout0 to 7, ERROR) is “Hi-Z” during reset state.

SDA/SI

Data input and output (I²C)/Data input (SPI). It is the data input and output pin of the I²C compatible bus or the data input pin of the SPI depending on the mode of operation.

If interface is not to be used, fix the pin to “High”. However, even if interface is not to be used, providing a communication terminal on board is still recommended.

SA/SO

Slave address selection (I²C)/Data output (SPI). It is the slave address selection pin of the I²C compatible bus or the data output pin of the SPI depending on the mode of operation.

If interface is not to be used, fix the pin to “High”. However, even if interface is not to be used, providing a communication terminal on board is still recommended.

Table 9. ORDERING INFORMATION

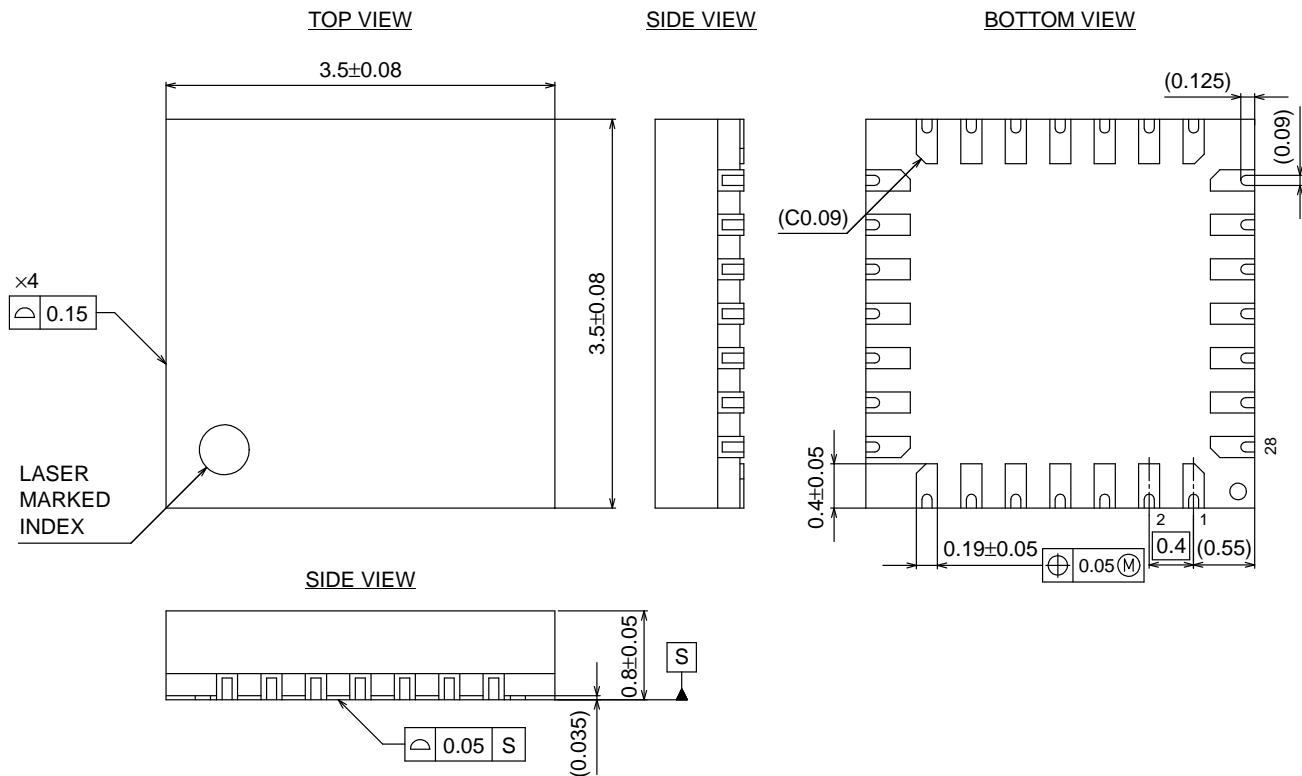
| Device | Package | Shipping (Qty / Packing) [†] |
|---------------|---------------------------------------------|---------------------------------------|
| LC717A00AR-NH | VCT28 3.5 × 3.5 (Pb-Free / Halogen Free) | 2000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

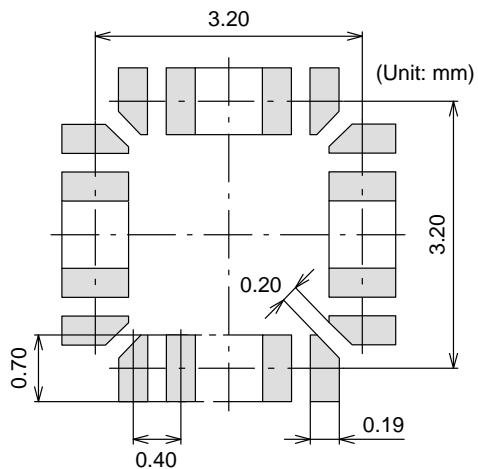
LC717A00AR

PACKAGE DIMENSIONS

VCT28 3.5x3.5
CASE 601AE
ISSUE A




SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDERRM/D](http://www.onsemi.com/SOLDERRM/D).

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