xCORE-200 USB sliceKIT Hardware Manual

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XMOS

SYNOPSIS

This document pertains to the 1V1 revision of the XP-SKC-XU216 sliceKIT Core Board.

Table of Contents

1 Overview

IN THIS CHAPTER

1.1 Introduction

This document covers the hardware design of the xCORE-200 USB sliceKIT Core Board (XP-SKC-XU216).

The Core Board contains a fully pinned out 500MHz, 16-core XU216-512-FB236 device, with its GPIOs connected to three expansion connectors (termed `Slots`) to interface with expansion cards (called sliceCARDs) that plug into the slots. The Core Board has specialist `Slot`, for USB connectivity. The Core Board also contains all circuitry necessary for operating and debugging the XMOS system. Multiple sliceKIT Core Boards can be interconnected to form a multi XMOS device system with bi-directional 5-bit xCONNECT Links being present between the boards. The xCORE-200 USB Core Board is only capable of being the start of a chain i.e. the chain master.

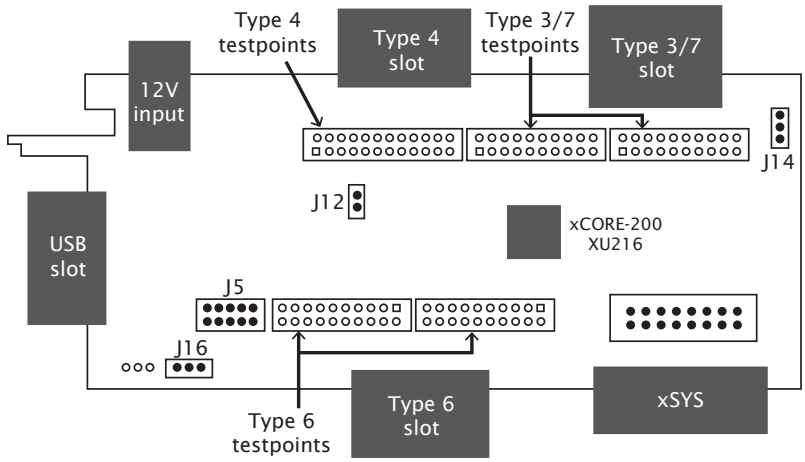

Figure 1: xCORE-200 USB sliceKIT Core board

1.2 sliceKIT System Layout

Figure 1 shows the layout of the xCORE-200 USB Core Board. Each of the four slots has a specific numbering - 3/7, 4, 6 and USB (labelled U), printed on the Core Board silkscreen. The slot 4 contains 24 xCORE GPIO; the slots 3/7 , 6 contain 20 xCORE GPIO. The USB Slice slot contains 8 xCORE GPIO along with the USB differential data signals.

All Slots are 36 pin PCI express style connectors in either socket or edge finger (plug) types.

3/7 and 4 Slots are pinned out from Tile 1 of the XU216 and the USB (U) and 6 Slots from Tile 0.

1.2.1 Slot naming conventions

xCORE-200 devices like the XU216-512-FB236 used on the xCORE-200 USB sliceKIT Core Board, include dedicated 32 bit ports in addition to the 1, 4, 8 and 16 bit ports supported on XS1 sliceKIT Core Boards. To support the additional ports, a numeric naming convention is used on xCORE-200 sliceKIT Core Boards instead of the symbols used previously. The following table shows the new and old conventions.

XS1 Symbol	xCORE-200 Number	Description
U	U	USB
A	A	Analog
STAR	1	1, 4, 8, 16-bit ports
TRIANGLE	2	1, 4, 8, 16-bit ports
SQUARE	3	1, 4, 8, 16-bit ports
CIRCLE	4	1, 4, 8, 16-bit ports
DIAMOND	5	1, 4, 8, 16-bit ports
-New-	6	32-bit ports
-New-	7	32-bit ports

2 Core Board

IN THIS CHAPTER

The xCORE-200 USB Core Board includes the xU216-512-FB236 device and support circuitry. The device GPIO are connected to the Slots, with test points available for each signal.

The Core Board is powered by a 12V external power supply, provided with the kit.

An xTAG debug adapter can be connected to the xSYS connector, providing a debug link from a USB host.

2.1 Power Supply

Power input to the sliceKIT Core Board is via a standard barrel jack connector. A standard 12V external power supply should be used to power the board. Each Core Board requires its own 12V supply. This input supply is used to generate the main 5V board supply via a DC-DC converter.

The 5V board supply is fed to all the GPIO Slot connectors as well as powering the Core Board itself. A 3V3 I/O supply is generated by a DC-DC converter from the 5V main supply, and a 3V3 analogue supply is generated by an LDO converter from the 5V main supply.

The Core Board provides 3V3 and 5V at 0.25A to each slot for a total of approximately 2W per slice.

The 12V supply is provided to the USB Slot connector for local conversion for USB charger supplies.

2.2 Debug

Debug of the system is via the xSYS Connector. The JTAG signals are connected as shown below.

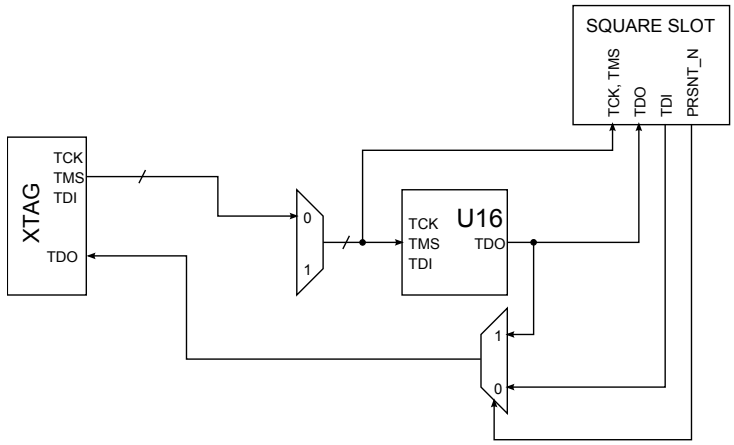

Figure 2: JTAG Chain

A presence detect signal is present on both the Type-3 Slot connector to allow detection of a connected board and subsequent automatic switching of the JTAG chain. In a system of multiple Core Boards, the Master is the source of the JTAG chain so the system can only be debugged from the master. Other boards see no devices in the JTAG chain.

The use of xSCOPE is covered in the xCONNECT Links section (2.6).

2.3 XU216 Device Boot Procedure

Master Core Boards boot from the QSPI flash, while slave Core Boards boot from xCONNECT link XL0 from the next connected Core Board.

To allow re-use of the QSPI boot pins (ports 1B, 1C, 4B) as signal GPIO pins for the Type-6 slot, Jumper J12 and a latched bus switch is used which connects the xCORE QSPI pins to either the QSPI Flash or to the sliceCARD Slots. The switch is controlled by X0D30 and X0D31. Once the device has booted X0D31 is used to enable or disable the QSPI interface, X0D30 should then transition from low to high to latch the selection. The QSPI selection state is then maintained until the system is reset.

Once this sequence is completed the selection has been latched, therefore X0D30 and X0D31 will be available in the J5 header.

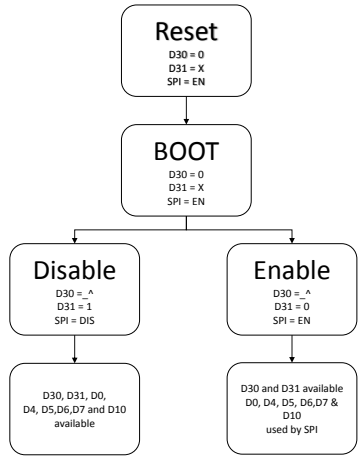

Figure 3: QSPI Select Flow Diagram

If the SPI is not disabled, sliceCARDs in the Type-6 slot may not function as expected. If there are no sliceCARDs in the Type-6 slot, then it does not matter whether the SPI has been disabled or not. Therefore, applications which require runtime access to the QSPI flash should either leave the Type-6 slot unpopulated or check to ensure that the Card which is in there will be unaffected by the operation of the Flash. The applications which reuse the QSPI GPIOs should remove the Jumper - J12 during flashing of the device for proper operation.

The xTAG debug adapter system can use the boot mode select signal to force all devices in the chain (master and slave Core Boards) to boot from JTAG (don't boot) for debug purposes.

If not in this mode, the devices will boot from SPI or xCONNECT link as appropriate.

2.4 xCONNECT Links

The Type-7 slot contains two 5-bit xCONNECT Links, XL1 and XL2, which can be used for chaining sliceKIT Core Boards together.

2.5 Reset

The whole system is held in reset until all power supplies are stable, and reset is connected to all sliceCARDs so any circuitry on them can be reset. It also indicates to the sliceCARDs that their power input is stable. The reset from the xTAG debug adapter resets the whole system, if required for debugging.

2.6 Clocking

There are two clock sources available on the Core Board. One provides a 25MHz system clock, the other is a 24MHz clock provided to the XU216 device.

The system clock from a Master Core Board is fed automatically to all of the slave Core Boards so the whole system will operate synchronously.

The system clock is also fed to each of the sliceCARD slots.

2.7 Loop-back Port

Jumper J16 can be used to enable a loop-back between a 1-bit port on Tile0 and Tile1. With the loop-back enabled port X0D39 is connected to X1D12, and disconnected from the `Header J5`. With the loop-back disabled X0D39 is connected to the `Header J5`.

2.8 Type-3/ Type-7 Slot

The GPIOs connected to the `Type-3` slot can be changed to an alternative `Type-7` configuration by setting the jumper J14. For `Type-3` slot GPIO J14 should be connected between `Pin 1---Pin 2` ‘; for “ Type-7 “ GPIOs J14 should be connected between “Pin 2—Pin 3‘.

The `Type-7` configuration exposes 20 bits of the 32-bit port, which can be useful for applications requiring a wide bus; the `Type-3` configuration exposes more 1-bit ports.

2.9 Slot Pinouts and Testpoints

The signal assignments for the connectors on the Core Board and sliceCARDs can be seen in the following tables, with the related testpoints.

2.9.1 USB SLOT TOP SIDE PINOUT TABLE

PCIE A (TOP)	SIGNAL	FUNCTION
A1	*GND*	POWER SUPPLY GROUND
A2	*GND*	POWER SUPPLY GROUND
A3	USB DN	USB DATA NEGATIVE
A4	USB DP	USB DATA POSITIVE
A5	*GND*	POWER SUPPLY GROUND
A6	*GND*	POWER SUPPLY GROUND
A7	X0D33	P4E3 P8C7 P16B7
A8	X0D32	P4E2 P8C6 P16B6
A9	*GND*	POWER SUPPLY GROUND
A10	X0D27	P4E1 P8C1 P16B1
A11	X0D26	P4E0 P8C0 P16B0
KEY	**KEY**	**MECHANICAL KEY**
A12	*3V3*	3.3V POWER SUPPLY
A13	*GND*	POWER SUPPLY GROUND
A14	*5V*	5.0V POWER SUPPLY
A15	*5V*	5.0V POWER SUPPLY
A16	*GND*	POWER SUPPLY GROUND
A17	*12V*	12.0V POWER SUPPLY
A18	*12V*	12.0V POWER SUPPLY

2.9.2 USB SLOT BOTTOM SIDE PINOUT TABLE

PCIE B (BOT)	SIGNAL	FUNCTION
B1	*GND*	POWER SUPPLY GROUND
B2	*GND*	POWER SUPPLY GROUND
B3	*GND*	POWER SUPPLY GROUND
B4	*GND*	POWER SUPPLY GROUND
B5	*GND*	POWER SUPPLY GROUND
B6	*GND*	POWER SUPPLY GROUND
B7	NC	NOT CONNECTED
B8	X0D35	P1L0
B9	X0D36	P1M0 P8D0 P16B8
B10	X0D0	P1A0
B11	X0D11	P1D0
KEY	**KEY**	**MECHANICAL KEY**
B12	RESET	xCORE-200 RESET
B13	*GND*	POWER SUPPLY GROUND
B14	*VBUS*	VBUS POWER SUPPLY IN
B15	*VBUS*	VBUS POWER SUPPLY IN
B16	*GND*	POWER SUPPLY GROUND
B17	*12V*	12.0V POWER SUPPLY
B18	*12V*	12.0V POWER SUPPLY

2.9.3 Type-3 SLOT TOP SIDE PINOUT TABLE

PCIE B (TOP)	SIGNAL	FUNCTION			
B1	*DEBUG*	xSYS DEBUG SIGNAL			
B2	*TCK*	xSYS TCK SIGNAL			
B3	*GND*	POWER SUPPLY GROUND			
B4	*TDI*	xSYS TDI SIGNAL			
B5	*3V3*	POWER SUPPLY 3.3V			
B6	X1D2	P4A0	P8A0	P16A0	P32A20
B7	X1D3	P4A1	P8A1	P16A1	P32A21
B8	*GND*	POWER SUPPLY GROUND			
B9	X1D4	P4B0	P8A2	P16A2	P32A22
B10	X1D10	P1C0			
B11	X1D5	P4B1	P8A3	P16A3	P32A23
KEY	**KEY**	**MECHANICAL KEY**			
B12	X1D14	P4C0	P8B0	P16A8	P32A28
B13	X1D15	P4C1	P8B1	P16A9	P32A29
B14	*CLK*	MAIN SYSTEM CLOCK			
B15	X1D22	P1G0			
B16	*GND*	POWER SUPPLY GROUND			
B17	X1D16	P4D0	P8B2	P16A10	
B18	X1D17	P4D1	P8B3	P16A11	

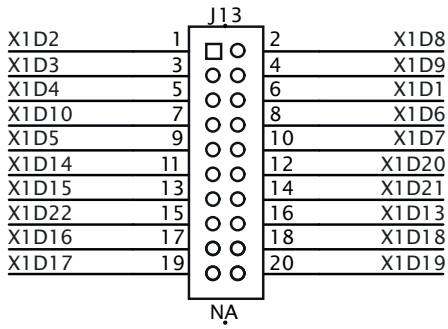

Figure 4: J13: Type-3 Slot Testpoints

2.9.4 Type-3 SLOT BOTTOM SIDE PINOUT TABLE

PCIE A (BOT)	SIGNAL	FUNCTION
A1	*NC*	NOT CONNECTEDNAL
A2	*5V*	POWER SUPPLY 5V
A3	*TMS*	xSYS TMS SIGNAL
A4	*TDO*	xSYS TDO SIGNAL
A5	*PRSNT*	SYSTEM PRESENT SIGNAL (ACTIVE LOW)
A6	X1D8	P4A2 P8A6 P16A6 P32A26
A7	X1D9	P4A3 P8A7 P16A7 P32A27
A8	X1D1	P1B0
A9	X1D6	P4B2 P8A4 P16A4 P32A24
A10	*GND*	POWER SUPPLY GROUND
A11	X1D7	P4B3 P8A5 P16A5 P32A25
KEY	**KEY**	**MECHANICAL KEY**
A12	X1D20	P4C2 P8B6 P16A14 P32A30
A13	X1D21	P4C3 P8B7 P16A15 P32A31
A14	*GND*	POWER SUPPLY GROUND
A15	X1D13	P1F0
A16	*RST_N*	xCORE-200 RESET (ACTIVE LOW)
A17	X1D18	P4D2 P8B4 P16A12
A18	X1D19	P4D3 P8B5 P16A13

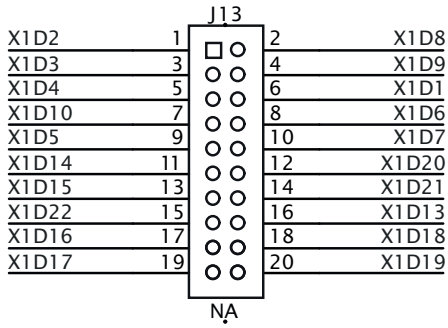

Figure 5: J13: Type-3 Slot Testpoints

2.9.5 Type-7 SLOT TOP SIDE PINOUT TABLE

PCIE B (TOP)	SIGNAL	FUNCTION
B1	*DEBUG*	xSYS DEBUG SIGNAL
B2	*TCK*	xSYS TCK SIGNAL
B3	*GND*	POWER SUPPLY GROUND
B4	*TDI*	xSYS TDI SIGNAL
B5	*3V3*	POWER SUPPLY 3.3V
B6	X1D57	P32A8
B7	X1D56	P32A7
B8	*GND*	POWER SUPPLY GROUND
B9	X1D55	P32A6
B10	X1D49	P32A0
B11	X1D54	P32A5
KEY	**KEY**	**MECHANICAL KEY**
B12	X1D69	P32A18
B13	X1D68	P32A17
B14	*CLK*	MAIN SYSTEM CLOCK
B15	X1D61	P32A10
B16	*GND*	POWER SUPPLY GROUND
B17	X1D67	P32A16
B18	X1D66	P32A17

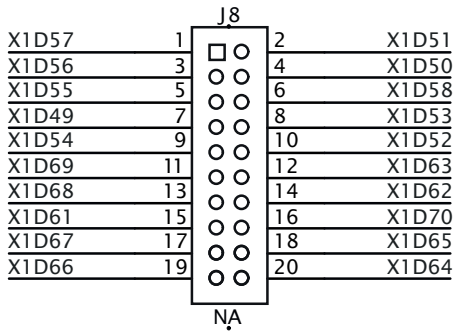

Figure 6: J8: Type-7 Slot Testpoints

2.9.6 Type-7 SLOT BOTTOM SIDE PINOUT TABLE

PCIE A (BOT)	SIGNAL	FUNCTION
A1	*NC*	NOT CONNECTED
A2	*5V*	POWER SUPPLY 5V
A3	*TMS*	xSYS TMS SIGNAL
A4	*TDO*	xSYS TDO SIGNAL
A5	*PRSNT*	SYSTEM PRESENT SIGNAL (ACTIVE LOW)
A6	X1D51	P32A2
A7	X1D50	P32A1
A8	X1D58	P32A9
A9	X1D53	P32A4
A10	*GND*	POWER SUPPLY GROUND
A11	X1D52	P32A3
KEY	**KEY**	**MECHANICAL KEY**
A12	X1D63	P32A12
A13	X1D62	P32A11
A14	*GND*	POWER SUPPLY GROUND
A15	X1D70	P32A19
A16	*RST_N*	xCORE-200 RESET (ACTIVE LOW)
A17	X1D65	P32A14
A18	X1D64	P32A13

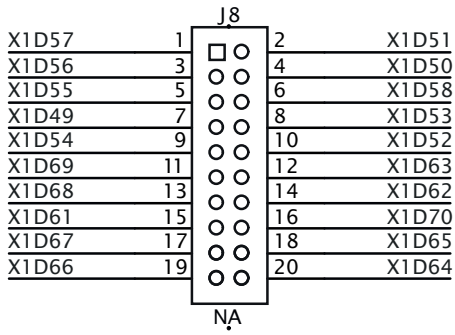

Figure 7: J8: Type-7 Slot Testpoints

2.9.7 Type-4 SLOT TOP SIDE PINOUT TABLE

PCIE B (TOP)	SIGNAL	FUNCTION			
B1	*NC*	NOT CONNECTED			
B2	X1D0	P1A0			
B3	*GND*	POWER SUPPLY GROUND			
B4	X1D11	P1D0			
B5	*3V3*	POWER SUPPLY 3.3V			
B6	X1D26		P4E0	P8C0	P16B0
B7	X1D27		P4E1	P8C1	P16B1
B8	*GND*	POWER SUPPLY GROUND			
B9	X1D28		P4F0	P8C2	P16B2
B10	X1D34	P1K0			
B11	X1D29		P4F1	P8C3	P16B3
KEY	**KEY**	**MECHANICAL KEY**			
B12	X1D36	P1M0		P8D0	P16B8
B13	X1D37	P1N0		P8D1	P16B9
B14	*CLK*	MAIN SYSTEM CLOCK			
B15	X1D24	P1I0			
B16	*GND*	POWER SUPPLY GROUND			
B17	X1D38	P1O0		P8D2	P16B10
B18	X1D39	P1P0		P8D3	P16B11

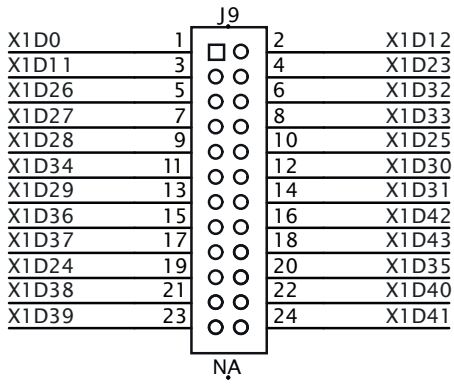

Figure 8: J9: Type-4 Slot Testpoints

2.9.8 Type-4 SLOT BOTTOM SIDE PINOUT TABLE

PCIE A (BOT)	SIGNAL	FUNCTION
A1	*NC*	NOT CONNECTED
A2	*5V*	POWER SUPPLY 5V
A3	X1D12	P1E0
A4	X1D23	P1H0
A5	*GND*	POWER SUPPLY GROUND
A6	X1D32	P4E2 P8C6 P16B6
A7	X1D33	P4E3 P8C7 P16B7
A8	X1D25	P1J0
A9	X1D30	P4F2 P8C4 P16B4
A10	*GND*	POWER SUPPLY GROUND
A11	X1D31	P4F3 P8C5 P16B5
KEY	**KEY**	**MECHANICAL KEY**
A12	X1D42	P8D6 P16B14
A13	X1D43	P8D7 P16B15
A14	*GND*	POWER SUPPLY GROUND
A15	X1D35	P1L0
A16	*RST_N*	xCORE-200 RESET (ACTIVE LOW)
A17	X1D40	P8D4 P16B12
A18	X1D41	P8D5 P16B13

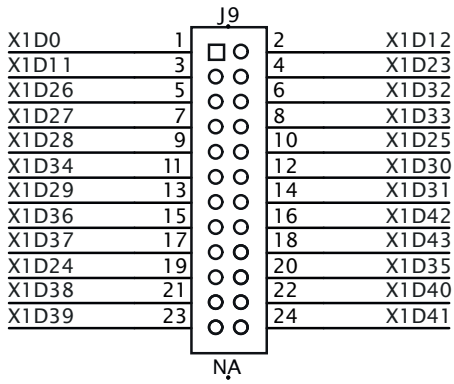

Figure 9: J9: Type-4 Slot Testpoints

2.9.9 Type-6 SLOT TOP SIDE PINOUT TABLE

PCIE B (TOP)	SIGNAL	FUNCTION			
B1	*NC*	NOT CONNECTED			
B2	*NC*	NOT CONNECTED			
B3	*GND*	POWER SUPPLY GROUND			
B4	*NC*	NOT CONNECTED			
B5	*3V3*	POWER SUPPLY 3.3V			
B6	X0D2	P4A0	P8A0	P16A0	P32A20
B7	X0D3	P4A1	P8A1	P16A1	P32A21
B8	*GND*	POWER SUPPLY GROUND			
B9	X0D4_EXT	P4B0	P8A2	P16A2	P32A22
B10	X0D10EXT	P1C0			
B11	X0D5_EXT	P4B1	P8A3	P16A3	P32A23
KEY	**KEY**	**MECHANICAL KEY**			
B12	X0D14	P4C0	P8B0	P16A8	P32A28
B13	X0D15	P4C1	P8B1	P16A9	P32A29
B14	*CLK*	MAIN SYSTEM CLOCK			
B15	X0D38	P1O0	P8D2	P16B10	
B16	*GND*	POWER SUPPLY GROUND			
B17	X0D16	P4D0	P8B2	P16A10	
B18	X0D17	P4D1	P8B3	P16A11	

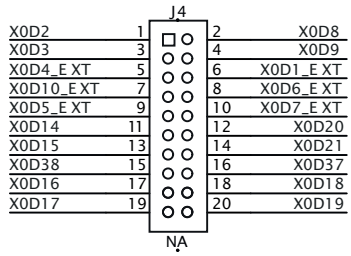

Figure 10: J4: Type-6 Slot Testpoints

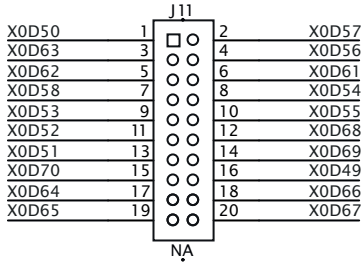

Figure 11: J11: Type-6 Slot Testpoints

2.9.10 Type-6 SLOT BOTTOM SIDE PINOUT TABLE

PCIE A (BOT)	SIGNAL	FUNCTION			
A1	*NC*	NOT CONNECTED			
A2	*5V*	POWER SUPPLY 5V			
A3	*NC*	NOT CONNECTED			
A4	*NC*	NOT CONNECTED			
A5	*GND*	POWER SUPPLY GROUND			
A6	X0D8	P4A2	P8A6	P16A6	P32A26
A7	X0D9	P4A3	P8A7	P16A7	P32A27
A8	X0D1_EXT	P1B0			
A9	X0D6_EXT	P4B2	P8A4	P16A4	P32A24
A10	*GND*	POWER SUPPLY GROUND			
A11	X0D7_EXT	P4B3	P8A5	P16A5	P32A25
KEY	**KEY**	**MECHANICAL KEY**			
A12	X0D20	P4C2	P8B6	P16A14	P32A30
A13	X0D21	P4C3	P8B7	P16A15	P32A31
A14	*GND*	POWER SUPPLY GROUND			
A15	X0D37	P1N0	P8D0	P16B8	
A16	*RST_N*	xCORE-200 RESET (ACTIVE LOW)			
A17	X0D18	P4D2	P8B4	P16A12	
A18	X0D19	P4D3	P8B5	P16A13	

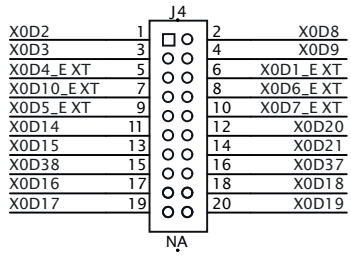

Figure 12: J4: Type-6 Slot Testpoints

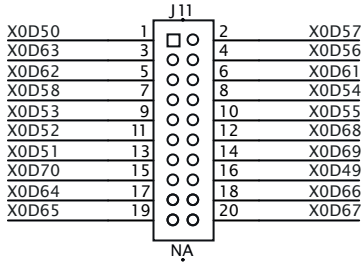

Figure 13: J11: Type-6 Slot Testpoints

2.9.11 System Services Slot Signals

On all Slots, TDO is always out of the sliceKIT Core Board, TDI is always in to the Core Board.

MSEL, TCK, TMS, RST_N are all inputs to the Core Board from the xSYS Connector and outputs from the Core Board on the Type-3 Slot.

DEBUG is bidirectional. PRSNT_N is used on the Type-3 Slot to detect another Core Board is connected. This signal is used to switch the JTAG chain signals.

CLK and RST_N are output from all Slots.

2.10 xCORE-200 USB sliceKIT schematics

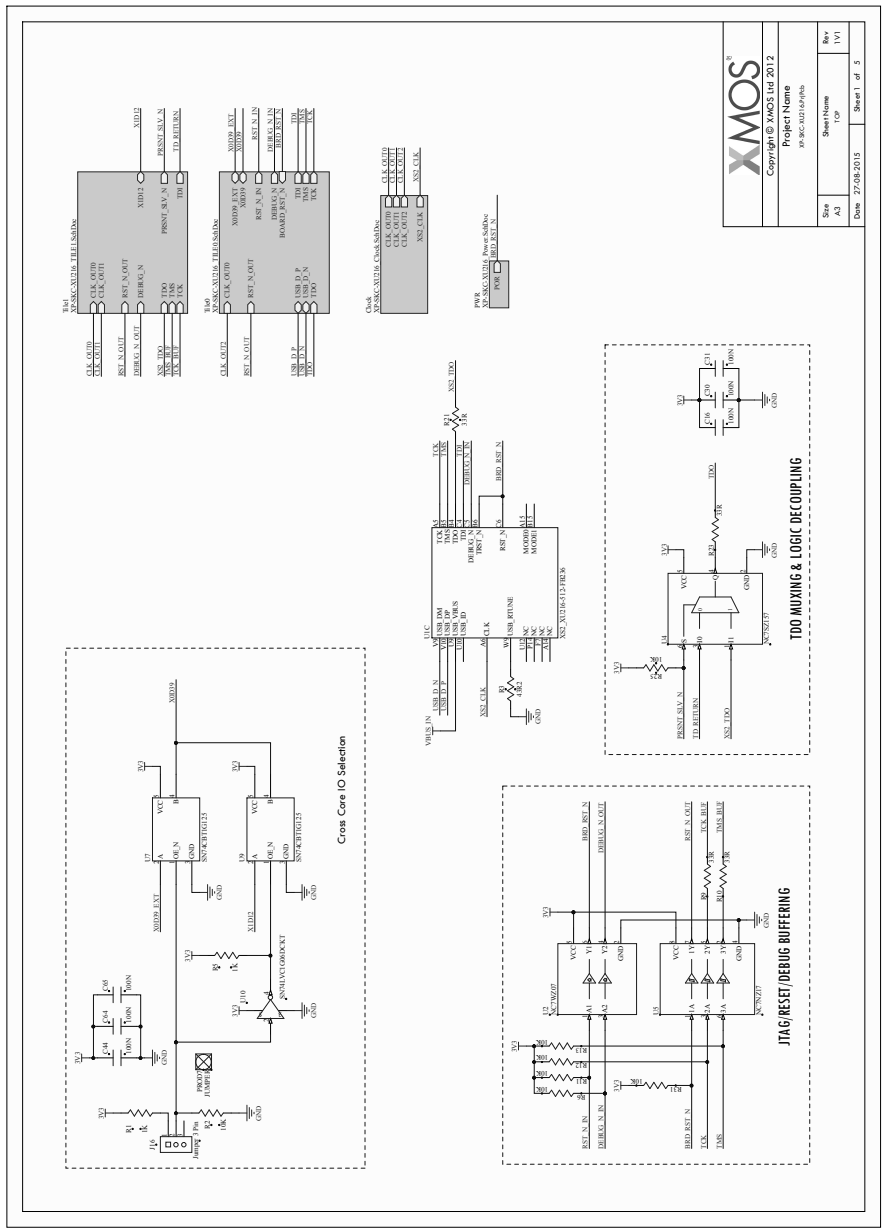

Figure 14: xCORE-200 USB sliceKIT schematic (1 of 5)

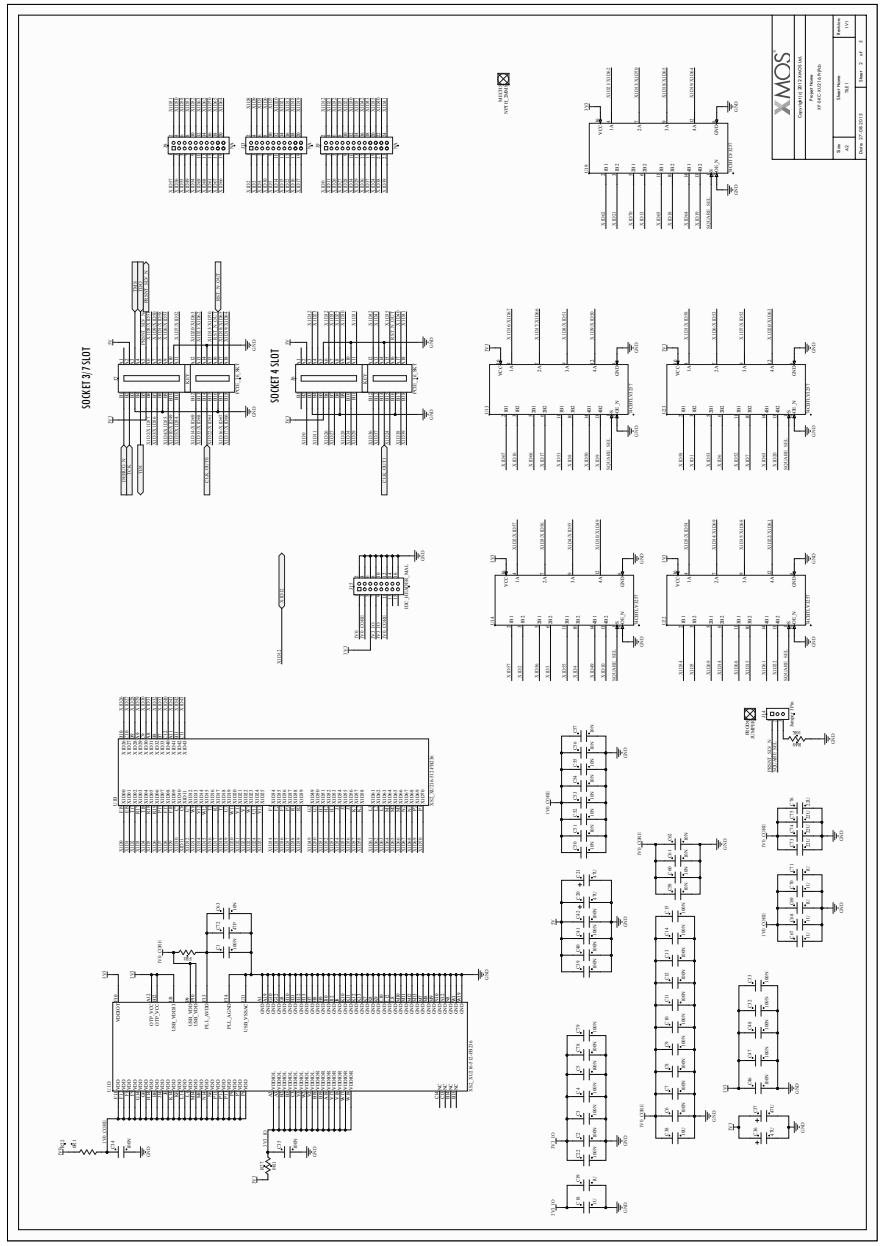

Figure 15: xCORE-200 USB sliceKIT schematic (2 of 5)

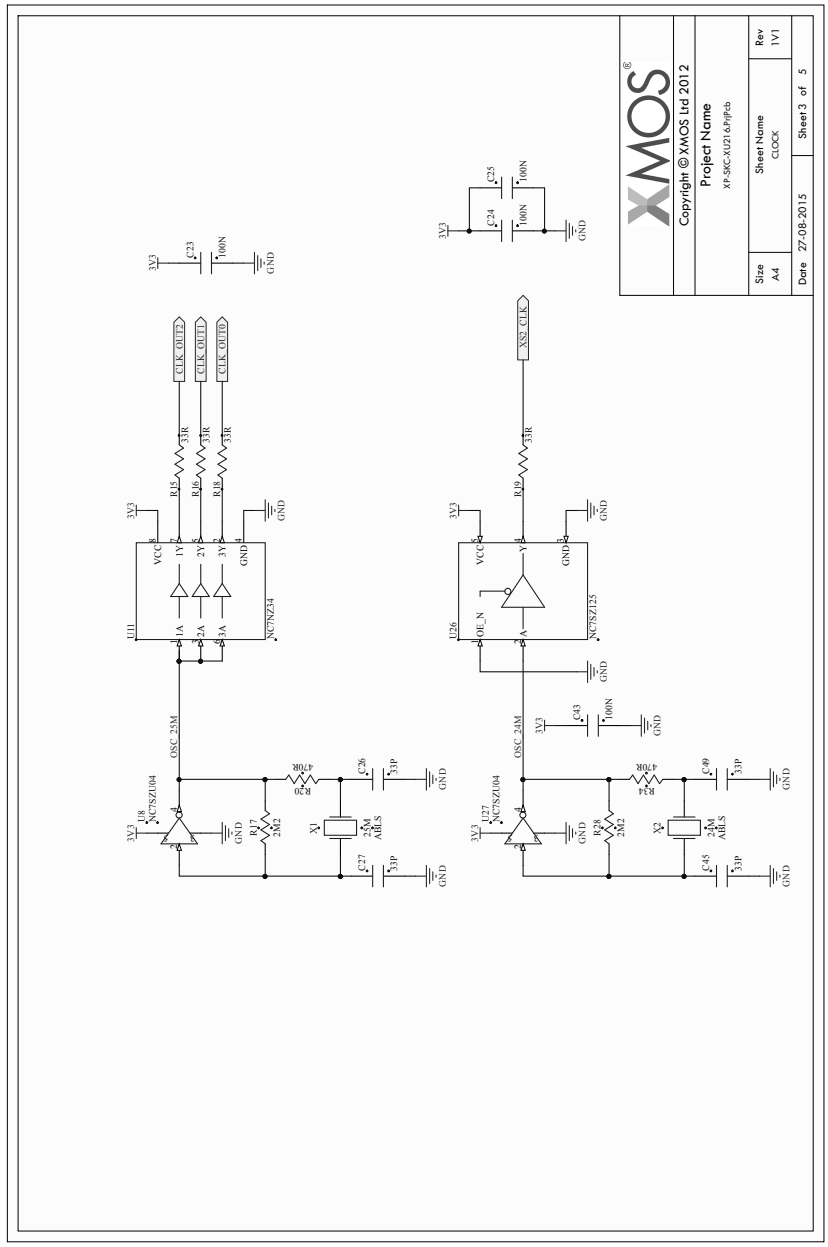

Figure 16: xCORE-200 USB sliceKIT schematic (3 of 5)

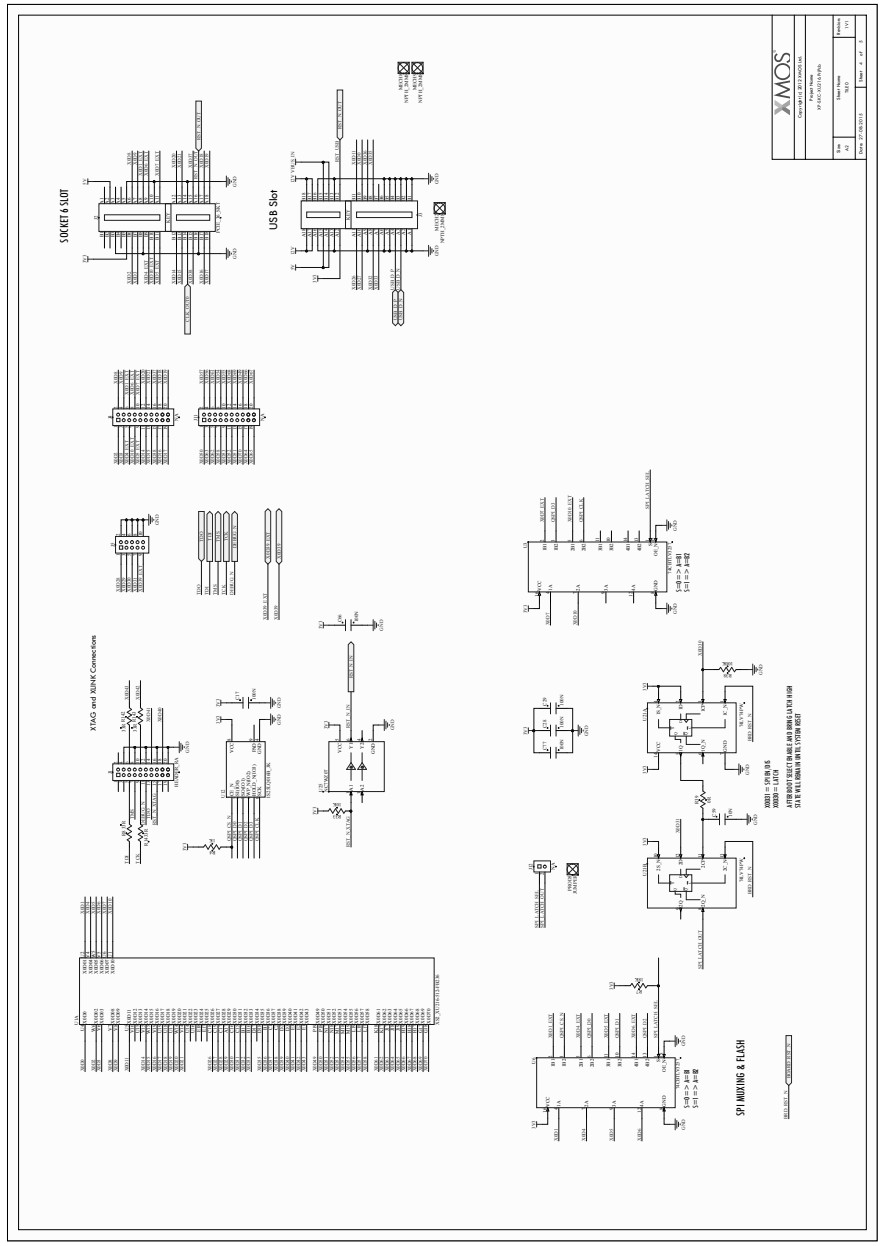

Figure 17: xCORE-200 USB sliceKIT schematic (4 of 5)

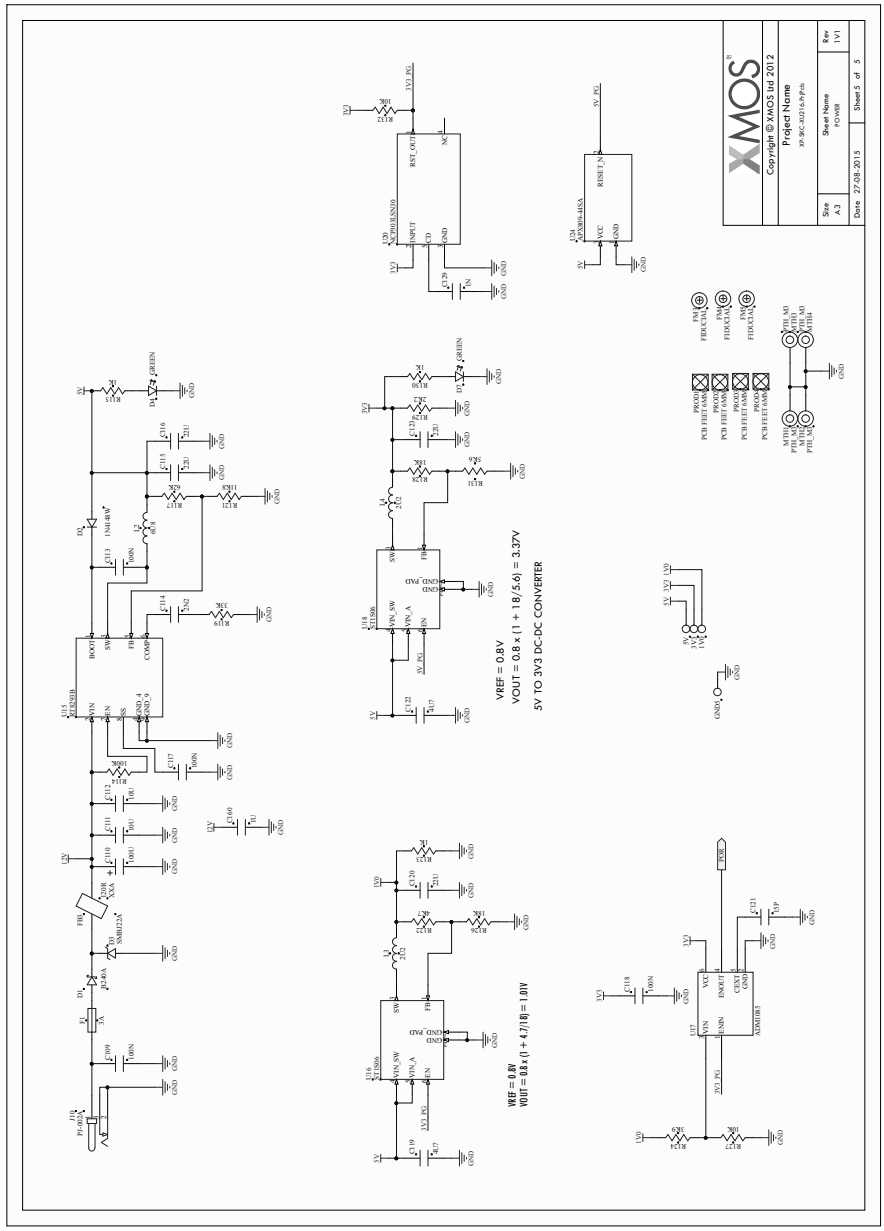

Figure 18: xCORE-200 USB sliceKIT schematic (5 of 5)

3 USB sliceCARDs

IN THIS CHAPTER

USB sliceCARDs connect to the PCI-E 36 pin connector J3 on the XU216 Core Board. They have a unique key design in order to prevent them being plugged in to non USB slice slots and prevent non USB slices being plugged in to a USB slice slot. The detail for the key design and the PCI-E 36 card edge finger can be seen in the figure below:

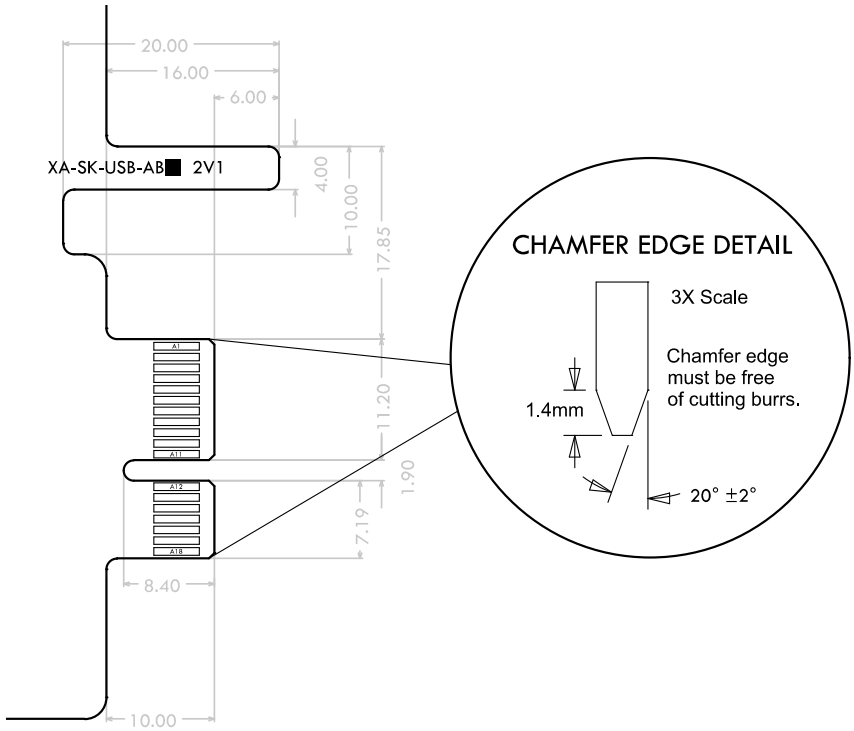

Figure 19: USB Slice Detail

3.1 XU216 USB Slice Pinout

The table below details the pinout of the USB slice connector from the XU216 Core Board:

PCIE A (TOP)	SIGNAL	FUNCTION	PCIE B (BOT)	SIGNAL	FUNCTION
A1	*GND*	POWER SUPPLY GROUND	B1	*GND*	POWER SUPPLY GROUND
A2	*GND*	POWER SUPPLY GROUND	B2	*GND*	POWER SUPPLY GROUND
A3	USB DN	USB DATA NEGATIVE	B3	*GND*	POWER SUPPLY GROUND
A4	USB DP	USB DATA POSITIVE	B4	*GND*	POWER SUPPLY GROUND
A5	*GND*	POWER SUPPLY GROUND	B5	*GND*	POWER SUPPLY GROUND
A6	*GND*	POWER SUPPLY GROUND	B6	*GND*	POWER SUPPLY GROUND
A7	X0D33	RESERVED FOR MFI	B7	*NC*	NOT CONNECTED
A8	X0D32	RESERVED	B8	X0D35	I2C SDA
A9	*GND*	POWER SUPPLY GROUND	B9	X0D36	I2C SCL
A10	X0D27	USB SEL 2	B10	X0D0	RESERVED
A11	X0D26	USB SEL 1	B11	X0D11	VBUS OUT ENABLE (H)
KEY	**KEY**	**MECHANICAL KEY**	**KEY**	**KEY**	**MECHANICAL KEY**
A12	*3V3*	3.3V POWER SUPPLY	B12	RST_USB	xCORE-200 RESET
A13	*GND*	POWER SUPPLY GROUND	B13	*GND*	POWER SUPPLY GROUND
A14	*5V*	5.0V POWER SUPPLY	B14	VBUS IN	VBUS FROM USB HOST
A15	*5V*	5.0V POWER SUPPLY	B15	VBUS IN	VBUS FROM USB HOST
A16	*GND*	POWER SUPPLY GROUND	B16	*GND*	POWER SUPPLY GROUND
A17	*12V*	12.0V POWER SUPPLY	B17	*12V*	12.0V POWER SUPPLY
A18	*12V*	12.0V POWER SUPPLY	B18	*12V*	12.0V POWER SUPPLY

Figure 20: USB Slice Pinout

3.2 USB AB Slice

The USB AB slice consists of a USB A connector, USB B connector and a high-speed 2:1 switch to select between them.

By default the USB data signals from the B type connector are routed to the U8 device on the U16 board. When the USB B connector is being routed the LED next to the connector is illuminated. In order to route the USB data signals from the A type connector the *USB_SEL* line should be bought high. When the USB A connector is being routed the LED next to the connector is illuminated.

5V is supplied to the USB A connector, from a local power supply, to provide VBUS to connected devices. This supply can be disabled by bringing the signal `VBUS_OUT_EN` low.

The figure below shows the layout of the USB A/B slice:

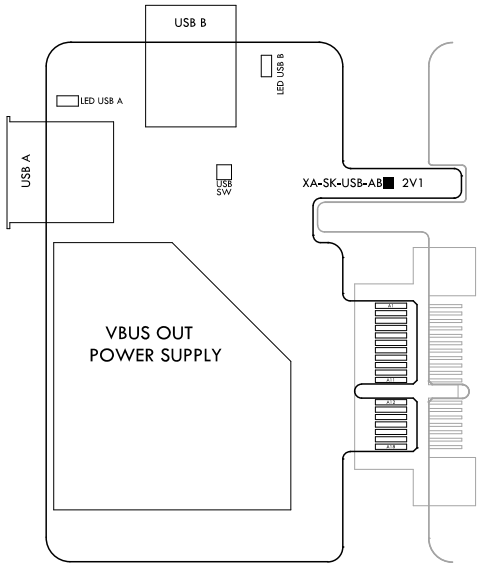

Figure 21: USB AB Slice

4 New Designs Based on sliceKIT

IN THIS CHAPTER

There are a number of sections of the design of the sliceKIT platform that have been optimized for flexibility to cover as many use cases as possible. Therefore some consideration may be required in what to leave out or change in a custom design. Some of the important points to consider are dealt with in this section.

Some general points to consider when implementing your own design are:

- Always check the datasheet of the xCORE device. In the case where the reference design and datasheet conflict, the datasheet presides.
- XMOS datasheets contain additional hardware design requirements and guidelines that are not covered in this document, which users of XMOS hardware reference designs must ensure are followed.
- The presence of a third party device in an XMOS hardware reference design does not make any statement about its general availability. You must make your own arrangements to ensure that all components can be sourced in the required volumes.

4.1 USB

The xCORE-200 USB sliceKIT platform has been designed to allow for a number of options when it comes to USB connectivity. In a custom design it is highly unlikely that a high-speed connector will be required, hence the USB slice connector can be removed and your own connectivity option can be implemented.

For all USB implementations the following points should be considered:

- Keep USB data lines as short as possible
- The USB data differential pair should have a characteristic impedance of 90R
- Common mode chokes, vias, connectors and stubs should be avoided if at all possible to maximise signal integrity
- For further information refer to **'High Speed USB Platform Design Guidelines'_**

The xCORE-200 Core Board USB design is a compromise to allow for maximum

flexibility in use. Therefore it should not be used as a reference for custom designs that require full USB compliance.

4.1.1 USB Device (B)

For a simple device only configuration a USB B connector (standard, mini or micro size) should be connected directly to the USB data lines of the XU216 device. If the device is to be bus powered an ESD device can be added to clamp the data lines to VBUS and ground and the connection to the XU216 VBUS pin can be omitted. If the device is to be self powered then the data lines should only be clamped to ground, and the VBUS input should be connected to the XU216 VBUS pin to detect host connection.

4.1.2 USB Host (A)

To implement a host only connection a USB A connector should be directly connected to the USB data lines of the XU216 device. The VBUS power supply will need to be provided locally. An ESD device can be added to clamp the data lines to VBUS and ground.

4.1.3 Multi Mode USB

For more complex configurations requiring a number of host and/or device connections to be available one or more high speed capable USB bus switches can be used, with the routing being controlled using one of the wider ports available on the XU device. There are many options for deciding which port to route to (and consequently which code to boot) from a user input switch to sensing connections and deciding priority.

4.2 Portmap

Due to the flexibility of the I/O on an xCORE-200 device the location of the signals routed to the XU216 can be easily optimized for your own layout.

As a general rule any 1-bit port pin can be easily swapped with any other. The only fixed 1-bit port pins are those connected to the SPI bus of the code flash device.

The location of signals on the 4-bit ports can be swapped with other signals on the same port, and the ports as a whole can be swapped, however care should be taken to ensure that all signals on the same port should be in the same direction i.e. all outputs or all inputs.

4.3 QSPI Routing Control

In order to maximize the functionality of the sliceKIT platform all of the ports used by the boot flash can also used by the system after boot. In order to allow for this the QSPI 1-bit ports are latched to either the flash device or to the I/O.

If your design does not make use of all of the 1-bit ports then the slave select line should be left to only control the QSPI interface and the rest of the QSPI 1-bit ports can be reused.

4.4 Debug Interface

During the development phase of a new design it is highly recommended that the full XSYS debug interface, including the xSCOPE xCONNECT link, should be included. This allows for full programming and debug interfaces.

Once the design is stable the xSCOPE xCONNECT link can be omitted, and if space is a concern the main JTAG signals can be bought out to a custom header, or test points.

For high volume builds it is possible to omit the debug interface altogether, however this will require another method of programming the flash e.g. preprogrammed before placement.

For single device designs most of the switching and buffering devices for the JTAG chain can be omitted.