

## HAT2261H

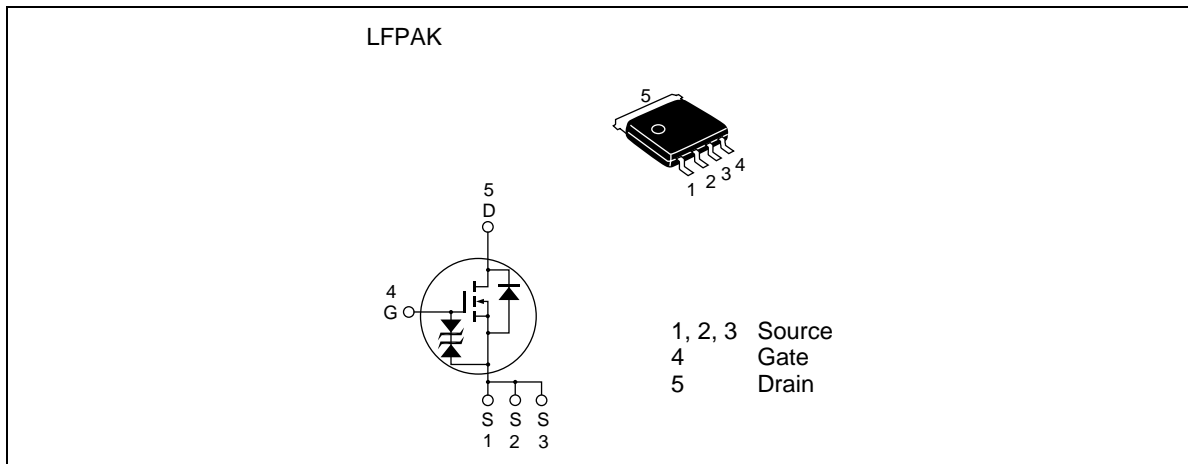
Silicon N Channel Power MOS FET Power Switching

Rev.1.00  
Jun.06.2005

### Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance  
 $R_{DS(on)} = 2.9 \text{ m}\Omega$  typ. (at  $V_{GS} = 10 \text{ V}$ )

### Outline



**Absolute Maximum Ratings**

(Ta = 25°C)

<b>Item</b>	<b>Symbol</b>	<b>Ratings</b>	<b>Unit</b>
Drain to source voltage	V <sub>DSS</sub>	30	V
Gate to source voltage	V <sub>GSS</sub>	±20	V
Drain current	I <sub>D</sub>	45	A
Drain peak current	I <sub>D(pulse)</sub> <sup>Note1</sup>	180	A
Body-drain diode reverse drain current	I <sub>DR</sub>	45	A
Avalanche current	I <sub>AP</sub> <sup>Note 2</sup>	25	A
Avalanche energy	E <sub>AR</sub> <sup>Note 2</sup>	62.5	mJ
Channel dissipation	P <sub>ch</sub> <sup>Note3</sup>	25	W
Channel to Case Thermal Resistance	θ <sub>ch-C</sub>	5.0	°C/W
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%  
2. Value at T<sub>ch</sub> = 25°C, R<sub>g</sub> ≥ 50 Ω  
3. T<sub>c</sub> = 25°C

## HAT2261H

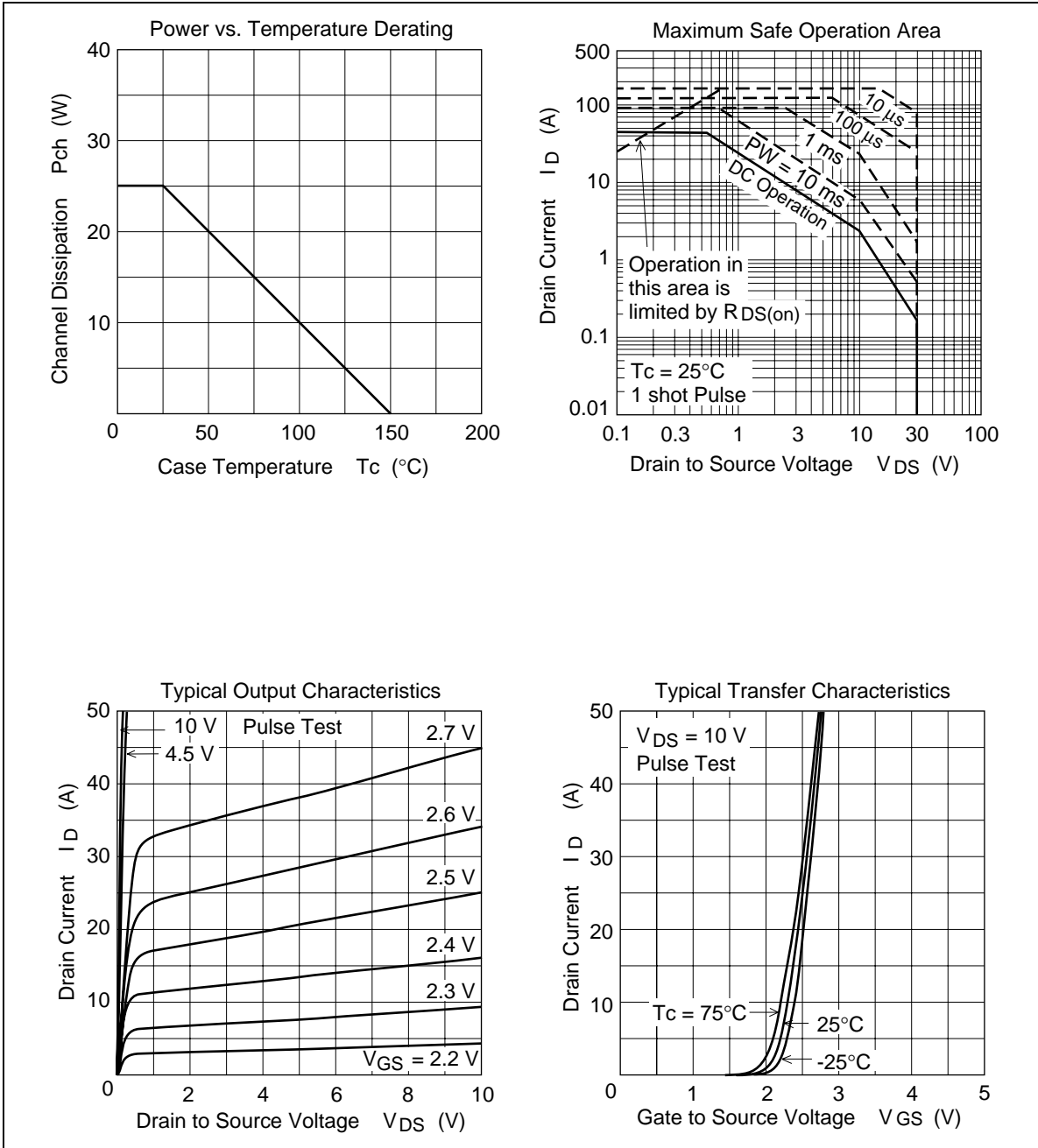
### Electrical Characteristics

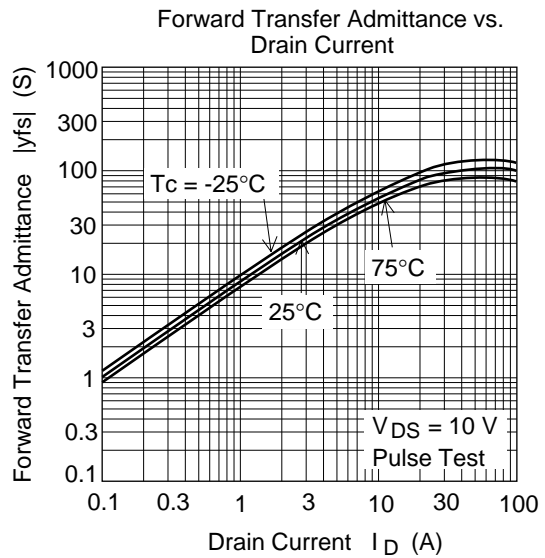
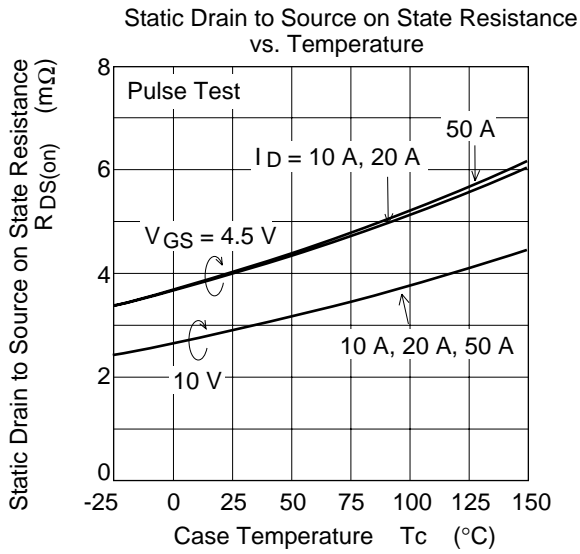
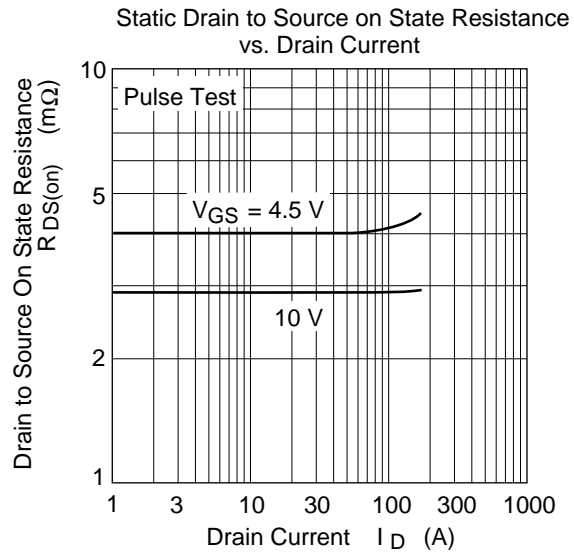
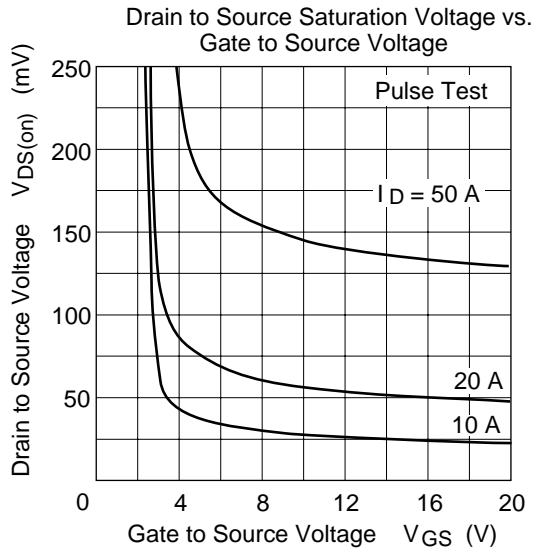
(T<sub>a</sub> = 25°C)

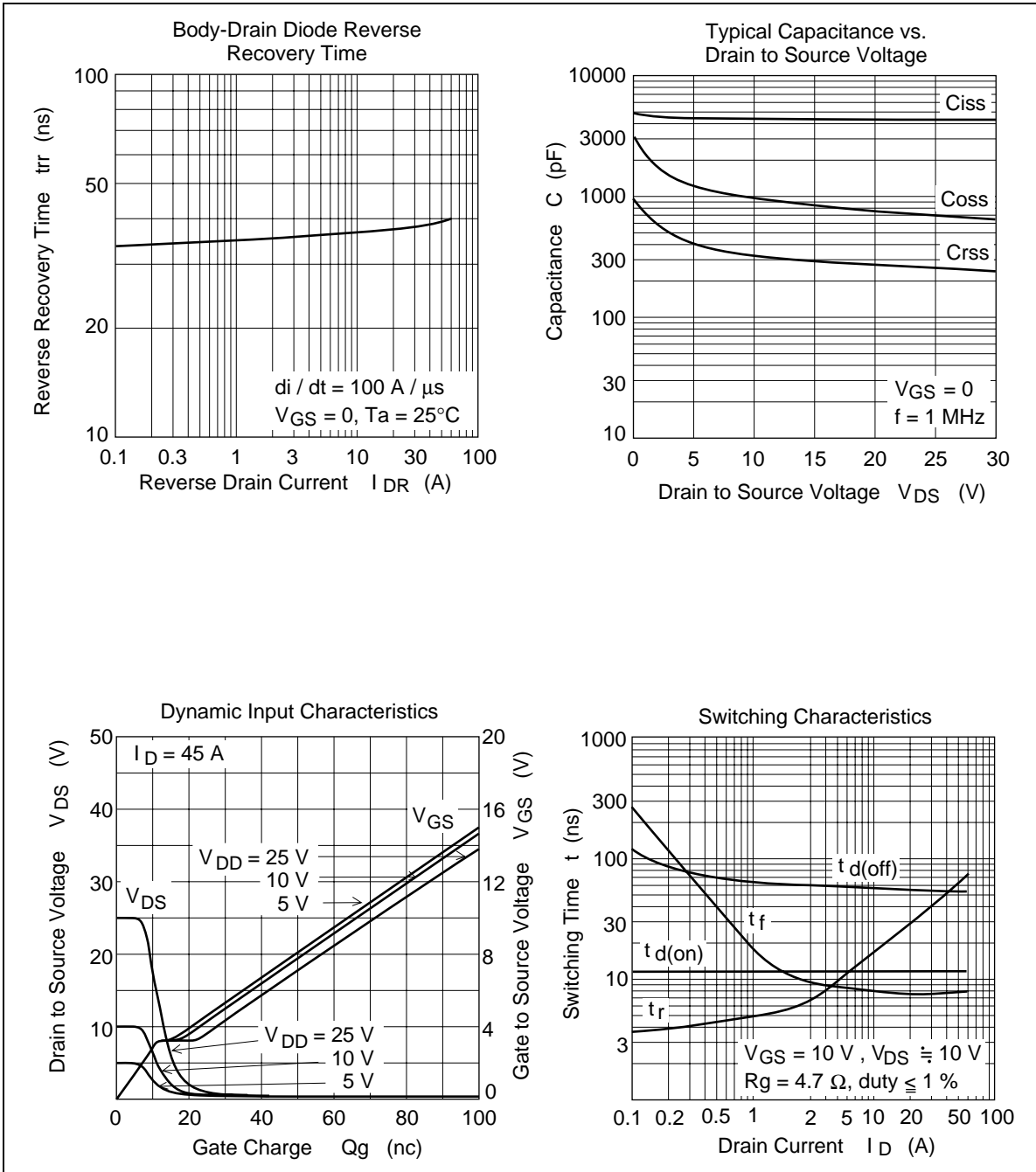
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	30	—	—	V	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0
Gate to source breakdown voltage	V <sub>(BR)GSS</sub>	± 20	—	—	V	I <sub>G</sub> = ±100 μA, V <sub>DS</sub> = 0
Gate to source leak current	I <sub>GSS</sub>	—	—	± 10	μA	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	1	μA	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0
Gate to source cutoff voltage	V <sub>GS(off)</sub>	1.6	—	2.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Static drain to source on state resistance	R <sub>DS(on)</sub>	—	2.9	3.8	mΩ	I <sub>D</sub> = 22.5 A, V <sub>GS</sub> = 10 V <sup>Note4</sup>
	R <sub>DS(on)</sub>	—	4.0	6.1	mΩ	I <sub>D</sub> = 22.5 A, V <sub>GS</sub> = 4.5 V <sup>Note4</sup>
Forward transfer admittance	y <sub>fs</sub>	52	87	—	S	I <sub>D</sub> = 22.5 A, V <sub>DS</sub> = 10 V <sup>Note4</sup>
Input capacitance	C <sub>iss</sub>	—	4400	—	pF	V <sub>DS</sub> = 10 V
Output capacitance	C <sub>oss</sub>	—	1000	—	pF	V <sub>GS</sub> = 0
Reverse transfer capacitance	C <sub>rss</sub>	—	330	—	pF	f = 1 MHz
Gate Resistance	R <sub>g</sub>	—	0.5	—	Ω	
Total gate charge	Q <sub>g</sub>	—	27	—	nc	V <sub>DD</sub> = 10 V
Gate to source charge	Q <sub>gs</sub>	—	12	—	nc	V <sub>GS</sub> = 4.5 V
Gate to drain charge	Q <sub>gd</sub>	—	5.9	—	nc	I <sub>D</sub> = 45 A
Turn-on delay time	t <sub>d(on)</sub>	—	12	—	ns	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 22.5 A
Rise time	t <sub>r</sub>	—	35	—	ns	V <sub>DD</sub> ≅ 10 V
Turn-off delay time	t <sub>d(off)</sub>	—	55	—	ns	R <sub>L</sub> = 0.44 Ω
Fall time	t <sub>f</sub>	—	7.5	—	ns	R <sub>g</sub> = 4.7 Ω
Body–drain diode forward voltage	V <sub>DF</sub>	—	0.83	1.08	V	I <sub>F</sub> = 45 A, V <sub>GS</sub> = 0 <sup>Note4</sup>
Body–drain diode reverse recovery time	t <sub>rr</sub>	—	37	—	ns	I <sub>F</sub> = 45 A, V <sub>GS</sub> = 0 diF/ dt = 100 A/ μs

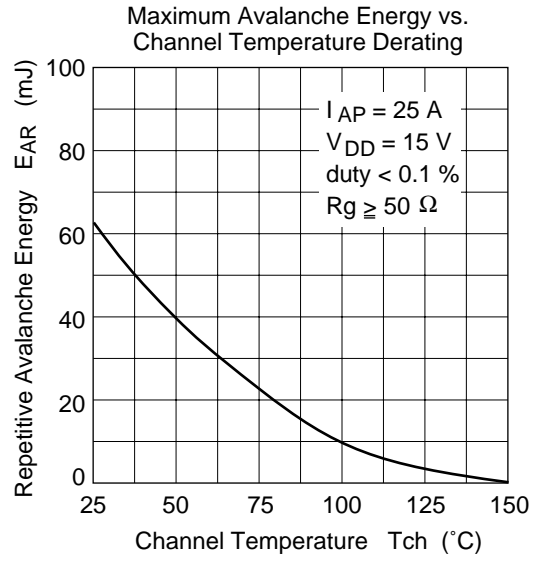
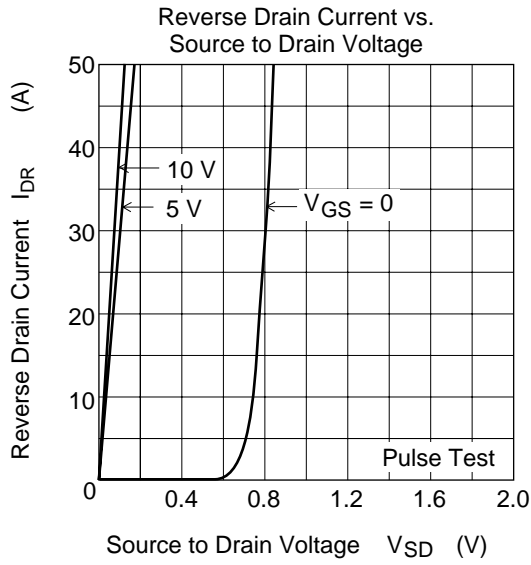
Notes: 4. Pulse test

Main Characteristics

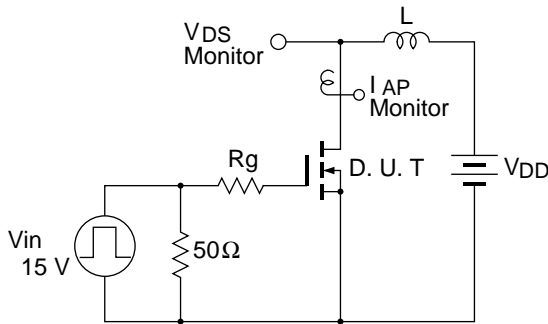






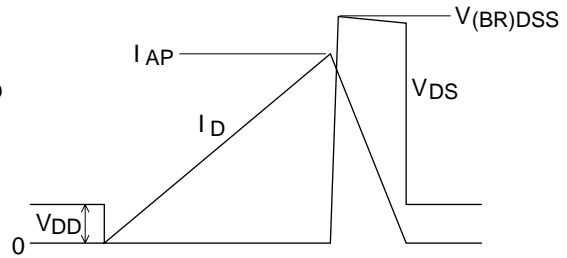


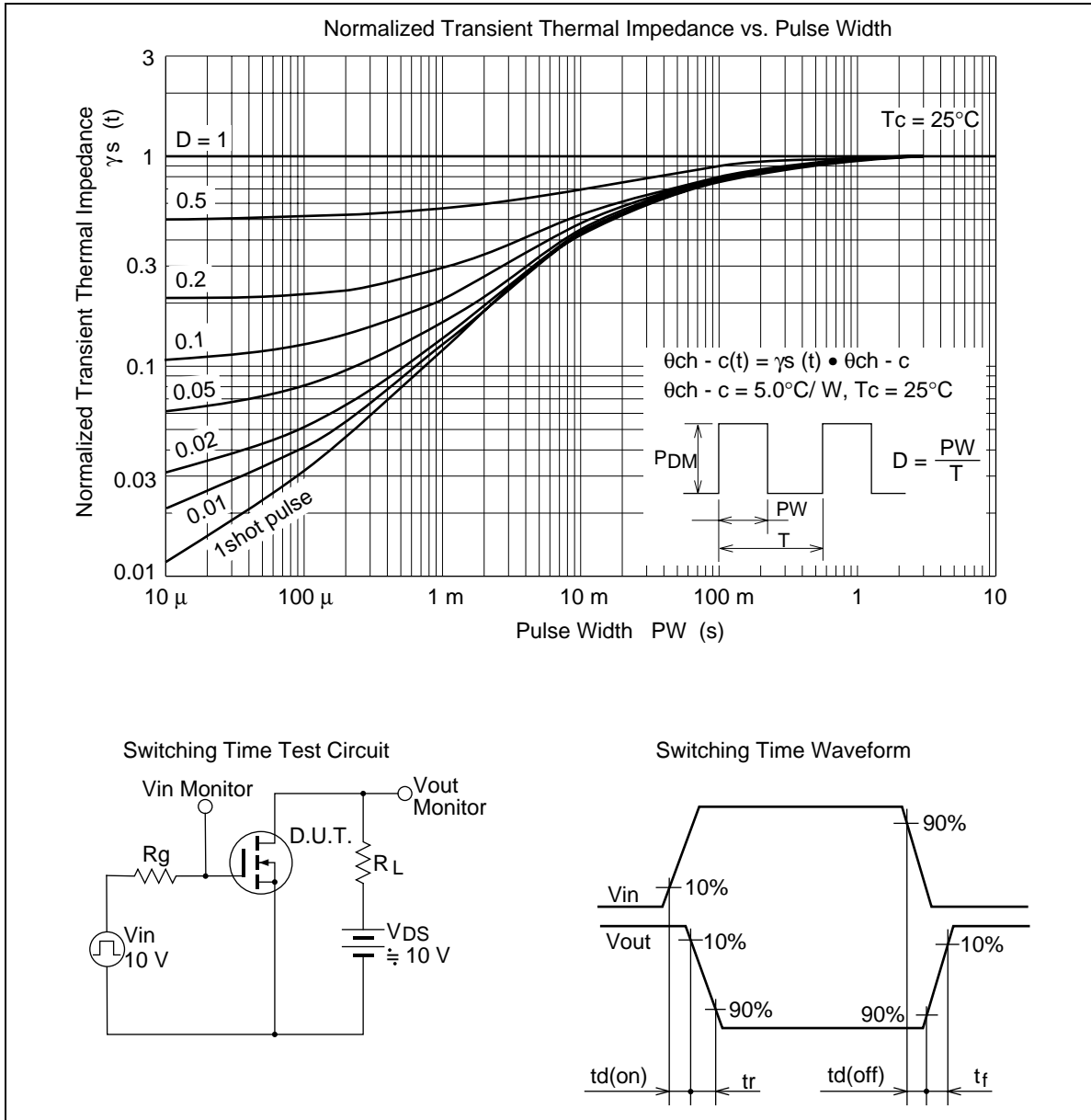
Avalanche Test Circuit



Avalanche Waveform

$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



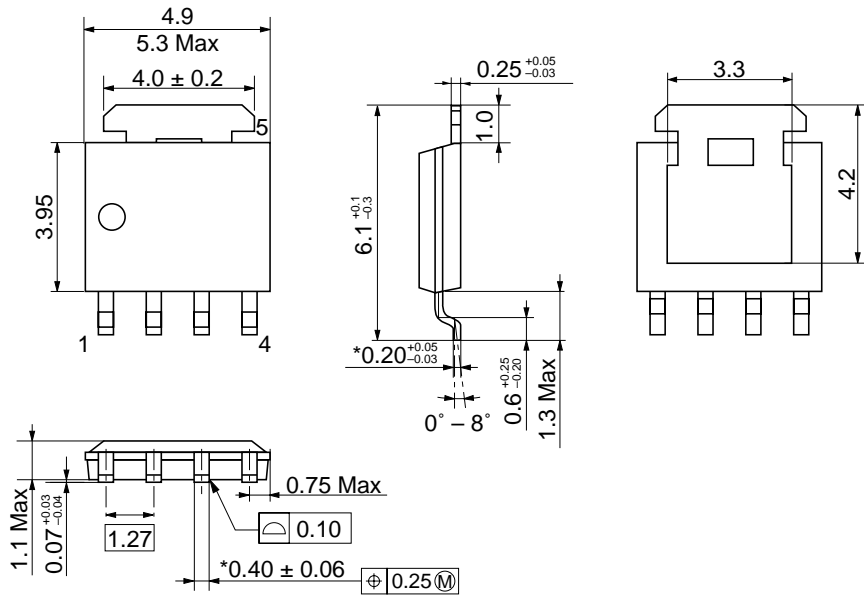




Package Dimensions

As of January, 2003

Unit: mm



\*Ni/Pd/Au plating

Package Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

**Renesas Technology Corp.** Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

---

**Keep safety first in your circuit designs!**

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.  
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

**Notes regarding these materials**

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
  2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
  3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors.  
Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (<http://www.renesas.com>).
  4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
  5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
  6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
  7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
  8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.
- 



<http://www.renesas.com>



Copyright © 2003. Renesas Technology Corporation, All rights reserved. Printed in Japan.  
Colophon 0.0