DS21Q43A
Quad E1 Framer

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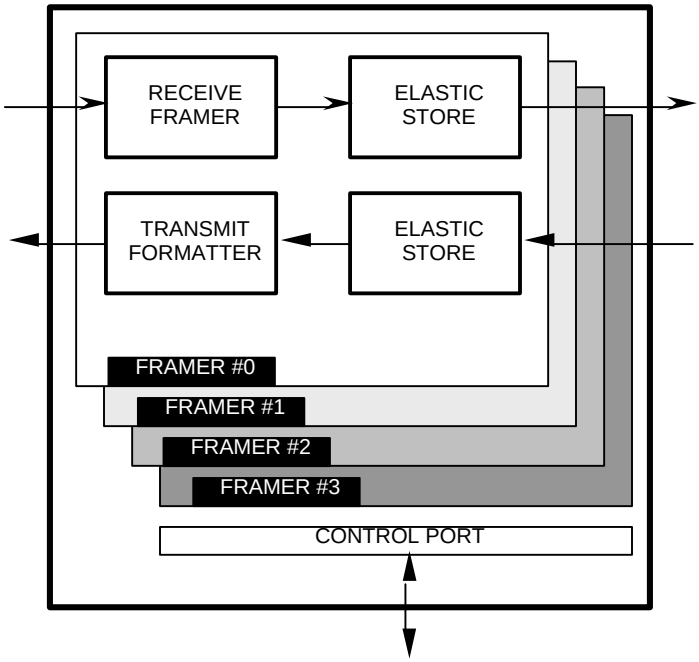
FEATURES

- Four E1 (CEPT or PCM-30) /ISDN-PRI framing transceivers
- All four framers are fully independent; transmit and receive sections of each framer are fully independent
- Frames to FAS, CAS, CCS, and CRC4 formats
- 8-bit parallel control port that can be connected to either multiplexed or non-multiplexed buses
- Each of the four framers contains dual two-frame elastic stores that can connect to asynchronous or synchronous backplanes up to 8.192 MHz
- Easy access to Si and Sa bits
- Extracts and inserts CAS signaling
- Large counters for bipolar and code violations, CRC4 code word errors, FAS word errors, and E-bits
- Programmable output clocks for Fractional E1, per channel loopback, H0 and H12 applications
- Detects and generates AIS, remote alarm, and remote multiframe alarms
- Pin-compatible with DS21Q41B Quad T1 Framer
- 5V supply; low power CMOS
- Available in 128-pin TQFP
- Industrial (-40°C to +85°C) grade version available (DS21Q43ATN)

FUNCTIONAL DIAGRAM



ACTUAL SIZE

DESCRIPTION

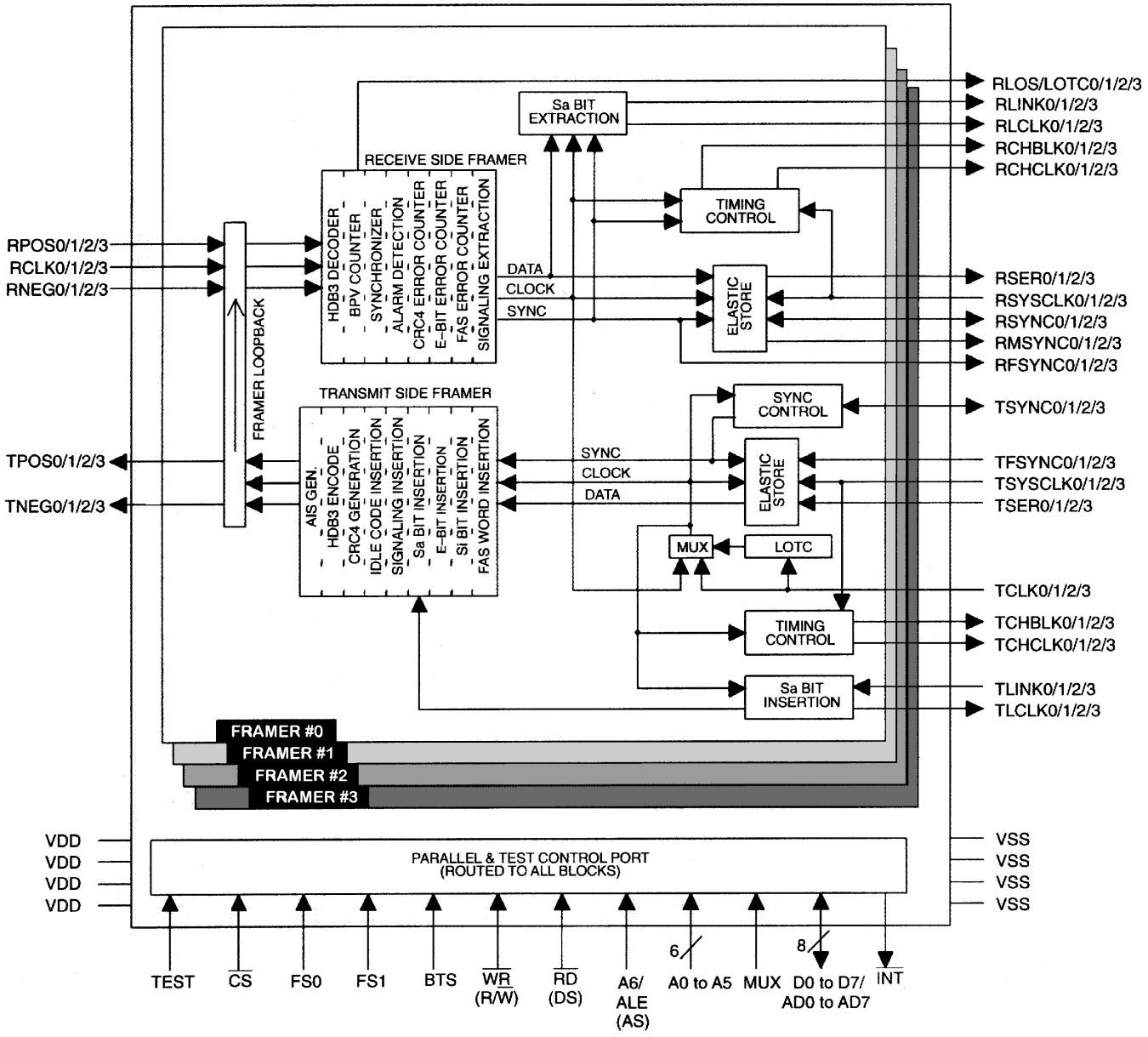
The DS21Q43A combines four of the popular DS2143 E1 Controllers onto a single monolithic die. The "A" designation denotes that some new features are available in the Quad version which were not available in the single E1 device. The added features in the DS21Q43A are listed in Section 1. The DS21Q43A offers a substantial space savings to applications that require more than one E1 framer on a card. The Quad version is only slightly bigger than the single E1 device. All four framers in the DS21Q43A are totally independent; they do not share a common framing synchronizer. Also, the transmit and receive sides of each framer are totally independent. The dual two-frame elastic stores contained in each of the four framers can be independently enabled and disabled as required. The DS21Q43A meets all of the latest specifications, including CCITT/ITU G.704, G.706, G.962, and I.431 as well as ETS 300 011 and ETS 300 233.

1.0 INTRODUCTION

The DS21Q43A Quad E1 Framer is made up of five main parts: framer #0, framer #1, framer #2, framer #3, and the control port which is shared by all four framers. See the Block Diagram in Figure 1-1. Each of the four framers within the DS21Q43A maintains the same register structure that appeared in the DS2143. The two framer-select inputs (FS0 and FS1) are used to determine which framer within the DS21Q43A is being accessed. In this manner, software written for the DS2143 can also be used in the DS21Q43A with only slight modifications. Several new features have been added to the framers in the DS21Q43A over the DS2143.

ADDED FEATURE	SECTION
Non-multiplexed parallel control port operation	2 and 13
Transmit side elastic store	10
Expanded access to Sa and Si bits	6
Control signals RFSYNC, RMSYNC, and TFSYNC	1
FAS word error counting	5
Code violation counting	5
Automatic AIS generation upon loss of frame sync	3
Automatic remote alarm generation	3
Per-channel signaling insertion	9 and 11
Per-channel loopback from RSER to TSER	8 and 11
Option to update error counters every 62.5 ms	5
CRC4 resync criteria met status bit	4
Elastic store reset	10
Hardware 3-state control	1

DS21Q43A BLOCK DIAGRAM Figure 1-1

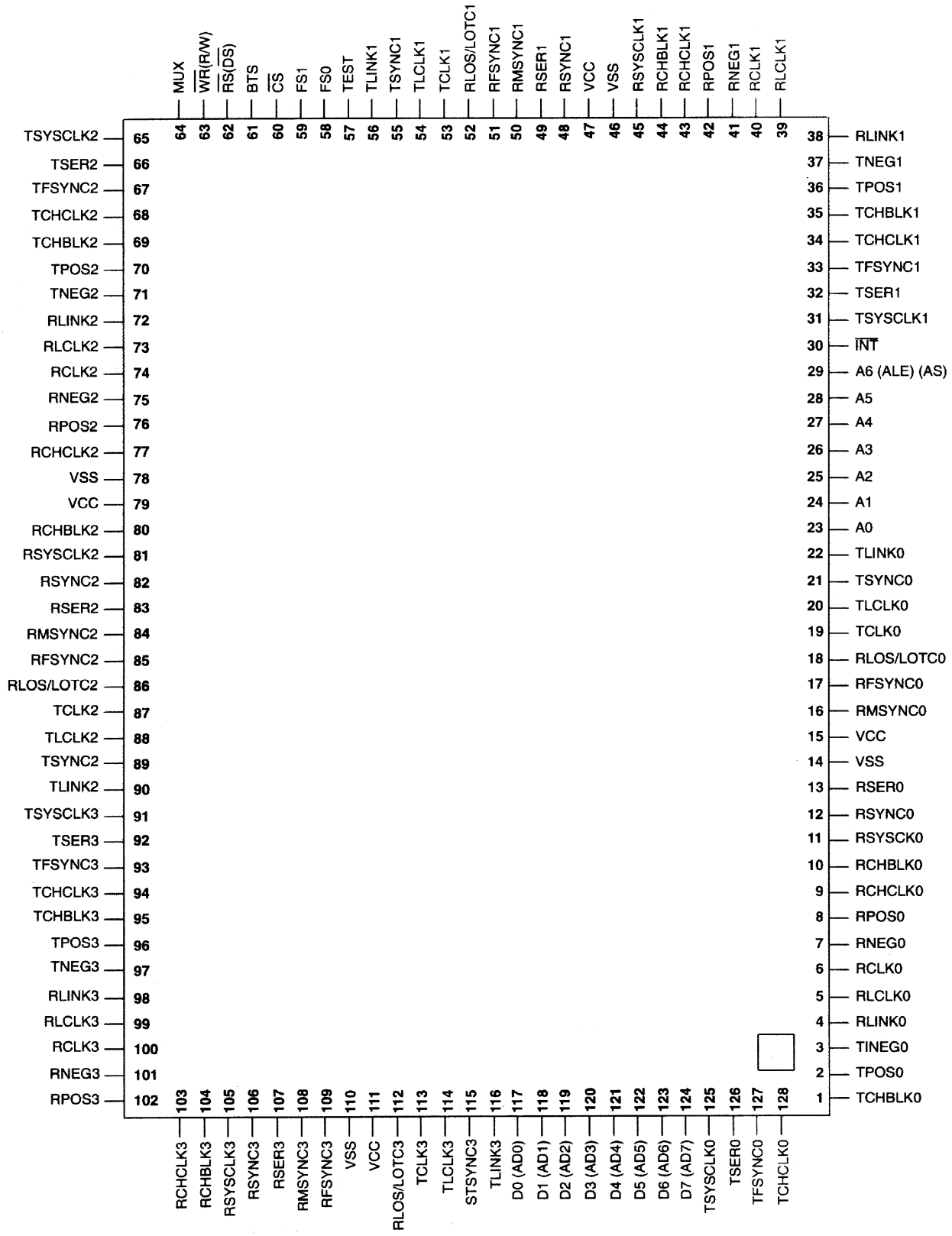


READER'S NOTE

This data sheet assumes a particular nomenclature of the E1 operating environment. There are 32 8-bit timeslots in an E1 system which are numbered 0 to 31. Timeslot 0 is transmitted first and received first. These 32 timeslots are also referred to as channels with a numbering scheme of 1 to 32. Timeslot 0 is identical to channel 1, timeslot 1 is identical to channel 2, and so on. Each timeslot (or channel) is made up of 8 bits which are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. Throughout this data sheet, the following abbreviations will be used:

FAS	Frame Alignment	CRC4	Cyclical Redundancy Check
CAS	Channel Associated Signaling	CCS	Common Channel Signaling
MF	Multiframe	Sa	Additional bits
Si	International bits	E-bit	CRC4 Error bits

PIN-OUT CONFIGURATION Figure 1-2



TRANSMIT PIN LIST Table 1-1

PIN	SYMBOL	TYPE	DESCRIPTION
19	TCLK0	I	Transmit Clock for Framer 0
53	TCLK1	I	Transmit Clock for Framer 1
87	TCLK2	I	Transmit Clock for Framer 2
113	TCLK3	I	Transmit Clock for Framer 3
126	TSER0	I	Transmit Serial Data for Framer 0
32	TSER1	I	Transmit Serial Data for Framer 1
66	TSER2	I	Transmit Serial Data for Framer 2
92	TSER3	I	Transmit Serial Data for Framer 3
128	TCHCLK0	O	Transmit Channel Clock from Framer 0
34	TCHCLK1	O	Transmit Channel Clock from Framer 1
68	TCHCLK2	O	Transmit Channel Clock from Framer 2
94	TCHCLK3	O	Transmit Channel Clock from Framer 3
1	TCHBLK0	O	Transmit Channel Block from Framer 0
35	TCHBLK1	O	Transmit Channel Block from Framer 1
69	TCHBLK2	O	Transmit Channel Block from Framer 2
95	TCHBLK3	O	Transmit Channel Block from Framer 3
20	TLCLK0	O	Transmit Link Clock from Framer 0
54	TLCLK1	O	Transmit Link Clock from Framer 1
88	TLCLK2	O	Transmit Link Clock from Framer 2
114	TLCLK3	O	Transmit Link Clock from Framer 3
22	TLINK0	I	Transmit Link Data for Framer 0
56	TLINK1	I	Transmit Link Data for Framer 1
90	TLINK2	I	Transmit Link Data for Framer 2
116	TLINK3	I	Transmit Link Data for Framer 3
2	TPOS0	O	Transmit Bipolar Data from Framer 0
36	TPOS1	O	Transmit Bipolar Data from Framer 1
70	TPOS2	O	Transmit Bipolar Data from Framer 2
96	TPOS3	O	Transmit Bipolar Data from Framer 3
3	TNEG0	O	Transmit Bipolar Data from Framer 0
37	TNEG1	O	Transmit Bipolar Data from Framer 1
71	TNEG2	O	Transmit Bipolar Data from Framer 2
97	TNEG3	O	Transmit Bipolar Data from Framer 3
21	TSYNC0	I/O	Transmit Sync for Framer 0
55	TSYNC1	I/O	Transmit Sync for Framer 1
89	TSYNC2	I/O	Transmit Sync for Framer 2
115	TSYNC3	I/O	Transmit Sync for Framer 3

127	TFSYNC0	I	Transmit Sync for Elastic Store in Framer 0
33	TFSYNC1	I	Transmit Sync for Elastic Store in Framer 1
67	TFSYNC2	I	Transmit Sync for Elastic Store in Framer 2
93	TFSYNC3	I	Transmit Sync for Elastic Store in Framer 3
125	TSYSCLK0	I	Transmit System Clock for Elastic Store in Framer 0
31	TSYSCLK1	I	Transmit System Clock for Elastic Store in Framer 1
65	TSYSCLK2	I	Transmit System Clock for Elastic Store in Framer 2
91	TSYSCLK3	I	Transmit System Clock for Elastic Store in Framer 3

RECEIVE PIN LIST Table 1-2

PIN	SYMBOL	TYPE	DESCRIPTION
6	RCLK0	I	Receive Clock for Framer 0
40	RCLK1	I	Receive Clock for Framer 1
74	RCLK2	I	Receive Clock for Framer 2
100	RCLK3	I	Receive Clock for Framer 3
13	RSER0	O	Receive Serial Data from Framer 0
49	RSER1	O	Receive Serial Data from Framer 1
83	RSER2	O	Receive Serial Data from Framer 2
107	RSER3	O	Receive Serial Data from Framer 3
9	RCHCLK0	O	Receive Channel Clock from Framer 0
43	RCHCLK1	O	Receive Channel Clock from Framer 1
77	RCHCLK2	O	Receive Channel Clock from Framer 2
103	RCHCLK3	O	Receive Channel Clock from Framer 3
10	RCHBLK0	O	Receive Channel Block from Framer 0
44	RCHBLK1	O	Receive Channel Block from Framer 1
80	RCHBLK2	O	Receive Channel Block from Framer 2
104	RCHBLK3	O	Receive Channel Block from Framer 3
5	RLCLK0	O	Receive Link Clock from Framer 0
39	RLCLK1	O	Receive Link Clock from Framer 1
73	RLCLK2	O	Receive Link Clock from Framer 2
99	RLCLK3	O	Receive Link Clock from Framer 3
4	RLINK0	O	Receive Link Data from Framer 0
38	RLINK1	O	Receive Link Data from Framer 1
72	RLINK2	O	Receive Link Data from Framer 2
98	RLINK3	O	Receive Link Data from Framer 3
8	RPOS0	I	Receive Bipolar Data for Framer 0
42	RPOS1	I	Receive Bipolar Data for Framer 1
76	RPOS2	I	Receive Bipolar Data for Framer 2

102	RPOS3	I	Receive Bipolar Data for Framer 3
7	RNEG0	I	Receive Bipolar Data for Framer 0
41	RNEG1	I	Receive Bipolar Data for Framer 1
75	RNEG2	I	Receive Bipolar Data for Framer 2
101	RNEG3	I	Receive Bipolar Data for Framer 3
12	RSYNC0	I/O	Receive Sync for Framer 0
48	RSYNC1	I/O	Receive Sync for Framer 1
82	RSYNC2	I/O	Receive Sync for Framer 2
106	RSYNC3	I/O	Receive Sync for Framer 3
17	RFSYNC0	O	Receive Frame Sync from Framer 0
51	RFSYNC1	O	Receive Frame Sync from Framer 1
85	RFSYNC2	O	Receive Frame Sync from Framer 2
109	RFSYNC3	O	Receive Frame Sync from Framer 3
16	RMSYNC0	O	Receive Multiframe Sync from Framer 0
50	RMSYNC1	O	Receive Multiframe Sync from Framer 1
84	RMSYNC2	O	Receive Multiframe Sync from Framer 2
108	RMSYNC3	O	Receive Multiframe Sync from Framer 3
11	RSYSCLK0	I	Receive System Clock for Elastic Store in Framer 0
45	RSYSCLK1	I	Receive System Clock for Elastic Store in Framer 1
81	RSYSCLK2	I	Receive System Clock for Elastic Store in Framer 2
105	RSYSCLK3	I	Receive System Clock for Elastic Store in Framer 3
18	RLOS/LOTC0	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 0
52	RLOS/LOTC1	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 1
86	RLOS/LOTC2	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 2
112	RLOS/LOTC3	O	Receive Loss of Sync/Loss of Transmit Clock from Framer 3

CONTROL PORT/TEST/SUPPLY PIN LIST Table 1-3

PIN	SYMBOL	TYPE	DESCRIPTION
57	TEST	I	3-State Control for all Output and I/O Pins.
60	$\overline{CS}$	I	Chip Select.
58	FS0	I	Framer Select 0 for Parallel Control Port.
59	FS1	I	Framer Select 1 for Parallel Control Port.
61	BTS	I	Bus Type Select for Parallel Control Port.
63	$\overline{WR}$ (R/$\overline{W}$)	I	Write Input (Read/Write).
62	$\overline{RD}$ (DS)	I	Read Input (Data Strobe).
23	A0	I	Address Bus Bit 0; LSB.
24	A1	I	Address Bus Bit 1.
25	A2	I	Address Bus Bit 2.
26	A3	I	Address Bus Bit 3.
27	A4	I	Address Bus Bit 4.
28	A5	I	Address Bus Bit 5.
29	A6 or ALE (AS)	I	Address Bus Bit 6; MSB or Address Latch Enable (Address Strobe).
30	$\overline{INT}$	O	Receive Alarm Interrupt for all Four Framers.
64	MUX	I	Non-Multiplexed or Multiplexed Bus Select.
117	D0 or AD0	I/O	Data Bus Bit 0 or Address/Data Bus Bit 0; LSB.
118	D1 or AD1	I/O	Data Bus Bit 1 or Address/Data Bus Bit 1.
119	D2 or AD2	I/O	Data Bus Bit 2 or Address/Data Bus Bit 2.
120	D3 or AD3	I/O	Data Bus Bit 3 or Address/Data Bus Bit 3.
121	D4 or AD4	I/O	Data Bus Bit 4 or Address/Data Bus Bit 4.
122	D5 or AD5	I/O	Data Bus Bit 5 or Address/Data Bus Bit 5.
123	D6 or AD6	I/O	Data Bus Bit 6 or Address/Data Bus Bit 6.
124	D7 or AD7	I/O	Data Bus Bit 7 or Address/Data Bus Bit 7; MSB.
15	V_{DD}	-	Positive Supply Voltage.
47	V_{DD}	-	Positive Supply Voltage.
79	V_{DD}	-	Positive Supply Voltage.
111	V_{DD}	-	Positive Supply Voltage.
14	V_{SS}	-	Signal Ground.
46	V_{SS}	-	Signal Ground.
78	V_{SS}	-	Signal Ground.
110	V_{SS}	-	Signal Ground.

DS21Q43A PIN DESCRIPTION Table 1-4

Transmit Clock [TCLK]. 2.048 MHz primary clock. Used to clock data through the transmit side formatter. Necessary for proper operation of the parallel control port.

Transmit Serial Data [TSER]. Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.

Transmit Channel Clock [TCHCLK]. 256 kHz clock which pulses high during the LSB of each channel. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for parallel to serial conversion of channel data. See Section 11 for timing details.

Transmit Bipolar Data [TPOS and TNEG]. Updated on rising edge of TCLK. Can be programmed to output NRZ data on TPOS via the TCR1.7 control bit.

Transmit Channel Block [TCHBLK]. A user programmable output that can be forced high or low during any of the 32 E1 channels. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384 kpbs service (H0), 1920 kpbs (H12), or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications and for per-channel loopback. See Section 11 for timing details.

Transmit System Clock [TSYSCLK]. 1.544 MHz or 2.048 MHz clock. Only used when the transmit side elastic store function is enabled. Should be tied low in applications that do not use the transmit side elastic store.

Transmit Link Clock [TLCLK]. 4 kHz to 20 kHz demand clock for the TLINK input. Controlled by TCR2. See Section 11 for timing details.

Transmit Link Data [TLINK]. If enabled via TCR2, this pin will be sampled on the falling edge of TCLK to insert data into the Sa bit positions. See Section 11 for timing details.

Transmit Sync [TSYNC]. A pulse at this pin will establish either frame or multiframe boundaries for the DS21Q43A. Via TCR1.1, the DS21Q43A can be programmed to output either a frame or multiframe pulse at this pin. See Section 11 for timing details.

Transmit Frame Sync [TFSYNC]. 8 kHz pulse. Only used when the transmit side elastic store is enabled. A pulse at this pin will establish frame boundaries for the DS21Q43A. Should be tied low in applications that do not use the transmit side elastic store. See Section 11 for timing details.

Receive Link Data [RLINK]. Updated with full received E1 data stream on the rising edge of RCLK. See Section 11 for timing details.

Receive Link Clock [RLCLK]. 4 kHz to 20 kHz demand clock for the RLINK output. Controlled by RCR2. See Section 11 for timing details. Necessary for proper operation of the parallel control port.

Receive Clock [RCLK]. 2.048 MHz primary clock. Used to clock data through the receive side of the framer. Necessary for proper operation of the parallel control port.

Receive Channel Clock [RCHCLK]. 256 kHz clock which pulses high during the LSB of each channel. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for parallel to serial conversion of channel data. See Section 11 for timing details.

Receive Channel Block [RCHBLK]. A user programmable output that can be forced high or low during any of the 32 E1 channels. Synchronous with RCLK when the transmit side elastic store is disabled. Synchronous with RSYSCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all E1 channels are used such as Fractional E1, 384 kpbs service (H0), 1920 kpbs (H12), or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications and for per-channel loopback. See Section 11 for timing details.

Receive Serial Data [RSER]. Received NRZ serial data. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.

Receive Sync [RSYNC]. An extracted pulse, one RCLK wide, is output at this pin which identifies either frame (RCR1.6=0) or multiframe boundaries (RCR1.6=1). If the receive side elastic store is enabled via RCR2.1, then this pin can be enabled to be an input at which a frame boundary pulse is applied. See Section 11 for timing details.

Receive Frame Sync [RFSYNC]. An extracted 8 kHz pulse, one RCLK wide, is output at this pin which identifies frame boundaries. See Section 11 for timing details.

Receive Multiframe Sync [RMSYNC]. Only used when the receive side elastic store is enabled. An extracted pulse, one RSYSCLK wide, is output at this pin which identifies either CAS or CRC4 multiframe boundaries. If the receive side elastic store is disabled, then this output should be ignored. See Section 11 for timing details.

Receive Bipolar Data Inputs [RPOS and RNEG]. Sampled on falling edge of RCLK. Tie together to receive NRZ data and disable bipolar violation monitoring circuitry.

Receive System Clock [RSYSCLK]. 1.544 MHz or 2.048 MHz clock. Only used when the elastic store function is enabled. Should be tied low in applications that do not use the elastic store. Allowing this pin to float can cause the device to 3-state its outputs.

Receive Loss of Sync/Loss of Transmit Clock [RLOS/LOTC]. A dual function output. If CCR1.6=0, then this pin will toggle high when the synchronizer is searching for the E1 frame or multiframe. If TCR2.0=1, then this pin will toggle high the TCLK pin has not been toggled for 5 µs.

Receive Alarm Interrupt [$\overline{\text{INT}}$]. Flags host controller during conditions defined in the Status Registers of the four framers. User can poll the Interrupt Status Register (ISR) to determine which status register in which framer is active (if any). Active low, open drain output.

3-State Control [TEST]. Set high to 3-state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board-level testing.

Bus Operation [MUX]. Set low to select non-multiplexed bus operation. Set high to select multiplexed bus operation.

Data Bus [D0 to D7] or Address/Data Bus [AD0 to AD7]. In non-multiplexed bus operation (MUX=0), serves as the data bus. In multiplexed bus operation (MUX=1), serves as an 8-bit multiplexed address/data bus.

Address Bus [A0 to A5]. In non-multiplexed bus operation (MUX=0), serves as the address bus. In multiplexed bus operation (MUX=1), these pins are not used and should be tied low.

Bus Type Select [BTS]. Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{RD}$ (DS), ALE(AS), and $\overline{WR}$ (R/$\overline{W}$) pins. If BTS=1, then these pins assume the function listed in parentheses ().

Read Input [$\overline{RD}$] (Data Strobe [DS]).

Framer Selects [FS0 and FS1]. Selects which of the four framers to be accessed.

Chip Selects [$\overline{CS}$]. Must be low to read or write to any of the four framers.

A6 or Address Latch Enable [ALE] (Address Strobe [AS]). In non-multiplexed bus operation (MUX=0), serves as the upper address bit. In multiplexed bus operation (MUX=1), serves to demultiplex the bus on a positive-going edge.

Write Input [$\overline{WR}$] (Read/Write [R/$\overline{W}$]).

Positive Supply [V_{DD}]. 5.0 volts ± 0.5 volts.

Signal Ground [V_{SS}]. 0.0 volts.

DS21Q43A FRAMER DECODE Table 1-5

FS1	FS0	FRAMER ACCESSED
0	0	#0
0	1	#1
1	0	#2
1	1	#3

DS21Q43A REGISTER MAP Table 1-6

ADDRESS	R/W	REGISTER NAME
00	R	BPV or Code Violation Count 1.
01	R	BPV or Code Violation Count 2
02	R	CRC4 Count 1/FAS Error Count 1.
03	R	CRC4 Error Count 2.
04	R	E-Bit Count 1/FAS Error Count 2.
05	R	E-Bit Count 2.
06	R	Status 1.
07	R	Status 2.
08	R/W	Receive Information.
09 to 0F	-	Not Used.
(2)	R	Interrupt Status Register.
10	R/W	Receive Control 1.
11	R/W	Receive Control 2.
12	R/W	Transmit Control 1.
13	R/W	Transmit Control 2.
14	R/W	Common Control 1.
15	R/W	Test 1.
16	R/W	Interrupt Mask.
17	R/W	Interrupt Mask.
18	R/W	Test 3.
19	R/W	Test 2.
1A	R/W	Common Control 2.
1B	R/W	Common Control 3.
1C	R/W	Transmit Sa Control Register.
1D	-	Not Used.
1E	R	Synchronizer Status.
1F	R	Receive Non-Align Frame.
20	R/W	Transmit Align Frame.
21	R/W	Transmit Non-Align Frame.
22	R/W	Transmit Channel Blocking 1.
23	R/W	Transmit Channel Blocking 2.
24	R/W	Transmit Channel Blocking 3.
25	R/W	Transmit Channel Blocking 4.
26	R/W	Transmit Idle 1.
27	R/W	Transmit Idle 2.
28	R/W	Transmit Idle 3.

29	R/W	Transmit Idle 4.
2A	R/W	Transmit Idle Definition.
2B	R/W	Receive Channel Blocking 1.
2C	R/W	Receive Channel Blocking 2.
2D	R/W	Receive Channel Blocking 3.
2E	R/W	Receive Channel Blocking 4.
2F	R/W	Receive Align Frame.
30	R	Receive Signaling 1.
31	R	Receive Signaling 2.
32	R	Receive Signaling 3.
33	R	Receive Signaling 4.
34	R	Receive Signaling 5.
35	R	Receive Signaling 6.
36	R	Receive Signaling 7.
37	R	Receive Signaling 8.
38	R	Receive Signaling 9.
39	R	Receive Signaling 10.
3A	R	Receive Signaling 11.
3B	R	Receive Signaling 12.
3C	R	Receive Signaling 13.
3D	R	Receive Signaling 14.
3E	R	Receive Signaling 15.
3F	R	Receive Signaling 16.
40	R/W	Transmit Signaling 1.
41	R/W	Transmit Signaling 2.
42	R/W	Transmit Signaling 3.
43	R/W	Transmit Signaling 4.
44	R/W	Transmit Signaling 5.
45	R/W	Transmit Signaling 6.
46	R/W	Transmit Signaling 7.
47	R/W	Transmit Signaling 8.
48	R/W	Transmit Signaling 9.
49	R/W	Transmit Signaling 10.
4A	R/W	Transmit Signaling 11.
4B	R/W	Transmit Signaling 12.
4C	R/W	Transmit Signaling 13.
4D	R/W	Transmit Signaling 14.
4E	R/W	Transmit Signaling 15.

4F	R/W	Transmit Signaling 16.
50	R/W	Transmit Si Bits Align Frame.
51	R/W	Transmit Si Bits Non-Align Frame.
52	R/W	Transmit Remote Alarm Bits.
53	R/W	Transmit Sa4 Bits.
54	R/W	Transmit Sa5 Bits.
55	R/W	Transmit Sa6 Bits.
56	R/W	Transmit Sa7 Bits.
57	R/W	Transmit Sa8 Bits.
58	R	Receive Si Bits Align Frame.
59	R	Receive Si Bits Non-Align Frame.
5A	R	Receive Remote Alarm Bits.
5B	R	Receive Sa4 Bits.
5C	R	Receive Sa5 Bits.
5D	R	Receive Sa6 Bits.
5E	R	Receive Sa7 Bits.
5F	R	Receive Sa8 Bits.

NOTES:

1. The Test Registers 1, 2, and 3 are used only by the factory; these registers must be cleared (set to all 0s) on power-up initialization to insure proper operation.
2. Any register address between 60h and 7Fh or between E0h and FFh will allow the status of the interrupts to appear on the bus.
3. Register addresses 09h through 0Fh are reserved for future use.

2.0 PARALLEL PORT

The DS21Q43A is controlled via either a non-multiplexed (MUX=0) or multiplexed (MUX=1) bus by an external microcontroller or microprocessor. The DS21Q43A can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parentheses (). See the timing diagrams in the AC Electrical Characteristics for more details.

3.0 CONTROL AND TEST REGISTERS

The operation of the DS21Q43A is configured via a set of seven registers. Typically, the control registers are only accessed when the system is powered up. Once the DS21Q43A has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Registers (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and three Common Control Registers (CCR1, CCR2 and CCR3). Each of the seven registers is described in this section.

The Test Registers at addresses 15, 18, and 19 hex are used by the factory in testing the DS21Q43A. On power-up, the Test Registers should be set to 00 hex in order for the DS21Q43A to operate properly.

RCR1: RECEIVE CONTROL REGISTER 1 (Address=10 Hex)

(MSB)							(LSB)
RSMF	RSM	RSIO	-	-	FRC	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
RSMF	RCR1.7	**RSYNC Multiframe Function.** Only used if the RSYNC pin is programmed in the multiframe mode (RCR1.6=1). 0=RSYNC outputs CAS multiframe boundaries. 1=RSYNC outputs CRC4 multiframe boundaries.
RSM	RCR1.6	**RSYNC Mode Select.** 0=frame mode (see the timing in Section 11). 1=multiframe mode (see the timing in Section 11).
RSIO	RCR1.5	**RSYNC I/O Select.** 0=RSYNC is an output (depends on RCR1.6). 1=RSYNC is an input (only valid if elastic store enabled). (note: this bit must be set to 0 when RCR2.1=0).
-	RCR1.4	**Not Assigned.** Should be set to 0 when written.
-	RCR1.3	**Not Assigned.** Should be set to 0 when written.
FRC	RCR1.2	**Frame Resync Criteria.** 0=resync if FAS received in error 3 consecutive times. 1=resync if FAS or bit 2 of non-FAS is received in error 3 consecutive times.
SYNCE	RCR1.1	**Sync Enable.** 0=auto resync enabled. 1=auto resync disabled.
RESYNC	RCR1.0	**Resync.** When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync.

SYNC/RESYNC CRITERIA Table 3-1

FRAME OR MULTI-FRAME LEVEL	SYNC CRITERIA	RESYNC CRITERIA	ITU SPEC.
FAS	FAS present in frame N and N+2, and FAS not present in frame N + 1	Three consecutive incorrect FAS received Alternate (RCR1.2=1) the above criteria is met or three consecutive incorrect bit 2 of non-FAS received	G.706 4.1.1 4.1.2
CRC4	Two valid MF alignment words found within 8 ms	915 or more CRC4 code words out of 1000 received in error	G.706 4.2 and 4.3.2
CAS	Valid MF alignment word found and previous timeslot 16 contains code other than all 0s	Two consecutive MF alignment words received in error	G.732 5.2

RCR2: RECEIVE CONTROL REGISTER 2 (Address=11 Hex)

(MSB) **(LSB)**

Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	RBCS	RESE	-

SYMBOL	POSITION	NAME AND DESCRIPTION
Sa8S	RCR2.7	**Sa8 Bit Select.** Set to 1 to report the Sa8 bit at the RLINK pin; set to 0 to not report the Sa8 bit.
Sa7S	RCR2.6	**Sa7 Bit Select.** Set to 1 to report the Sa7 bit at the RLINK pin; set to 0 to not report the Sa7 bit.
Sa6S	RCR2.5	**Sa6 Bit Select.** Set to 1 to report the Sa6 bit at the RLINK pin; set to 0 to not report the Sa6 bit.
Sa5S	RCR2.4	**Sa5 Bit Select.** Set to 1 to report the Sa5 bit at the RLINK pin; set to 0 to not report the Sa5 bit.
Sa4S	RCR2.3	**Sa4 Bit Select.** Set to 1 to report the Sa4 bit at the RLINK pin; set to 0 to not report the Sa4 bit.
RBCS	RCR2.2	**Receive Side Backplane Clock Select.** 0=if RSYSCLK is 1.544 MHz 1=if RSYSCLK is 2.048 MHz
RESE	RCR2.1	**Receive Side Elastic Store Enable.** 0=elastic store is bypassed 1=elastic store is enabled
-	RCR2.0	**Not Assigned.** Should be set to 0 when written.

TCR1: TRANSMIT CONTROL REGISTER 1 (Address=12 Hex)

(MSB)							(LSB)
ODF	TFPT	T16S	TUA1	TSiS	TSA1	TSM	TSIO

SYMBOL	POSITION	NAME AND DESCRIPTION
ODF	TCR1.7	**Output Data Format.** 0=bipolar data at TPOS and TNEG 1=NRZ data at TPOS; TNEG=0
TFPT	TCR1.6	**Transmit Timeslot 0 Pass Through.** 0=FAS bits/Sa bits/Remote Alarm sourced internally from the TAF and TNAF registers 1=FAS bits/Sa bits/Remote Alarm sourced from TSER
T16S	TCR1.5	**Transmit Timeslot 16 Data Select.** 0=sample timeslot 16 at TSER pin 1=source timeslot 16 from TS0 to TS15 registers
TUA1	TCR1.4	**Transmit Unframed All 1s.** 0=transmit data normally 1=transmit an unframed all 1s code at TPOS and TNEG
TSiS	TCR1.3	**Transmit International Bit Select.** 0=sample Si bits at TSER pin 1=source Si bits from TAF and TNAF registers (in this mode, TCR1.6 must be set to 0)
TSA1	TCR1.2	**Transmit Signaling All 1s.** 0=normal operation 1=force timeslot 16 in every frame to all 1s
TSM	TCR1.1	**TSYNC Mode Select**. 0=frame mode (see the timing in Section 11) 1=CAS and CRC4 multiframe mode (see the timing in Section 11)
TSIO	TCR1.0	**TSYNC I/O Select.** 0=TSYNC is an input 1=TSYNC is an output

NOTE:

1. See Figure 11-9 for more details about how the Transmit Control Registers affect the operation of the DS21Q43A.

TCR2: TRANSMIT CONTROL REGISTER 2 (Address=13 Hex)

(MSB)							(LSB)
Sa8S	Sa7S	Sa6S	Sa5S	Sa4S	ODM	AEBE	PF

SYMBOL	POSITION	NAME AND DESCRIPTION
Sa8S	TCR2.7	**Sa8 Bit Select.** Set to 1 to source the Sa8 bit from the TLINK pin; set to 0 to not source the Sa8 bit.
Sa7S	TCR2.6	**Sa7 Bit Select.** Set to 1 to source the Sa7 bit from the TLINK pin; set to 0 to not source the Sa7 bit.
Sa6S	TCR2.5	**Sa6 Bit Select.** Set to 1 to source the Sa6 bit from the TLINK pin; set to 0 to not source the Sa6 bit.
Sa5S	TCR2.4	**Sa5 Bit Select**. Set to 1 to source the Sa5 bit from the TLINK pin; set to 0 to not source the Sa5 bit.
Sa4S	TCR2.3	**Sa4 Bit Select.** Set to 1 to source the Sa4 bit from the TLINK pin; set to 0 to not source the Sa4 bit.
ODM	TCR2.2	**Output Data Mode.** 0=pulses at TPOS and TNEG are one full TCLK period wide 1=pulses at TPOS and TNEG are 1/2 TCLK period wide
AEBE	TCR2.1	**Automatic E-Bit Enable.** 0=E-bits not automatically set in the transmit direction 1=E-bits automatically set in the transmit direction.
PF	TCR2.0	**Function of RLOS/LOTC Pin.** 0=Receive Loss of Sync (RLOS) 1=Loss of Transmit Clock (LOTC)

CCR1: COMMON CONTROL REGISTER 1 (Address=14 Hex)

(MSB)							(LSB)
FLB	THDB3	TG802	TCRC4	RSM	RHDB3	RG802	RCRC4

SYMBOL	POSITION	NAME AND DESCRIPTION
FLB	CCR1.7	**Framer Loopback.** 0=loopback disabled 1=loopback enabled
THDB3	CCR1.6	**Transmit HDB3 Enable.** 0=HDB3 disabled 1=HDB3 enabled
TG802	CCR1.5	**Transmit G.802 Enable.** See Section 11 for details. 0=do not force TCHBLK high during bit 1 of timeslot 26 1=force TCHBLK high during bit 1 of timeslot 26
TCRC4	CCR1.4	**Transmit CRC4 Enable.** 0=CRC4 disabled 1=CRC4 enabled
RSM	CCR1.3	**Receive Signaling Mode Select.** 0=CAS signaling mode 1=CCS signaling mode
RHDB3	CCR1.2	**Receive HDB3 Enable.** 0=HDB3 disabled 1=HDB3 enabled
RG802	CCR1.1	**Receive G.802 Enable.** See Section 11 for details. 0=do not force RCHBLK high during bit 1 of timeslot 26 1=force RCHBLK high during bit 1 of timeslot 26
RCRC4	CCR1.0	**Receive CRC4 Enable.** 0=CRC4 disabled 1=CRC4 enabled

FRAMER LOOPBACK

When CCR1.7 is set to a 1, the DS21Q43A will enter a Framer LoopBack (FLB) mode. This loopback is useful in testing and debugging applications. In FLB, the DS21Q43A will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

1. data will be transmitted as normal at TPOS and TNEG
2. data at RPOS and RNEG will be ignored
3. the receive side signals become synchronous with TCLK instead of RCLK.

CCR2: COMMON CONTROL REGISTER 2 (Address=1A Hex)

(MSB)							(LSB)
ECUS	VCRFS	AAIS	ARA	RSERC	LOTCMC	-	-

SYMBOL	POSITION	NAME AND DESCRIPTION
ECUS	CCR2.7	**Error Counter Update Select.** 0=update error counters once a second 1=update error counters every 62.5 ms (500 frames)
VCRFS	CCR2.6	**VCR Function Select**. 0=count BiPolar Violations (BPVs) 1=count Code Violations (CVs)
AAIS	CCR2.5	**Automatic AIS Generation**. 0=disabled 1=enabled
ARA	CCR2.4	**Automatic Remote Alarm Generation.** 0=disabled 1=enabled
RSERC	CCR2.3	**RSER Control.** 0=allow RSER to output data as received under all conditions 1=force RSER to 1 under loss of frame alignment conditions
LOTCMC	CCR2.2	**Loss of Transmit Clock Mux Control.** Determines whether the transmit side formatter should switch to the ever-present RCLK if the TCLK should fail to transition (see Figure 1-1). 0=do not switch to RCLK if TCLK stops 1=switch to RCLK if TCLK stops
-	CCR2.1	**Not Assigned.** Should be set to 0 when written.
-	CCR2.0	**Not Assigned.** Should be set to 0 when written.

AUTOMATIC ALARM GENERATION

When either CCR2.4 or CCR2.5 is set to 1, the DS21Q43A monitors the receive side to determine if any of the following conditions are present: loss of receive frame synchronization, AIS alarm (all 1s) reception, or loss of receive carrier (or signal). If any one (or more) of the above conditions is present, then the DS21Q43A will either force an AIS alarm (if CCR2.5=1) or a Remote Alarm (CCR2.4=1) to be transmitted via the TPOS and TNEG pins. It is an illegal state to have both CCR2.4 and CCR2.5 set to 1 at the same time.

CCR3: COMMON CONTROL REGISTER 3 (Address=1B Hex)

(MSB)							(LSB)
TESE	TCBFS	TIRFS	ESR	LIRST	-	TBCS	-

SYMBOL	POSITION	NAME AND DESCRIPTION
TESE	CCR3.7	**Transmit Side Elastic Store Enable.** 0=elastic store is bypassed. 1=elastic store is enabled.
TCBFS	CCR3.6	**Transmit Channel Blocking Registers (TCBR) Function Select.** 0=TCBRs define the operation of the TCHBLK output pin. 1=TCBRs define which signaling bits are to be inserted.
TIRFS	CCR3.5	**Transmit Idle Registers (TIR) Function Select.** 0=TIRs define in which channels to insert idle code. 1=TIRs define in which channels to insert data from RSER.
ESR	CCR3.4	**Elastic Stores Reset.** Setting this bit from a 1 to a 0 will force the elastic stores to a known depth. Should be toggled after RSYSCLK and TSYSCLK have been applied and are stable. Must be set and cleared again for a subsequent reset. Do not leave this bit set high.
-	CCR3.3	**Not Assigned.** Should be set to 0 when written.
-	CCR3.2	**Not Assigned.** Should be set to 0 when written.
TBCS	CCR3.1	**Transmit Side Backplane Clock Select.** 0=if TSYSCLK is 1.544 MHz 1=if TSYSCLK is 2.048 MHz
-	CCR3.0	**Not Assigned.** Should be set to 0 when written.

POWER-UP SEQUENCE

On power-up, after the supplies are stable, the DS21Q43A should be configured for operation by writing to all of the internal registers (this includes the Test Registers) since the contents of the internal registers cannot be predicted on power-up. Finally, after the RSYSCLK and TSYSCLK inputs are stable, the ESR bit should be toggled from a 0 to a 1 and then back to 0 (this step can be skipped if the elastic store is not being used).

4.0 STATUS AND INFORMATION REGISTERS

There is a set of four registers that contain information on the current real time status of the DS21Q43A, Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Register (RIR), and Synchronizer Status Register (SSR). When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a 1. All of the bits in these registers operate in a latched fashion (except for the SSR).

This means that if an event occurs and a bit is set to a 1 in any of the registers, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again or if the alarm is still present.

The user will always precede a read of the SR1, SR2, and RIR registers with a write. The byte written to the register will inform the DS21Q43A which bits the user wishes to read and have cleared. The user will write a byte to one of these three registers, with a 1 in the bit positions he or she wishes to read and a 0 in the bit positions he or she does not wish to obtain the latest information. When a 1 is written to a bit location, the read register will be updated with current value and it will be cleared. When a 0 is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically AND'ed with the mask byte that was just written and this value should be written back into the same register to insure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This write-read-write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS21Q43A with higher-order software languages.

The SSR register operates differently than the other three. It is a read only register and it reports the status of the synchronizer in real time. This register is not latched and it is not necessary to precede a read of this register with a write.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt via the $\overline{\text{INT}}$ pin. All four of the framers share the $\overline{\text{INT}}$ output. Each of the alarms and events in the SR1 and SR2 can be either masked or unmasked from the interrupt pins via the Interrupt Mask Register 1 (IMR1) and Interrupt Mask Register 2 (IMR2) respectively. The user can determine which framer has active interrupts by polling the Interrupt Status Register (ISR).

ISR: INTERRUPT STATUS REGISTER (see Table 1-6, Note 2)

(MSB)							(LSB)
F3SR2	F3SR1	F2SR2	F2SR1	F1SR2	F1SR1	F0SR2	F0SR1

SYMBOL	POSITION	NAME AND DESCRIPTION
F3SR2	ISR.7	**Status of Interrupt for SR2 in Framer 3.** 1=interrupt active.
F3SR1	ISR.6	**Status of Interrupt for SR1 in Framer 3.** 1=interrupt active.
F2SR2	ISR.5	**Status of Interrupt for SR2 in Framer 2.** 1=interrupt active.
F2SR1	ISR.4	**Status of Interrupt for SR1 in Framer 2.** 1=interrupt active.
F1SR2	ISR.3	**Status of Interrupt for SR2 in Framer 1.** 1=interrupt active.
F1SR1	ISR.2	**Status of Interrupt for SR1 in Framer 1.** 1=interrupt active.
F0SR2	ISR.1	**Status of Interrupt for SR2 in Framer 0.** 1=interrupt active.
F0SR1	ISR.0	**Status of Interrupt for SR1 in Framer 0.** 1=interrupt active.

RIR: RECEIVE INFORMATION REGISTER (Address=08 Hex)

(MSB)							(LSB)
TESF	TESE	LORC	RESF	RESE	CRCRC	FASRC	CASRC

SYMBOL	POSITION	NAME AND DESCRIPTION
TESF	RIR.7	**Transmit Side Elastic Store Full.** Set when the elastic store buffer fills and a frame is deleted.
TESE	RIR.6	**Transmit Side Elastic Store Empty.** Set when the elastic store buffer empties and a frame is repeated.
LORC	RIR.5	**Loss of Receive Clock.** Set when the RCLK pin has not transitioned for at least 2 µs (3 µs ± 1 µs).
RESF	RIR.4	**Receive Side Elastic Store** Full. Set when the elastic store buffer fills and a frame is deleted.
RESE	RIR.3	**Receive Side Elastic Store Empty.** Set when the elastic store buffer empties and a frame is repeated.
CRCRC	RIR.2	**CRC Resync Criteria Met.** Set when 915/1000 code words are received in error.
FASRC	RIR.1	**FAS Resync Criteria Met.** Set when 3 consecutive FAS words are received in error.
CASRC	RIR.0	**CAS Resync Criteria Met.** Set when 2 consecutive CAS MF alignment words are received in error.

SSR: SYNCHRONIZER STATUS REGISTER (Address=1E Hex)

(MSB)							(LSB)
CSC5	CSC4	CSC3	CSC2	CSC0	FASSA	CASSA	CRC4SA

SYMBOL	POSITION	NAME AND DESCRIPTION
CSC5	SSR.7	**CRC4 Sync Counter Bit 5.** MSB of the 6-bit counter.
CSC4	SSR.6	**CRC4 Sync Counter Bit 4.**
CSC3	SSR.5	**CRC4 Sync Counter Bit 3.**
CSC2	SSR.4	**CRC4 Sync Counter Bit 2.**
CSC0	SSR.3	**CRC4 Sync Counter Bit 0.** LSB of the 6-bit counter. The next to LSB is not accessible.
FASSA	SSR.2	**FAS Sync Active.** Set while the synchronizer is searching for alignment at the FAS level.
CASSA	SSR.1	**CAS MF Sync Active.** Set while the synchronizer is searching for the CAS MF alignment word.
CRC4SA	SSR.0	**CRC4 MF Sync Active.** Set while the synchronizer is searching for the CRC4 MF alignment word.

CRC4 SYNC COUNTER

The CRC4 Sync Counter increments each time the 8 ms CRC4 multiframe search times out. The counter is cleared when the DS21Q43A has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling the CRC4 mode (CCR1.0=0). This counter is useful for determining the amount of time the DS21Q43A has been searching for synchronization at the CRC4 level. Annex B of ITU G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400 ms, then the search should be abandoned and proper action taken. The CRC4 Sync Counter will rollover.

SR1: STATUS REGISTER 1 (Address=06 Hex)

(MSB)							(LSB)
RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
RSA1	SR1.7	**Receive Signaling All Ones.** Set when the contents of timeslot 16 contains less than three 0s over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode.
RDMA	SR1.6	**Receive Distant MF Alarm.** Set when bit 6 of timeslot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode.
RSA0	SR1.5	**Receive Signaling All 0s.** Set when over a full MF, timeslot 16 contains all 0s.
RSLIP	SR1.4	**Receive Side Elastic Store Slip.** Set when the elastic store has either repeated or deleted a frame of data.
RUA1	SR1.3	**Receive Unframed All Ones.** Set when an unframed all ones code is received at RPOS and RNEG.
RRA	SR1.2	**Receive Remote Alarm.** Set when a remote alarm is received at RPOS and RNEG.
RCL	SR1.1	**Receive Carrier Loss.** Set when 255 consecutive 0s have been detected at RPOS and RNEG.
RLOS	SR1.0	**Receive Loss of Sync.** Set when the device is not synchronized to the receive E1 stream.

ALARM CRITERIA Table 4-1

ALARM	SET CRITERIA	CLEAR CRITERIA	ITU SPEC.
RSA1 (receive signaling all ones)	over 16 consecutive frames (one full MF) timeslot 16 contains less than three 0s	over 16 consecutive frames (one full MF) timeslot 16 contains three or more 0s	G.732 4.2
RSA0 (receive signaling all 0s)	over 16 consecutive frames (one full MF) timeslot 16 contains all 0s	over 16 consecutive frames (one full MF) timeslot 16 contains at least a single one	G.732 5.2
RDMA (receive distant multiframe alarm)	bit 6 in timeslot 16 of frame 0 set to 1 for two consecutive MFs	bit 6 in timeslot 16 of frame 0 set to 0 for two consecutive MFs	O.162 2.1.5
RUA1 (receive unframed all ones)	less than three 0s in two frames (512 bits)	more than two 0s in two frames (512 bits)	O.162 1.6.1.2
RRA (receive remote alarm)	bit 3 of non-align frame set to 1 for three consecutive occasions	bit 3 of non-align frame set to 0 for three consecutive occasions	O.162 2.1.4
RCL (receive carrier loss)	255 consecutive 0s received	in 255-bit times, at least 32 1s are received	G.775

SR2: STATUS REGISTER 2 (Address=07 Hex)

(MSB)							(LSB)
RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	TSLIP

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	SR2.7	**Receive CAS Multiframe**. Set every 2 ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries. Used to alert the host that signaling data is available.
RAF	SR2.6	**Receive Align Frame**. Set every 250 µs at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers.
TMF	SR2.5	**Transmit Multiframe**. Set every 2 ms (regardless if CRC4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.
SEC	SR2.4	**One Second Timer**. Set on increments of 1 second based on RCLK. If CCR2.7=1, then this bit will be set every 62.5 ms instead of once a second.
TAF	SR2.3	**Transmit Align Frame**. Set every 250 µs at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated.
LOTC	SR2.2	**Loss of Transmit Clock**. Set when the TCLK pin has not transitioned for one channel time (or 3.9 µs). Will force the LOTC pin high if enabled via TCR2.0. Based on RCLK.
RCMF	SR2.1	**Receive CRC4 Multiframe**. Set on CRC4 multiframe boundaries; will continue to be set every 2 ms on an arbitrary boundary if CRC4 is disabled.
TSLIP	SR2.0	**Transmit Elastic Store Slip.** Set when the elastic store has either repeated or deleted a frame of data.

IMR1: INTERRUPT MASK REGISTER 1 (Address=16 Hex)

(MSB)							(LSB)
RSA1	RDMA	RSA0	RSLIP	RUA1	RRA	RCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
RSA1	IMR1.7	**Receive Signaling All 1s**. 0=interrupt masked 1=interrupt enabled
RDMA	IMR1.6	**Receive Distant MF Alarm**. 0=interrupt masked 1=interrupt enabled
RSA0	IMR1.5	**Receive Signaling All 0s**. 0=interrupt masked 1=interrupt enabled
RSLIP	IMR1.4	**Receive Elastic Store Slip Occurrence**. 0=interrupt masked 1=interrupt enabled
RUA1	IMR1.3	**Receive Unframed All 1s**. 0=interrupt masked 1=interrupt enabled
RRA	IMR1.2	**Receive Remote Alarm**. 0=interrupt masked 1=interrupt enabled
RCL	IMR1.1	**Receive Carrier Loss**. 0=interrupt masked 1=interrupt enabled
RLOS	IMR1.0	**Receive Loss of Sync**. 0=interrupt masked 1=interrupt enabled

IMR2: INTERRUPT MASK REGISTER 2 (Address=17 Hex)

(MSB)							(LSB)
RMF	RAF	TMF	SEC	TAF	LOTC	RCMF	TSLIP

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	IMR2.7	**Receive CAS Multiframe.** 0=interrupt masked 1=interrupt enabled
RAF	IMR2.6	**Receive Align Frame.** 0=interrupt masked 1=interrupt enabled
TMF	IMR2.5	**Transmit Multiframe.** 0=interrupt masked 1=interrupt enabled
SEC	IMR2.4	**1-Second Timer.** 0=interrupt masked 1=interrupt enabled
TAF	IMR2.3	**Transmit Align Frame.** 0=interrupt masked 1=interrupt enabled
LOTC	IMR2.2	**Loss Of Transmit Clock.** 0=interrupt masked 1=interrupt enabled
RCMF	IMR2.1	**Receive CRC4 Multifram**e. 0=interrupt masked 1=interrupt enabled
TSLIP	IMR2.0	**Transmit Side Elastic Store Slip.** 0=interrupt masked 1=interrupt enabled

5.0 ERROR COUNT REGISTERS

There are a set of four counters in the DS21Q43A that record bipolar or code violations, errors in the CRC4 SMF code words, E-bits as reported by the far end, and word errors in the FAS. Each of these four counters are automatically updated on either 1-second boundaries (CCR2.7=0) or every 62.5 ms (CCR2.7=1) as determined by the timer in Status Register 2 (SR2.4). Hence, these registers contain performance data from either the previous second or the previous 100 ms. The user can use the interrupt from the timer to determine when to read these registers. The user has a full second (or 62.5 ms) to read the counters before the data is lost.

5.1 BPV or Code Violation Counter

Violation Count Register 1 (VCR1) is the most significant word and VCR2 is the least significant word of a 16-bit counter that records either BiPolar Violations (BPVs) or Code Violations (CVs). If CCR2.6=0, then the VCR counts bipolar violations. Bipolar violations are defined as consecutive marks of the same polarity. In this mode, if the HDB3 mode is set for the receive side via CCR1.2, then HDB3 code words are not counted as BPVs. If CCR2.6=1, then the VCR counts code violations as defined in ITU O.161. Code violations are defined as consecutive bipolar violations of the same polarity. In most applications, the DS21Q43A should be programmed to count BPVs when receiving AMI code and to count CVs when receiving HDB3 code. This counter increments at all times and is not disabled by loss of sync conditions. The counter saturates at 65,535 and will not rollover. The bit error rate on an E1 line would have to be greater than 10**-2 before the VCR would saturate.

VCR1: UPPER BIPOLAR VIOLATION COUNT REGISTER 1 (Address=00 Hex)
VCR2: LOWER BIPOLAR VIOLATION COUNT REGISTER 2 (Address=01 Hex)

(MSB)							(LSB)	
V15	V14	V13	V12	V11	V10	V9	V8	VCR1
V7	V6	V5	V4	V3	V2	V1	V0	VCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
V15	VCR1.7	**MSB of the 16-bit bipolar or code violation count.**
V0	VCR2.0	**LSB of the 16-bit bipolar or code violation count.**

5.2 CRC4 Error Counter

CRC4 Count Register 1 (CRCCR1) is the most significant word and CRCCR2 is the least significant word of a 10-bit counter that records word errors in the Cyclic Redundancy Check 4 (CRC4). Since the maximum CRC4 count in a 1-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

CRCCR1: CRC4 COUNT REGISTER 1 (Address=02 Hex)
CRCCR2: CRC4 COUNT REGISTER 2 (Address=03 Hex)

(MSB)							(LSB)	
(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	CRC9	CRC8	CRCCR1
CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	CRCCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC9	CRCCR1.1	**MSB of the 10-bit CRC4 error count.**
CRC0	CRCCR2.0	**LSB of the 10-bit CRC4 error count.**

NOTE:

1. The upper 6 bits of CRCCR1 at address 02 are the most significant bits of the 12-bit FAS error counter.

5.3 E-Bit Counter

E-bit Count Register 1 (EBCR1) is the most significant word and EBCR2 is the least significant word of a 10-bit counter that records Far End Block Errors (FEBE) as reported in the 1st bit of frames 13 and 15 on E1 lines running with CRC4 multiframe. These count registers will increment once each time the received E-bit is set to 0. Since the maximum E-bit count in a 1-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

EBCR1: E-BIT COUNT REGISTER 1 (Address=04 Hex)
EBCR2: E-BIT COUNT REGISTER 2 (Address=05 Hex)

(MSB)							(LSB)	
(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	(note 1)	EB9	EB8	EBCR1
EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	EBCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
EB9	EBCR1.1	**MSB of the 10-bit E-Bit count.**
EB0	EBCR2.0	**LSB of the 10-bit E-Bit count.**

NOTE:
1. The upper 6 bits of EBCR1 at address 04 are the least significant bits of the 12-bit FAS error counter.

5.4 FAS Error Counter

FAS Count Register 1 (FASCR1) is the most significant word and FASCR2 is the least significant word of a 12-bit counter that records word errors in the Frame Alignment Signal in timeslot 0. This counter is disabled during loss of frame synchronization conditions; it is not disabled during loss of synchronization at either the CAS or CRC4 multiframe level. Since the maximum FAS word error count in a 1-second period is 4000, this counter cannot saturate.

FASCR1: FAS BIT COUNT REGISTER 1 (Address=02 Hex)
FASCR2: FAS BIT COUNT REGISTER 2 (Address=04 Hex)

(MSB)							(LSB)	
FAS11	FAS10	FAS9	FAS8	FAS7	FAS6	(note 2)	(note 2)	FASCR1
FAS5	FAS4	FAS3	FAS2	FAS1	FAS0	(note 1)	(note 1)	FASCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
FAS11	FASCR1.7	**MSB of the 12-bit FAS error count.**
FAS0	FASCR2.2	**LSB of the 12-bit FAS error count.**

NOTES:
1. The lower 2 bits of FASCR1 at address 02 are the most significant bits of the 10-bit CRC4 error counter.
2. The lower 2 bits of FASCR2 at address 04 are the most significant bits of the 10-bit E-Bit counter.

6.0 ADDITIONAL (Sa) AND INTERNATIONAL (Si) BIT OPERATION

The DS21Q43A provides for access to both the Sa and the Si bits via three different methods. The first is via a hardware scheme using the RLINK/RLCLK and TLINK/ TLCLK pins. The first method is discussed in Section 6.1. The second involves using the internal RAF/RNAF and TAF/TNAF registers and is discussed in Section 6.2 The third method which is covered in Section 6.3 involves an expanded version of the second method and is one of the features added to the DS21Q43A from the original DS2143 definition.

6.1 Hardware Scheme

On the receive side, all of the received data is reported at the RLINK pin. Via RCR2, the user can control the RLCLK pin to pulse during any combination of Sa bits. This allows the user to create a clock that can be used to capture the needed Sa bits. If RSYNC is programmed to output a frame boundary, it will identify the Si bits. See Section 11 for detailed timing.

On the transmit side, the individual Sa bits can be either sourced from the internal TNAF register (see Section 6.2 for details) or from the external TLINK pin. Via TCR2, the DS21Q43A can be programmed to source any combination of the additional bits from the TLINK pin. If the user wishes to pass the Sa bits through the DS21Q43A without them being altered, then the device should be set up to source all 5 Sa bits via the TLINK pin and the TLINK pin should be tied to the TSER pin. Si bits can be inserted through the TSER pin via the clearing of the TCR1.3 bit. Please see the timing diagrams and the transmit data flow diagram in Section 11 for examples.

6.2 Internal Register Scheme Based on Doubleframe

On the receive side, the RAF and RNAF registers will always report the data as it received in the Additional and International bit locations. The RAF and RNAF registers are updated with the setting of the Receive Align Frame bit in Status Register 2 (SR2.6). The host can use the SR2.6 bit to know when to read the RAF and RNAF registers. It has 250 µs to retrieve the data before it is lost.

On the transmit side, data is sampled from the TAF and TNAF registers with the setting of the Transmit Align Frame bit in Status Register 2 (SR2.3). The host can use the SR2.3 bit to know when to update the TAF and TNAF registers. It has 250 µs to update the data or else the old data will be retransmitted. Data in the Si bit position will be overwritten if either the DS21Q43A is programmed: (1) to source the Si bits from the TSER pin, (2) in the CRC4 mode, or (3) to have automatic E-bit insertion enabled. Data in the Sa bit position will be overwritten if any of the TCR2.3 to TCR2.7 bits are set to 1 (please see Section 6.1 for details). Please see the register descriptions for TCR1 and TCR2 and the Transmit Data Flow diagram in Section 11 for more details.

RAF: RECEIVE ALIGN FRAME REGISTER (Address=2F Hex)

(MSB)							(LSB)
Si	0	0	1	1	0	1	1

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	RAF.7	**International Bit.**
0	RAF.6	**Frame Alignment Signal Bit.**
0	RAF.5	**Frame Alignment Signal Bit.**
1	RAF.4	**Frame Alignment Signal Bit.**
1	RAF.3	**Frame Alignment Signal Bit.**
0	RAF.2	**Frame Alignment Signal Bit.**
1	RAF.1	**Frame Alignment Signal Bit.**
1	RAF.0	**Frame Alignment Signal Bit.**

RNAF: RECEIVE NON-ALIGN FRAME REGISTER (Address=1F Hex)

(MSB)							(LSB)
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	RNAF.7	**International Bit.**
1	RNAF.6	**Frame Non-Alignment Signal Bit.**
A	RNAF.5	**Remote Alarm.**
Sa4	RNAF.4	**Additional Bit 4.**
Sa5	RNAF.3	**Additional Bit 5.**
Sa6	RNAF.2	**Additional Bit 6.**
Sa7	RNAF.1	**Additional Bit 7.**
Sa8	RNAF.0	**Additional Bit 8.**

TAF: TRANSMIT ALIGN FRAME REGISTER (Address=20 Hex)

(MSB)							(LSB)
Si	0	0	1	1	0	1	1

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	TAF.7	**International Bit.**
0	TAF.6	**Frame Alignment Signal Bit.**
0	TAF.5	**Frame Alignment Signal Bit.**
1	TAF.4	**Frame Alignment Signal Bit.**
1	TAF.3	**Frame Alignment Signal Bit.**
0	TAF.2	**Frame Alignment Signal Bit.**
1	TAF.1	**Frame Alignment Signal Bit.**
1	TAF.0	**Frame Alignment Signal Bit.**

TNAF: TRANSMIT NON-ALIGN FRAME REGISTER (Address=21 Hex)

(MSB)							(LSB)
Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	POSITION	NAME AND DESCRIPTION
Si	TNAF.7	**International Bit.**
1	TNAF.6	**Frame Non-Alignment Signal Bit.**
A	TNAF.5	**Remote Alarm (used to transmit the alarm).**
Sa4	TNAF.4	**Additional Bit 4.**
Sa5	TNAF.3	**Additional Bit 5.**
Sa6	TNAF.2	**Additional Bit 6.**
Sa7	TNAF.1	**Additional Bit 7.**
Sa8	TNAF.0	**Additional Bit 8.**

6.3 Internal Register Scheme Based on CRC4 Multiframe

On the receive side, there is a set of eight registers (RSiAF, RSiNAF, RRA, RSa4 to RSa8) that report the SI and Sa bits as they are received. These registers are updated with the setting of the Receive CRC4 Multiframe bit in Status Register 2 (SR2.1). The host can use the SR2.1 bit to know when to read these registers. The user has 2 ms to retrieve the data before it is lost. The MSB of each register is the first received. Please see the register descriptions below and the Transmit Data Flow diagram in Section 11 for more details.

On the transmit side, there is also a set of eight registers (TSiAF, TSiNAF, TRA, TSa4 to TSa8) that via the Transmit Sa Bit Control Register (TSaCR), can be programmed to insert both Si and Sa data. Data is sampled from these registers with the setting of the Transmit multiframe bit in Status Register 2 (SR2.5). The host can use the SR2.5 bit to know when to update these registers. It has 2 ms to update the data or else the old data will be retransmitted. The MSB of each register is the first bit transmitted. Please see the register descriptions below and the Transmit Data Flow diagram in Section 11 for more details.

REGISTER NAME	ADDRESS (HEX)	FUNCTION
RSiAF	58	The eight Si bits in the align frame.
RSiNAF	59	The eight Si bits in the non-align frame.
RRA	5A	The eight reportings of the receive remote alarm (RA).
RSa4	5B	The eight Sa4 reported in each CRC4 multiframe.
RSa5	5C	The eight Sa5 reported in each CRC4 multiframe.
RSa6	5D	The eight Sa6 reported in each CRC4 multiframe.
RSa7	5E	The eight Sa7 reported in each CRC4 multiframe.
RSa8	5F	The eight Sa8 reported in each CRC4 multiframe.
TSiAF	50	The eight Si bits to be inserted into the align frame.
TSiNAF	51	The eight Si bits to be inserted into the non-align frame.
TTA	52	The eight settings of receive remote alarm (RA).
TSa4	53	The eight Sa4 settings in each CRC4 multiframe.
TSa5	54	The eight Sa5 settings in each CRC4 multiframe.
TSa6	55	The eight Sa6 settings in each CRC4 multiframe.
TSa7	56	The eight Sa7 settings in each CRC4 multiframe.
TSa8	57	The eight Sa8 settings in each CRC4 multiframe.

TSACR: TRANSMIT SA BIT CONTROL REGISTER (Address=1C Hex)

(MSB) **(LSB)**

SiAF	SiNAF	RA	Sa4	Sa5	Sa6	Sa7	Sa8

SYMBOL	POSITION	NAME AND DESCRIPTION
SiAF	TSaCR.7	**International Bit in Align Frame Insertion Control Bit.** 0=do not insert data from the TSiAF register into the transmit data stream 1=insert data from the TSiAF register into the transmit data stream
SiNAF	TSaCR.6	**International Bit in Non-Align Frame Insertion Control Bit.** 0=do not insert data from the TSiNAF register into the transmit data stream 1=insert data from the TSiNAF register into the transmit data stream
RA	TSaCR.5	**Remote Alarm Insertion Control Bit.** 0=do not insert data from the TRA register into the transmit data stream 1=insert data from the TRA register into the transmit data stream
Sa4	TSaCR.4	**Additional Bit 4 Insertion Control Bit.** 0=do not insert data from the TSa4 register into the transmit data stream 1=insert data from the TSa4 register into the transmit data stream
Sa5	TSaCR.3	**Additional Bit 5 Insertion Control Bit.** 0=do not insert data from the TSa5 register into the transmit data stream 1=insert data from the TSa5 register into the transmit data stream
Sa6	TSaCR.2	**Additional Bit 6 Insertion Control Bit.** 0=do not insert data from the TSa6 register into the transmit data stream 1=insert data from the TSa6 register into the transmit data stream
Sa7	TSaCR.1	**Additional Bit 7 Insertion Control Bit.** 0=do not insert data from the TSa7 register into the transmit data stream 1=insert data from the TSa7 register into the transmit data stream
Sa8	TSaCR.0	**Additional Bit 8 Insertion Control Bit.** 0=do not insert data from the TSa8 register into the transmit data stream 1=insert data from the TSa8 register into the transmit data stream

7.0 SIGNALING OPERATION

The Channel Associated Signaling (CAS) bits embedded in the E1 stream can be extracted from the receive stream and inserted into the transmit stream by the DS21Q43A. Each of the 30 channels has four signaling bits (A/B/C/D) associated with it. The numbers in parenthesis () are the channel associated with a particular signaling bit. The channel numbers have been assigned as described in the ITU/CCITT documents. For example, channel 1 is associated with timeslot 1 and channel 30 is associated with timeslot 31. There is a set of 16 registers for the receive side (RS1 to RS16) and 16 registers on the transmit side (TS1 to TS16). The signaling registers are detailed below.

RS1 TO RS16: RECEIVE SIGNALING REGISTERS (Address=30 to 3F Hex)

(MSB)							**(LSB)**	
0	**0**	**0**	**0**	**X**	**Y**	**X**	**X**	RS1 (30)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	RS2 (31)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	RS3 (32)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	RS4 (33)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	RS5 (34)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	RS6 (35)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	RS7 (36)
A(7)	B(7)	C(7)	D(7)	A(22)	B(22)	C(22)	D(22)	RS8 (34)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	RS9 (35)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	RS10 (36)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	RS11 (3A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	RS12 (3B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	RS13 (3C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	RS14 (3D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	RS15 (3E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	RS16 (3F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	RS1.0/1/3	**Spare Bits.**
Y	RS1.2	**Remote Alarm Bit (integrated and reported in SR1.6).**
A(1)	RS2.7	**Signaling Bit A for Channel 1.**
D(30)	RS16.0	**Signaling Bit D for Channel 30.**

Each Receive Signaling Register (RS1 to RS16) reports the incoming signaling bits from two timeslots. The bits in the Receive Signaling Registers are updated on multiframe boundaries so the user can utilize the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The user has a full 2 ms to retrieve the signaling bits before the data is lost. The RS registers are updated under all conditions. Their validity should be qualified by checking for synchronization at the CAS level. In CCS signaling mode, RS1 to RS16 can also be used to extract

signaling information. Via the SR2.7 bit, the user will be informed when the signaling registers have been loaded with data. The user has 2 ms to retrieve the data before it is lost.

TS1 TO TS16: TRANSMIT SIGNALING REGISTERS (Address=40 to 4F Hex)

(MSB)							**(LSB)**	
0	**0**	**0**	**0**	**X**	**Y**	**X**	**X**	TS1 (40)
A(1)	B(1)	C(1)	D(1)	A(16)	B(16)	C(16)	D(16)	TS2 (41)
A(2)	B(2)	C(2)	D(2)	A(17)	B(17)	C(17)	D(17)	TS3 (42)
A(3)	B(3)	C(3)	D(3)	A(18)	B(18)	C(18)	D(18)	TS4 (43)
A(4)	B(4)	C(4)	D(4)	A(19)	B(19)	C(19)	D(19)	TS5 (44)
A(5)	B(5)	C(5)	D(5)	A(20)	B(20)	C(20)	D(20)	TS6 (45)
A(6)	B(6)	C(6)	D(6)	A(21)	B(21)	C(21)	D(21)	TS7 (46)
A(7)	B(7)	C(7)	D(7)	A(22)	B(22)	C(22)	D(22)	TS8 (47)
A(8)	B(8)	C(8)	D(8)	A(23)	B(23)	C(23)	D(23)	TS9 (48)
A(9)	B(9)	C(9)	D(9)	A(24)	B(24)	C(24)	D(24)	TS10 (49)
A(10)	B(10)	C(10)	D(10)	A(25)	B(25)	C(25)	D(25)	TS11 (4A)
A(11)	B(11)	C(11)	D(11)	A(26)	B(26)	C(26)	D(26)	TS12 (4B)
A(12)	B(12)	C(12)	D(12)	A(27)	B(27)	C(27)	D(27)	TS13 (4C)
A(13)	B(13)	C(13)	D(13)	A(28)	B(28)	C(28)	D(28)	TS14 (4D)
A(14)	B(14)	C(14)	D(14)	A(29)	B(29)	C(29)	D(29)	TS15 (4E)
A(15)	B(15)	C(15)	D(15)	A(30)	B(30)	C(30)	D(30)	TS16 (4F)

SYMBOL	POSITION	NAME AND DESCRIPTION
X	TS1.0/1/3	**Spare Bits.**
Y	TS1.2	**Remote Alarm Bit.**
A(1)	TS2.7	**Signaling Bit A for Channel 1.**
D(30)	TS16.0	**Signaling Bit D for Channel 30.**

Each Transmit Signaling Register (TS1 to TS16) contains the CAS bits for two timeslots that will be inserted into the outgoing stream if enabled to do so via TCR1.5. On multiframe boundaries, the DS21Q43A will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe bit in Status Register 2 (SR2.5) to know when to update the signaling bits. The bit will be set every 2 ms and the user has 2 ms to update the TSRs before the old data will be retransmitted.

The TS1 register is special because it contains the CAS multiframe alignment word in its upper nibble. The upper nibble must always be set to 0000 or else the terminal at the far end will lose multiframe synchronization. If the user wishes to transmit a multiframe alarm to the far end, then the TS1.2 bit should be set to a 1. If no alarm is to be transmitted, then the TS1.2 bit should be cleared. The three remaining bits in TS1 are the spare bits. If they are not used, they should be set to 1. In CCS signaling mode, TS1 to TS16 can also be used to insert signaling information. Via the SR2.5 bit, the user will be

informed when the signaling registers need to be loaded with data. The user has 2 ms to load the data before the old data will be retransmitted. Via the CCR3.6 bit, the user has the option to use the Transmit Channel Blocking Registers (TCBRs) to determine on a channel by channel basis, which signaling bits are to be inserted via the TSRs (the corresponding bit in the TCBRs=1) and which are to be sourced from the TSER pin (the corresponding bit in the TCBRs=0). See the Transmit Data Flow diagram in Section 11 for more details.

8.0 TRANSMIT IDLE REGISTERS

There is a set of five registers in the DS21Q43A that can be used to custom tailor the data that is to be transmitted onto the E1 line, on a channel by channel basis. Each of the 32 E1 channels can be forced to have a user defined idle code inserted into them.

TIR1/TIR2/TIR3/TIR4: TRANSMIT IDLE REGISTERS (Address=26 to 29 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (26)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (27)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (28)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TIR4 (29)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	TIR4.7	**Transmit Idle Registers**. 0=do not insert the Idle Code into this channel
CH1	TIR1.0	1=insert the Idle Code into this channel

NOTE:

If CCR3.5=1, then a 0 in the TIRs implies that channel data is to be sourced from TSER and a 1 implies that channel data is to be sourced from the RSER pin.

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address=2A Hex)

(MSB)							(LSB)
TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0

SYMBOL	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	**MSB of the Idle Code.**
TIDR0	TIDR.0	**LSB of the Idle Code.**

Each of the bit positions in the Transmit Idle Registers (TIR1/TIR2/TIR3/TIR4) represent a timeslot in the outgoing frame. When these bits are set to a 1, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR). In the TIDR, the MSB is transmitted first. Via the CCR3.5 bit, the user has the option to use the TIRs to determine on a channel by channel basis, if data from the RSER pin should be substituted for data from the TSER pin. In this mode, if the corresponding bit in the TIRs is set to 1, then data will be sourced from the RSER pin. If the corresponding bit in the TIRs is set to 0, then data for that channel will sourced from the TSER pin. See the Transmit Data Flow diagram in Section 11 for more details.

9.0 CLOCK BLOCKING REGISTERS

The Receive Channel Blocking Register (RCBR1/ RCBR2/RCBR3/RCBR4) and the Transmit Channel Blocking Registers (TCBR1/TCBR2/TCBR3/TCBR4) control the RCHBLK and TCHBLK pins respectively. The RCHBLK and TCHCLK pins are user programmable outputs that can be forced either high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in ISDN-PRI applications. When the appropriate bits are set to a 1, the RCHBLK and TCHCLK pins will be held high during the entire corresponding channel time. See the timing in Section 11 for an example. The TCBRs have alternate mode of use. Via the CCR3.6 bit, the user has the option to use the TCBRs to determine on a channel-by-channel basis which signaling bits are to be inserted via the TSRs (the corresponding bit in the TCBRs=1) and which are to be sourced from the TSER pin (the corresponding bit in the TCBR=0). See the Transmit Data Flow diagram in Section 11 for more details.

RCBR1/RCBR2/RCBR3/RCBR4: RECEIVE CHANNEL BLOCKING REGISTERS (Address=2B to 2E Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (2B)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (2C)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (2D)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	RCBR4 (2E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	RCBR4.7	**Receive Channel Blocking Registers**. 0=force the RCHBLK pin to remain low during this channel time
CH1	RCBR1.0	1=force the RCHBLK pin high during this channel time

TCBR1/TCBR2/TCBR3/TCBR4: TRANSMIT CHANNEL BLOCKING REGISTERS (Address=22 to 25 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (22)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR2 (23)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR3 (24)
CH32	CH31	CH30	CH29	CH28	CH27	CH26	CH25	TCBR4 (25)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH32	TCBR4.7	**Receive Channel Blocking Registers**. 0=force the TCHBLK pin to remain low during this channel time
CH1	TCBR1.0	1=force the TCHBLK pin high during this channel time

NOTE:

If CCR3.6=1, then a 0 in the TCBRs implies that signaling data is to be sourced from TSER and a 1 implies that signaling data for that channel is to be sourced from the Transmit Signaling (TS) registers. See definition below.

TCBR1/TCBR2/TCBR3/TCBR4: DEFINITION WHEN CCR3.6=1

(MSB)							(LSB)	
CH20	CH4	CH19	CH3	CH18	CH2	CH17*	CH1*	TCBR1
CH24	CH8	CH23	CH7	CH22	CH6	CH21	CH5	TCBR2
CH28	CH12	CH27	CH11	CH26	CH10	CH25	CH9	TCBR3
CH32	CH16	CH31	CH15	CH30	CH14	CH29	CH13	TCBR4

*=CH1 and CH17 should be set to 1 to allow the internal TS1 register to create the CAS Multiframe Alignment Word and Spare/Remote Alarm bits.

10.0 ELASTIC STORES OPERATION

Each framer within the DS21Q43A contains dual two-frame (512 bits) elastic stores, one for the receive direction, and one for the transmit direction. These elastic stores have two main purposes. First, they can be used to rate convert the E1 data stream to 1.544 Mbps (or a multiple of 1.544 Mbps) which is the T1 rate. Secondly, they can be used to absorb the differences in frequency and phase between the E1 data stream and an asynchronous (i.e., not frequency locked) backplane clock (which can be 1.544 MHz or 2.048 MHz or a multiple thereof up to 8.192 MHz). Both elastic stores contain full controlled slip capability which is necessary for this second purpose. The elastic stores can be forced to a known depth via the Elastic Store Reset bit (CCR3.4). Toggling the CCR3.4 bit forces the read and write pointers into opposite frames. Both elastic stores within the DS21Q43A are fully independent and no restrictions apply to the sourcing of the various clocks that are applied to them. The transmit side elastic store can be enabled whether the receive elastic store is enabled or disabled and vice versa. Also, each elastic store can interface to either a 1.544 MHz or 2.048 MHz backplane without regard to the backplane rate the other elastic store is interfacing to.

10.1 Receive Side

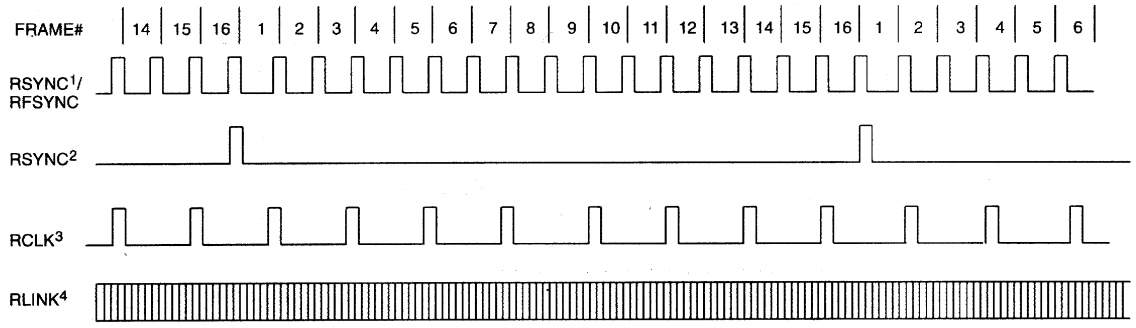
If the receive side elastic store is enabled (RCR2.1=1), then the user must provide either a 1.544 MHz (RCR2.2=0) or 2.048 MHz (RCR2.2=1) clock at the RSYSCLK pin. The user has the option of either providing a frame sync at the RSYNC pin (RCR1.5=1) or having the RSYNC pin provide a pulse on frame boundaries (RCR1.5=0). If the user wishes to obtain pulses at the frame boundary, then RCR1.6 must be set to 0 and if the user wishes to have pulses occur at the multiframe boundary, then RCR1.6 must be set to 1. The DS21Q43A will always indicate frame boundaries via the RFSYNC output whether the elastic store is enabled or not. If the elastic store is enabled, then either CAS (RCR1.7=0) or CRC4 (RCR1.7=1) multiframe boundaries will be indicated via the RMSYNC output. If the user selects to apply a 1.544 MHz clock to the RSYSCLK pin, then every fourth channel of the received E1 data will be deleted and an F-bit position (which will be forced to 1) will be inserted. Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be deleted from the received E1 data stream. Also, in 1.544 MHz applications, the RCHBLK output will not be active in channels 25 through 32 (or in other words, RCBR4 is not active). See Section 11 for more details. If the 512-bit elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data (256 bits) will be repeated at RSER and the SR1.4 and RIR.3 bits will be set to a 1. If the buffer fills, then a full frame of data will be deleted and the SR1.4 and RIR.4 bits will be set to a 1.

10.2 Transmit Side

The operation of the transmit elastic store is very similar to the receive side. The transmit side elastic store is enabled via CCR3.7. A 1.544 MHz (CCR3.1=0) or 2.048 MHz (CCR3.1=1) clock can be applied to the TSYSCLK input. If the user selects to apply a 1.544 MHz clock to the TSYSCLK pin, then the data sampled at TSER will be ignored every fourth channel. Hence channels 1, 5, 9, 13, 17, 21, 25, and 29 (timeslots 0, 4, 8, 12, 16, 20, 24, and 28) will be ignored. The user must supply a 8 kHz frame sync pulse to the TFSYNC input. See Section 11 for more details. Controlled slips in the transmit elastic store are reported in the SR2.0 bit and the direction of the slip is reported in the RIR.6 and RIR.7 bits.

11.0 TIMING DIAGRAMS/SYNCHRONIZATION FLOWCHART/TRANSMIT DATA FLOW DIAGRAM

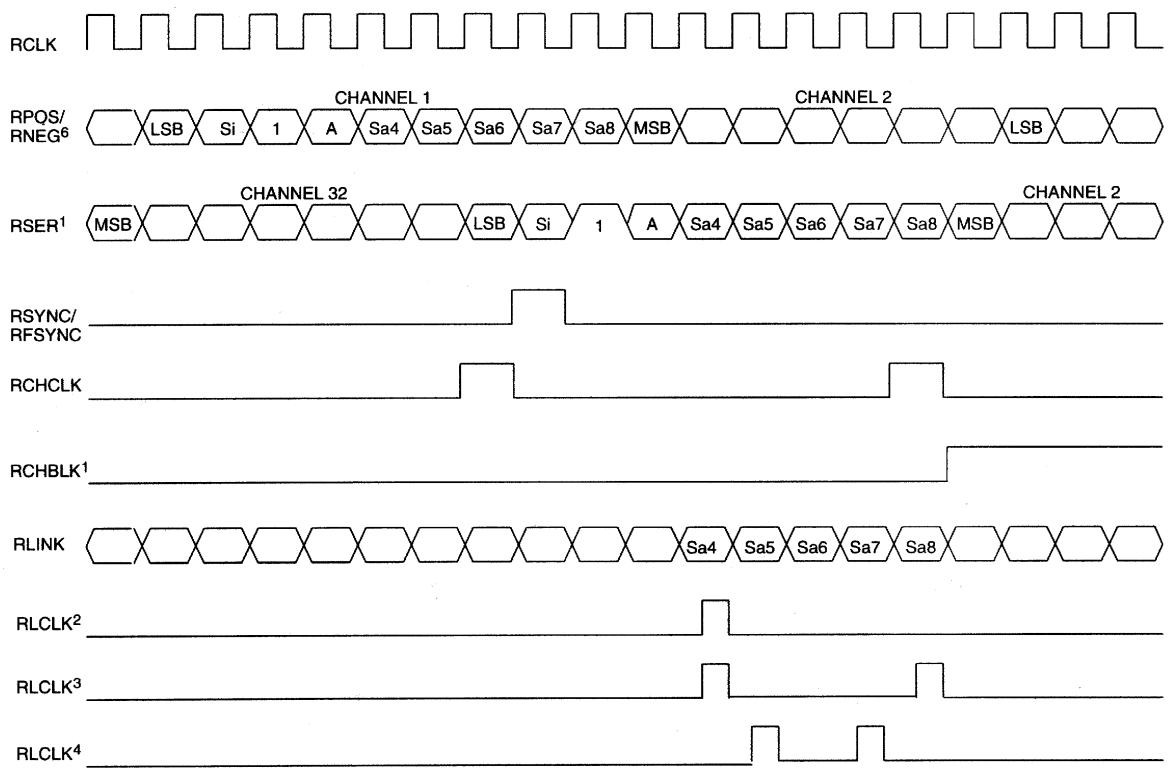
RECEIVE SIDE TIMING Figure 11-1



NOTES:

1. RSYNC in the frame mode (RCR1.6=0).
2. RSYNC in the multiframe mode (RCR1.6=1).
3. RLCLK is programmed to output just the Sa4 bit.
4. RLINK will always output all five Sa bits as well as the rest of the receive data stream.
5. This diagram assumes the CAS MF begins with the FAS word.

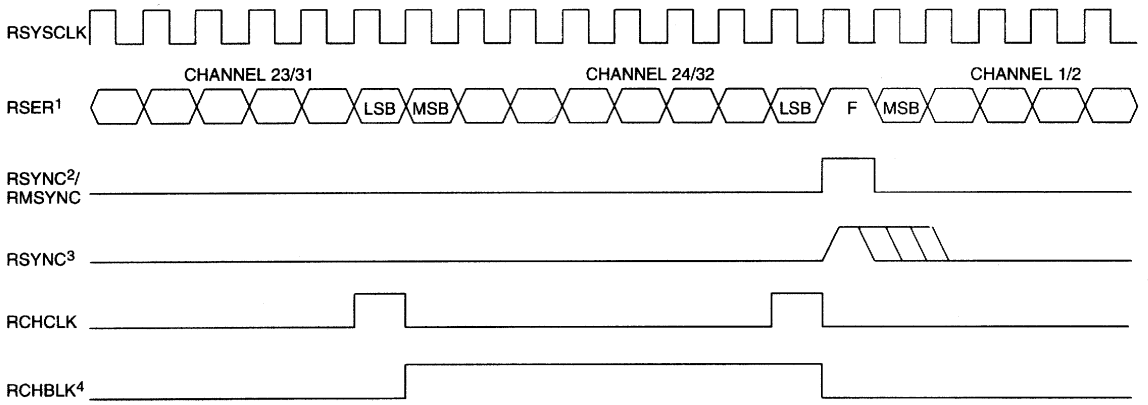
RECEIVE SIDE BOUNDARY TIMING (WITH ELASTIC STORE DISABLED) Figure 11-2



NOTES:

1. RCHBLK is programmed to block channel 2.
2. RLCLK is programmed to pulse during the Sa4 bits.
3. RLCLK is programmed to pulse during the SA4 and SA8 bits.
4. RLCLK is programmed to pulse during the Sa5 and Sa7 bits.
5. Shown is a non-align frame boundary.
6. There is a 6-RCLK delay from RPOS/RNEG to RSER.

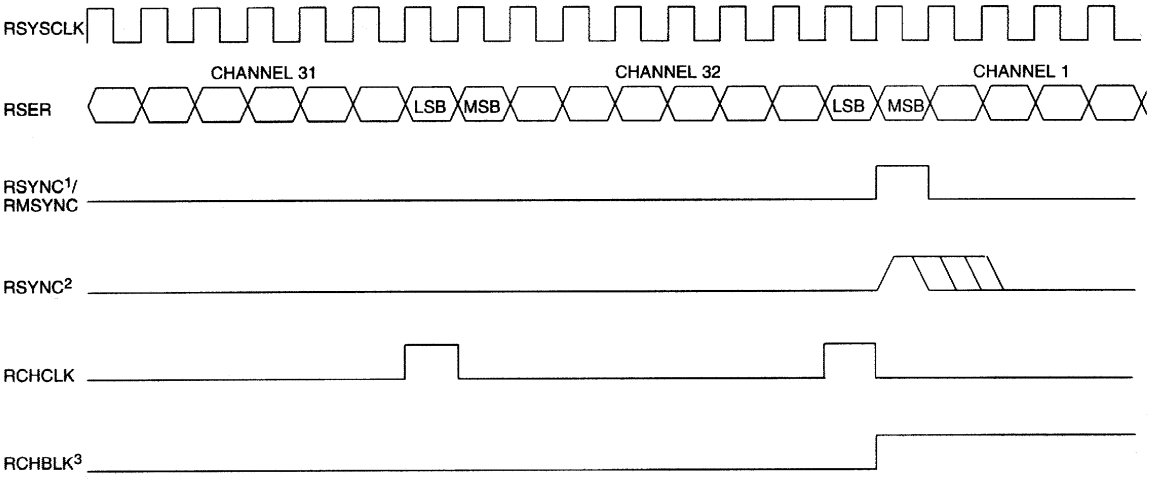
RECEIVE SIDE 1.544 MHz BOUNDARY TIMING (WITH ELASTIC STORE ENABLED) Figure 11-3



NOTES:

1. Data from the E1 channels 1, 5, 9, 13, 17, 21, 25, and 29 is dropped (channel 2 from the E1 link is mapped to channel 1 of the T1 link, etc.) and the F-bit position is added (forced to one).
2. RSYNC is in the output mode (RCR1.5=0).
3. RSYNC is in the input mode (RCR1.5=1).
4. RCHBLK is programmed to block channel 24.

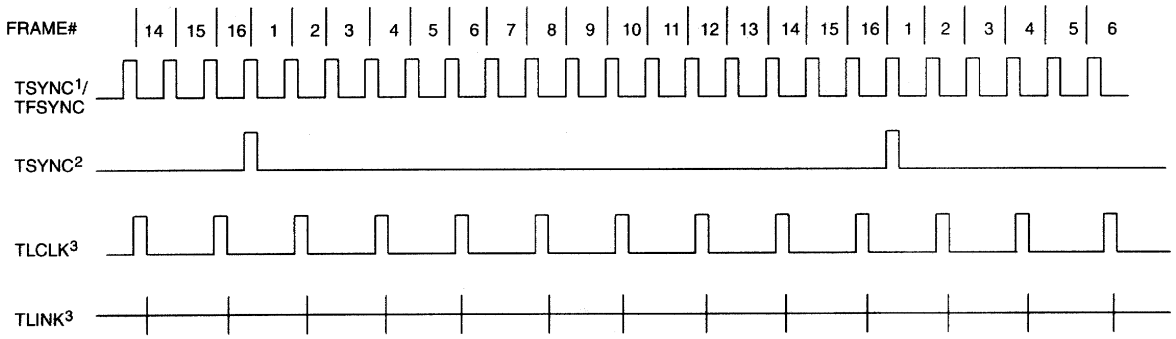
RECEIVE SIDE 2.048 MHz BOUNDARY TIMING (WITH ELASTIC STORE ENABLED) Figure 11-4



NOTES:

1. RSYNC is in the output mode (RCR1.5=0).
2. RSYNC is in the input mode (RCR1.5=1).
3. RCHBLK is programmed to block channel 1.

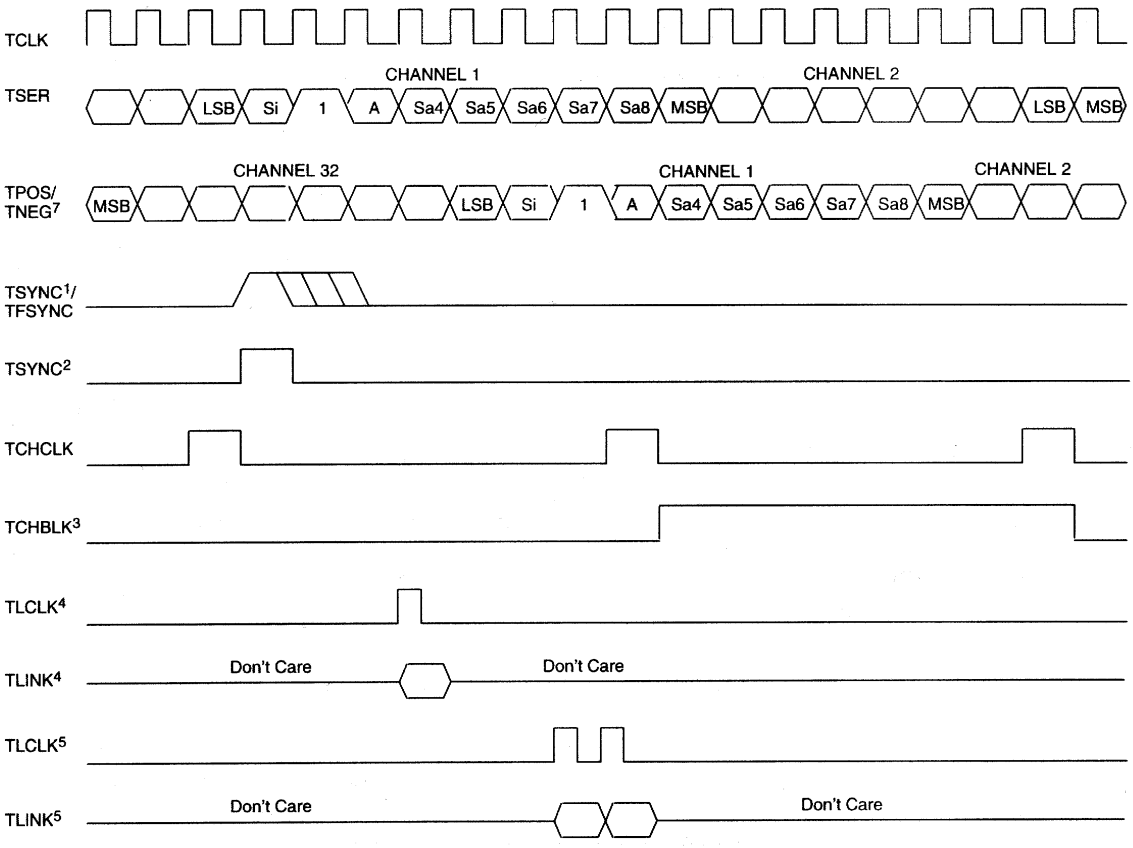
TRANSMIT SIDE TIMING Figure 11-5



NOTES:

1. TSYNC in the frame mode (TCR1.1=0).
2. TSYNC in the multiframe mode (TCR1.1=1).
3. TLINK is programmed to source only the Sa4 bit.
4. This diagram assumes both the CAS MF and the CRC4 begin with the align frame.

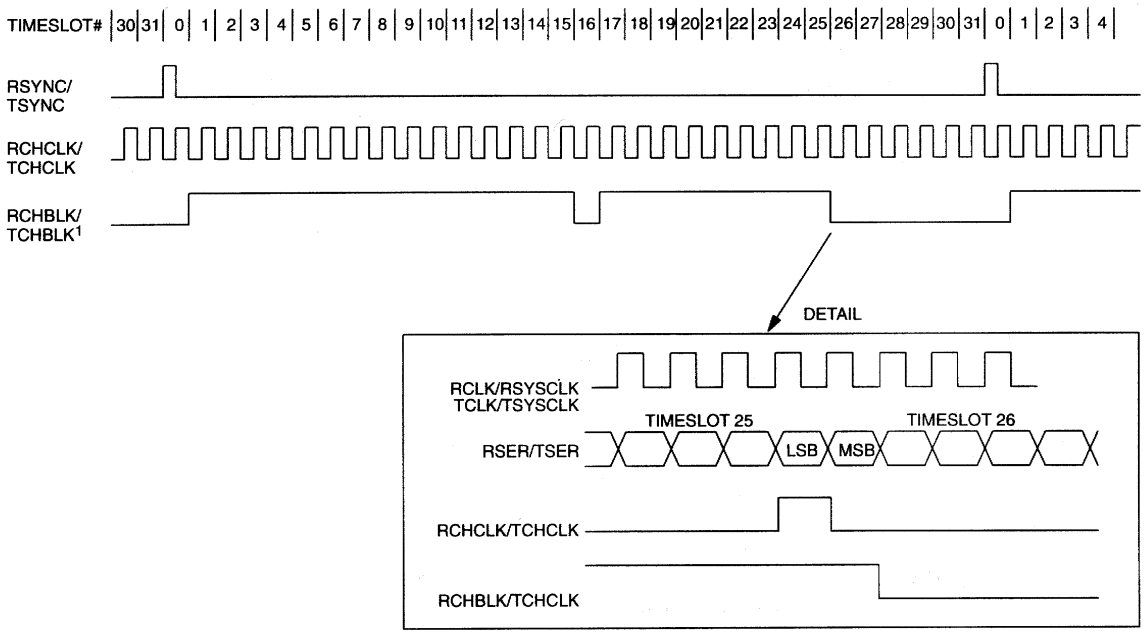
TRANSMIT SIDE BOUNDARY TIMING Figure 11-6



NOTES:

1. TSYNC is in the input mode (TCR1.0=0).
2. TSYNC is in the output mode (TCR1.0=1).
3. TCHBLK is programmed to block channel 2.
4. TLINK is programmed to source the Sa4 bits.
5. TLINK is programmed to source the Sa7 and Sa8 bits.
6. Shown is a non-align frame boundary.
7. There is a 5-TCLK delay from TSER to TPOS/TNEG.

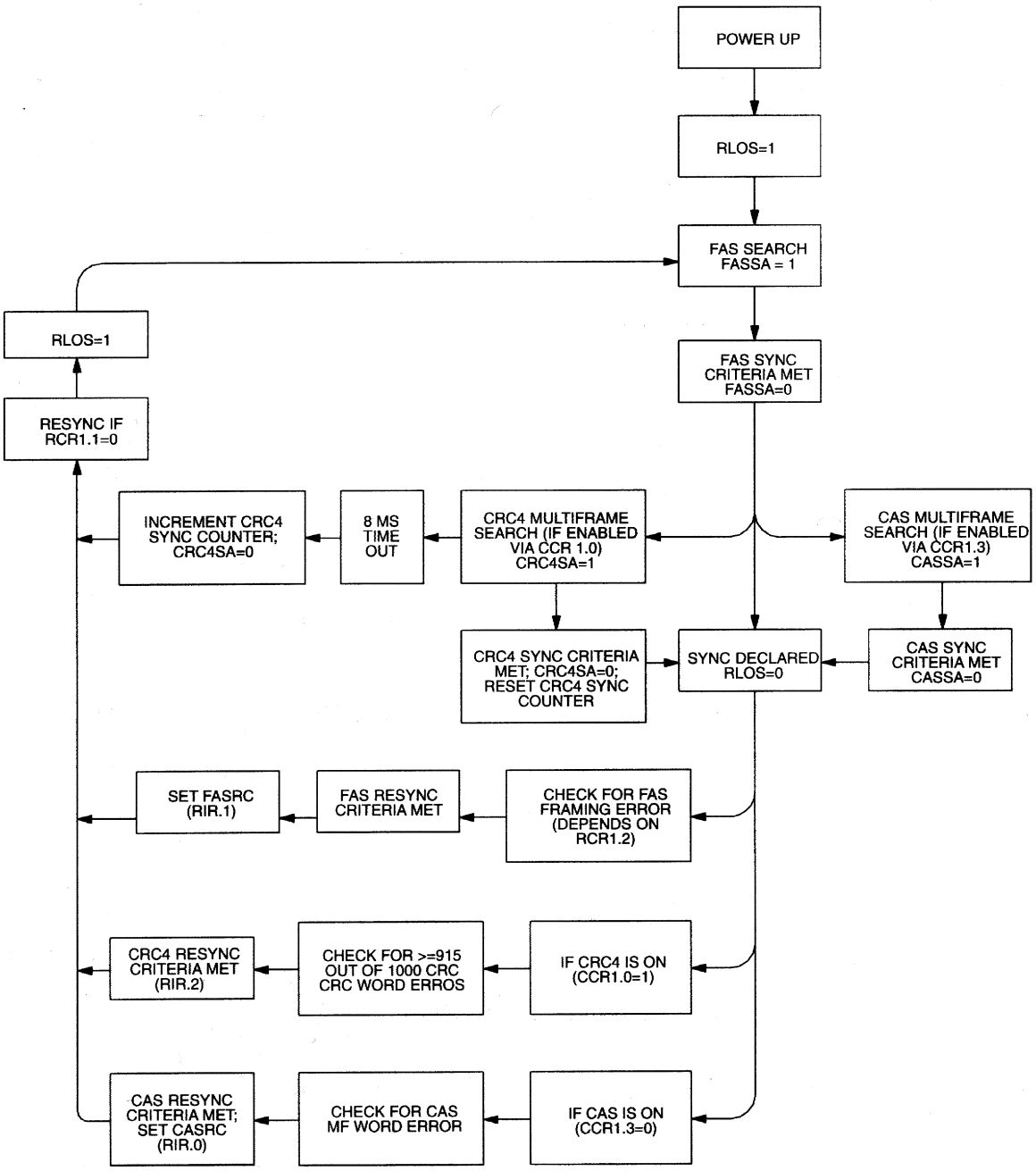
G.802 TIMING Figure 11-7



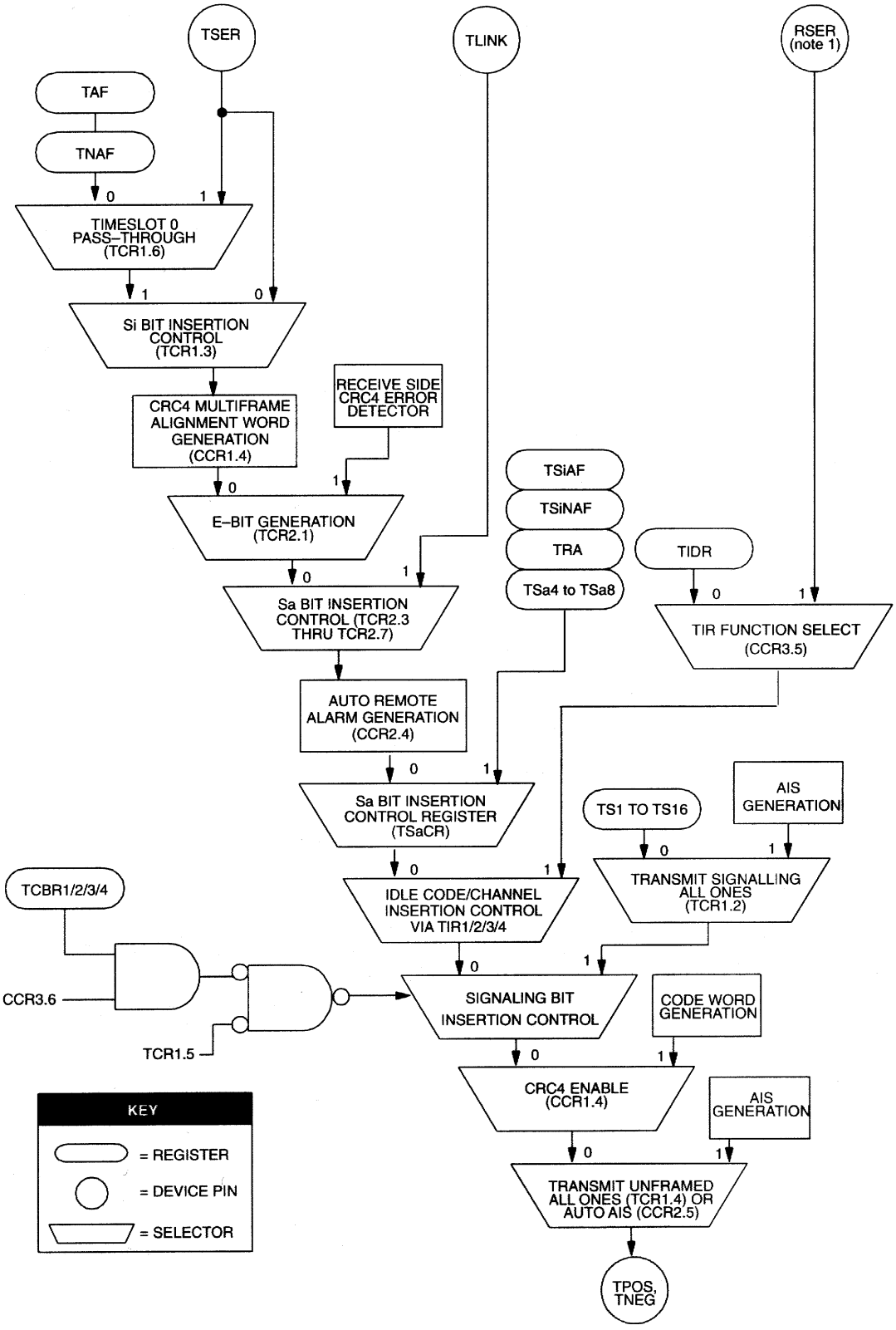
NOTE:

1. RCHBLK or TCHBLK is programmed to pulse high during timeslots 1 to 15, 17 to 25, and during bit 1 of timeslot 26.

DS21Q43A SYNCHRONIZATION FLOWCHART Figure 11-8



DS21Q43A TRANSMIT DATA FLOW Figure 11-9



NOTE:

1. TCLK must be tied to RCLK (or RSYSCLK if the elastic store is enabled) and TSYNC must be tied to RSYNC for data to be properly sourced from RSER.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C for DS21Q43AT
Operating Temperature	-40°C to +85°C for DS21Q43ATN
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATION CONDITIONS

(0°C to 70°C for DS21Q43AT; -40°C to +85°C for DS21Q43ATN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{DD}+0.3	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.50		5.50	V	1

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

DC CHARACTERISTICS

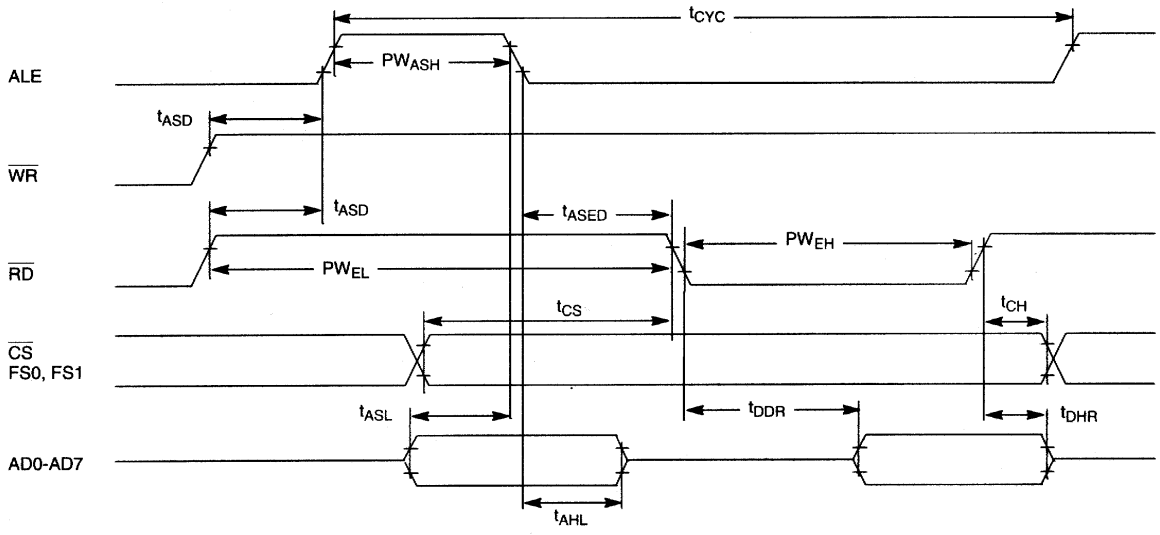
(0°C to 70°C; V_{DD}=5V ± 10% for DS21Q43AT; -40°C to +85°C; V_{DD}=5V ± 10% for DS21Q43ATN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current @ 5V	I_{DD}		32		mA	1
Input Leakage	I_{IL}	-1.0		+1.0	µA	2
Output Leakage	I_{LO}			1.0	µA	3
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

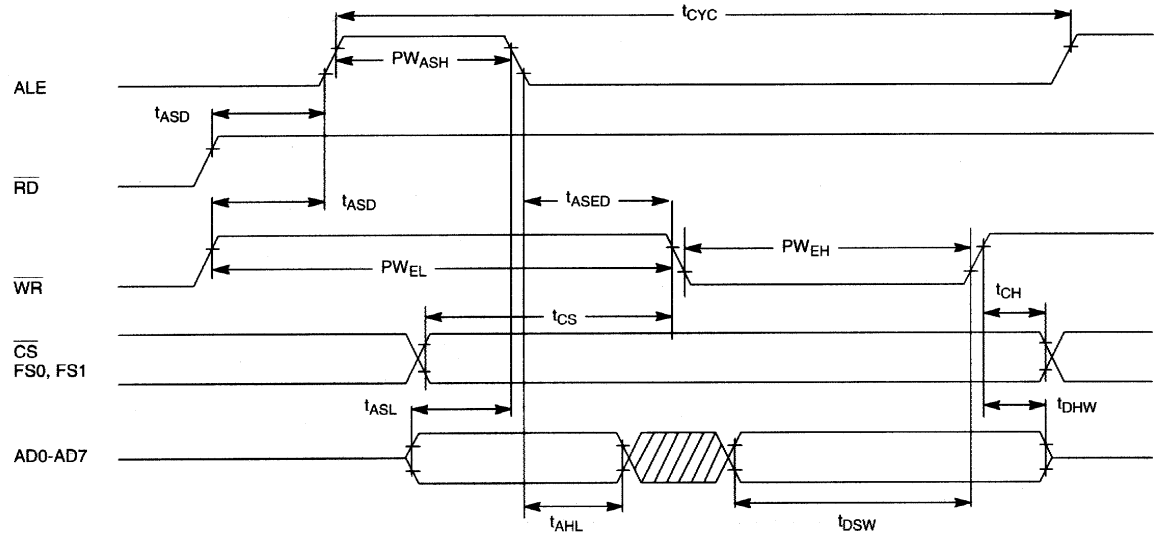
NOTES:

1. TCLK = RCLK = TSYSCLK = RSYSCLK = 2.048 MHz ; outputs open circuited.
2. $0.0V < V_{IN} < V_{DD}$.
3. Applied to $\overline{INT}$ when 3-stated.

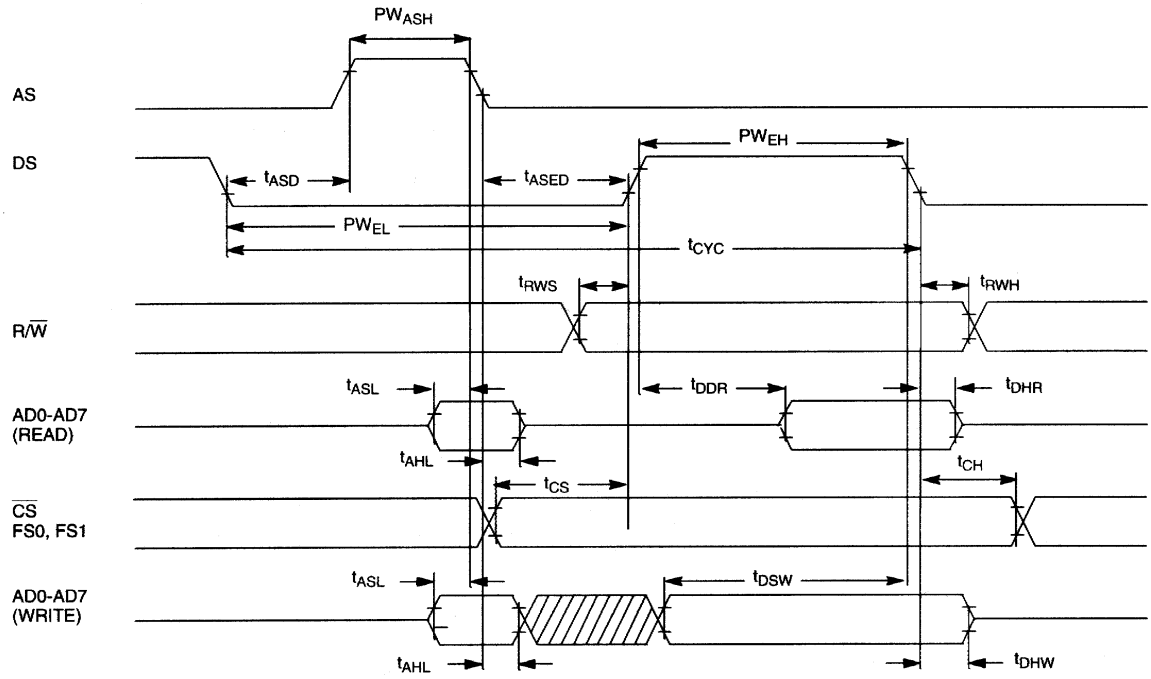
INTEL BUS READ AC TIMING (BTS=0/MUX=1) Figure 12-1



INTEL BUS WRITE AC TIMING (BTS=0/MUX=1) Figure 12-2



MOTOROLA BUS AC TIMING (BTS=1/MUX=1) Figure 12-3



AC CHARACTERISTICS - RECEIVE SIDE

(0°C to 70°C; V_{DD}=5V ± 10% for DS21Q43AT; -40°C to +85°C; V_{DD}=5V ± 10% for DS21Q43ATN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Period	t_{CP}		488		ns	
RCLK Pulse Width	t_{CH}	75			ns	
	t_{CL}	75			ns	
RSYSCLK Period	t_{SP}		648		ns	1
	t_{SP}		488		ns	2
RSYSCLK Pulse Width	t_{SH}	50			ns	
	t_{SL}	50			ns	
RSYNC Set Up to RSYSCLK Falling or RPOS/RNEG Set Up to RCLK Falling	t_{SU}	20			ns	
RSYNC Pulse Width	t_{PW}	50			ns	3
RPOS/RNEG Hold from RCLK Falling	t_{HD}	20			ns	
RCLK and RSYSCLK Rise and Fall Times	t_R, t_F			25	ns	
Delay RCLK or RSYSCLK to RSER Valid	t_{DD}			50	ns	
Delay RCLK or RSYSCLK to RCHCLK	t_{D1}			75	ns	
Delay RCLK or RSYSCLK to RCHBLK	t_{D2}			75	ns	
Delay RCLK to RFSYNC or RSYNC or	t_{D3}			75	ns	

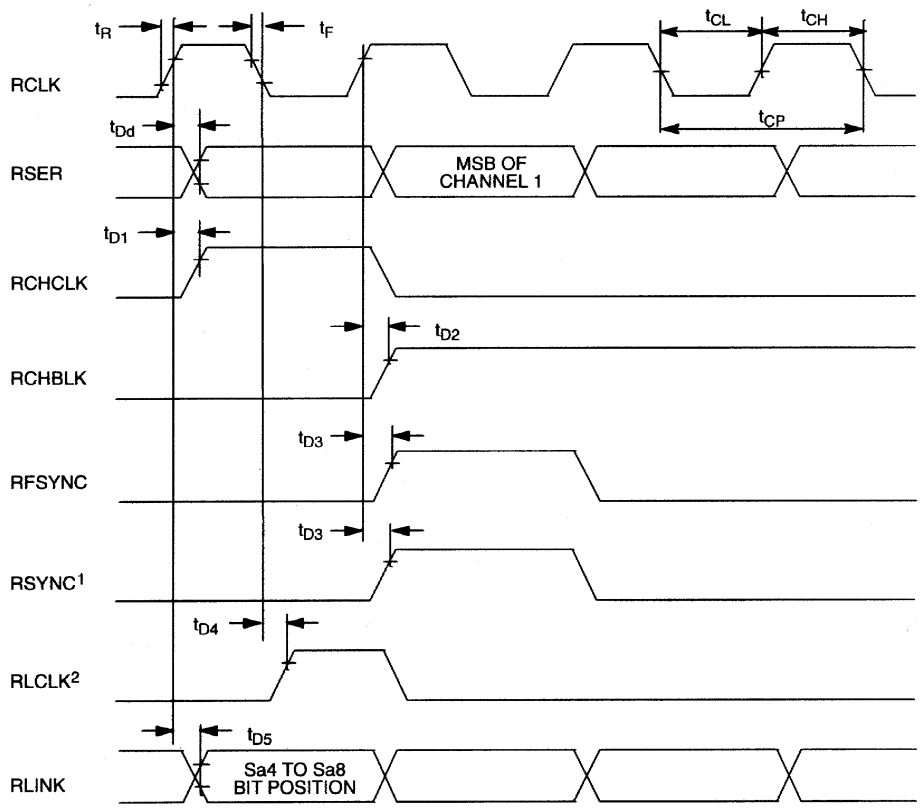
Delay RSYSCLK to RMSYNC or RSYNC						
Delay RCLK to RLCLK	t_{D4}			75	ns	
Delay RCLK to RLINK Valid	t_{D5}			75	ns	

See Figures 12-4 to 12-6 for details.

NOTES:

1. RSYSCLK=1.544 MHz.
2. RSYSCLK=2.048 MHz.
3. RSYNC in input mode.

RECEIVE SIDE AC TIMING Figure 12-4

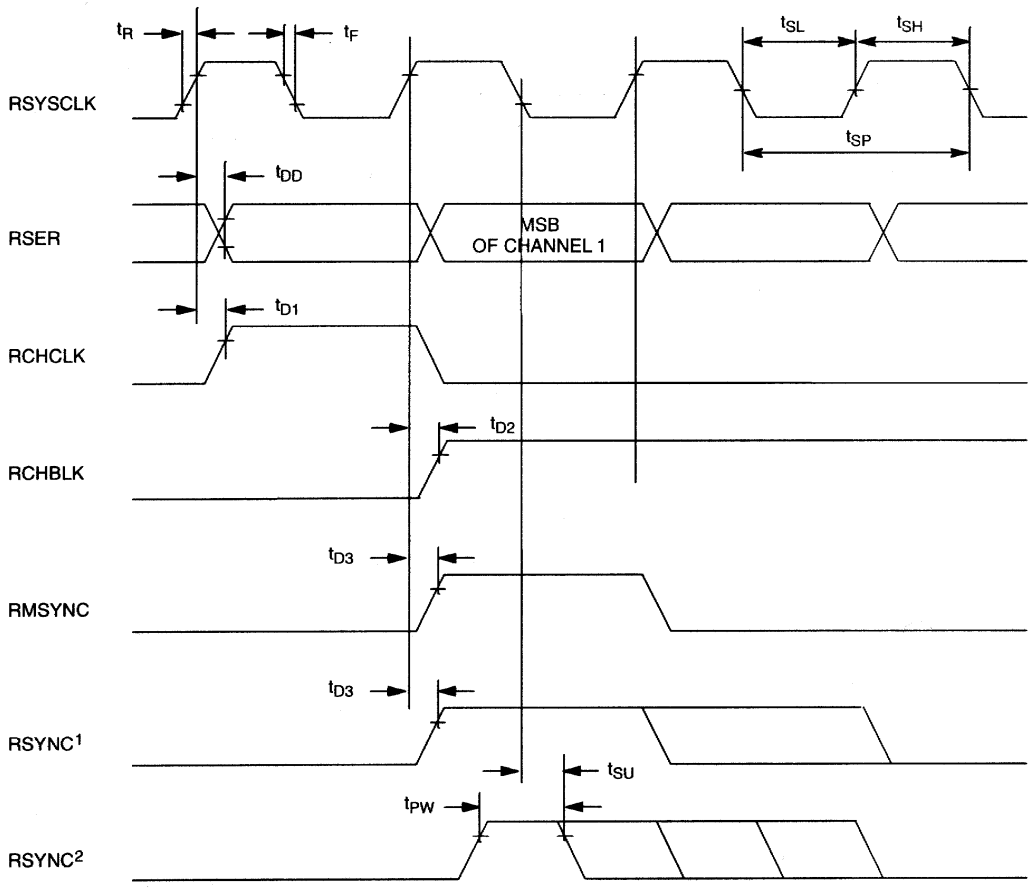


NOTES:

1. RSYNC is in the output mode (RCR1.5=0).

2. RLCLK will only pulse high during Sa bit locations as defined in RCR2; no relationship between RLCLK and RLCLK and RFSYNC is implied.

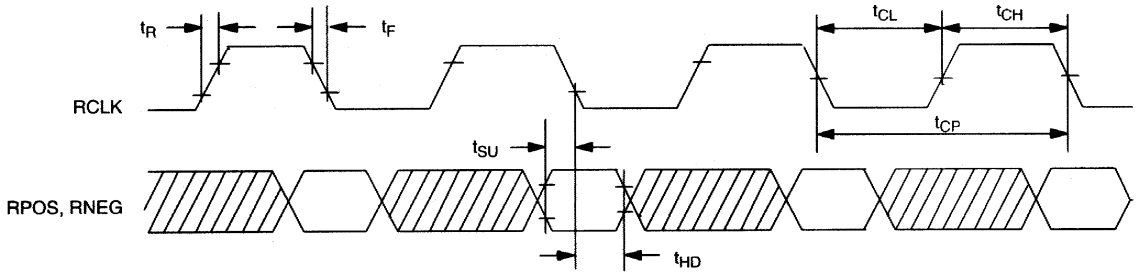
RECEIVE SYSTEM SIDE AC TIMING Figure 12-5



NOTES:

1. RSYNC is in the output mode (RCR 1.5=0).
2. RSYNC is in the input mode (RCR1.5=1).

RECEIVE LINE INTERFACE AC TIMING Figure 12-6



AC CHARACTERISTICS - TRANSMIT SIDE

(0°C to 70°C; V_{DD}=5V ± 10% for DS21Q43AT; -40°C to +85°C; V_{DD}=5V ± 10% for DS21Q43ATN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_{CP}		488		ns	
TCLK Pulse Width	t_{CH}	75			ns	
	t_{CL}	75			ns	
TSYSCLK Period	t_{SP}		648		ns	1
	t_{SP}		488		ns	2
TSYSCLK Pulse Width	t_{SH}	50			ns	
	t_{SL}	50			ns	
TSER, TSYNC and TLINK Set Up to TCLK Falling or TSER, TFSYNC Set Up to TSYSCLK Falling	t_{SU}	20			ns	
TSYNC, TFSYNC Pulse Width	t_{PW}	50			ns	3
TSER, TSYNC and TLINK Hold from TCLK Falling or TSER	t_{HD}	20			ns	
TCLK or TSYSCLK Rise and Fall Times	t_R, t_F			25	ns	
Delay TCLK to TPOS/TNEG Valid	t_{DD}			75	ns	
Delay TCLK to TCHCLK or TSYSCLK to TCHCLK	t_{D1}			75	ns	
Delay TCLK to TCHBLK or TSYSCLK to TCHBLK	t_{D2}			75	ns	
Delay TCLK to TSYNC	t_{D3}			75	ns	
Delay TCLK to TLCLK	t_{D4}			75	ns	

See Figures 12-7 to 12-9 for details.

NOTES:

1. TSYSCLK = 1.544 MHz.
2. TSYSCLK = 2.048 MHz.
3. TSYNC in input mode.

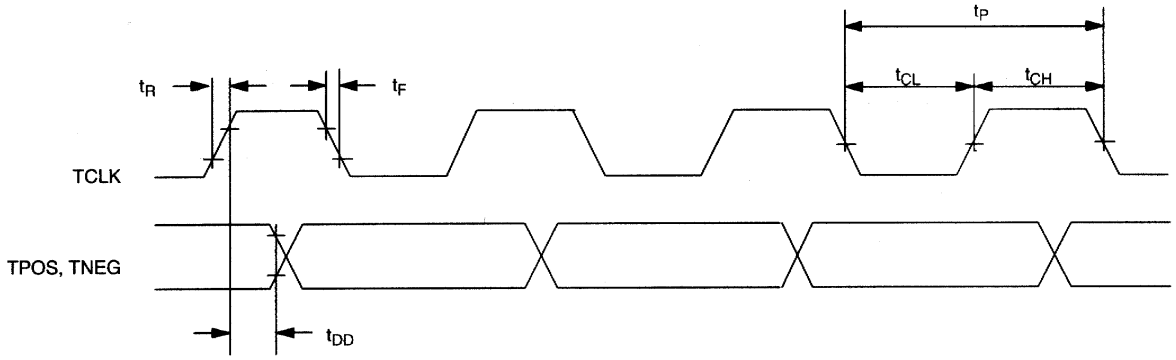
AC CHARACTERISTICS - MULTIPLEXED PARALLEL PORT (MUX=1)

(0°C to 70°C; V_{DD}=5V ± 10% for DS21Q43AT; -40°C to +85°C; V_{DD}=5V ± 10% for DS21Q43ATN)

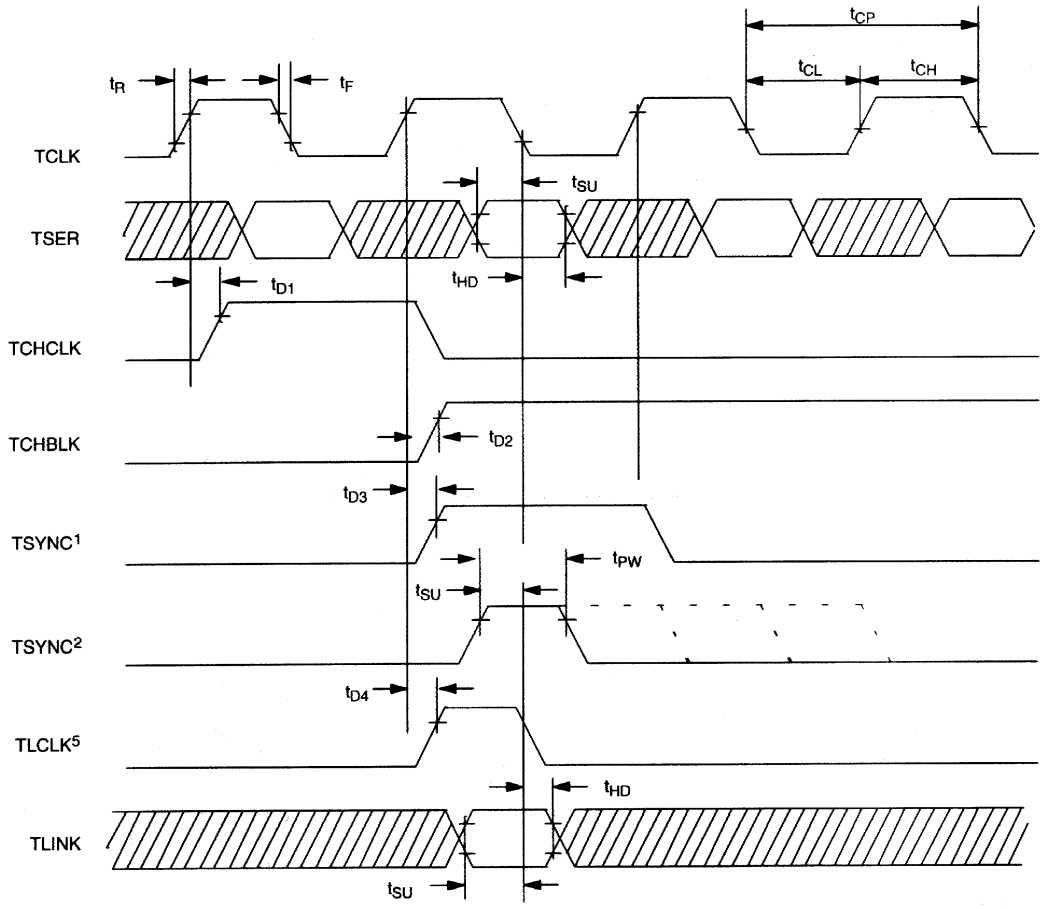
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	200			ns	
Pulse Width, DS Low or $\overline{RD}$ High	PW_{EL}	100			ns	
Pulse Width, DS High or $\overline{RD}$ Low	PW_{EH}	100			ns	
Input Rise/Fall Times	t_R, t_F			20	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS High	t_{RWS}	50			ns	
$\overline{CS}$, FS0, FS1 Setup Time before DS, $\overline{WR}$ or $\overline{RD}$ Active	t_{CS}	20			ns	
$\overline{CS}$, FS0, FS1 Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		50	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid to AS or ALE Fall	t_{ASL}	15			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time DS, $\overline{WR}$ or $\overline{RD}$ to AS or ALE Rise	t_{ASD}	20			ns	
Pulse Width AS or ALE High	PW_{ASH}	30			ns	
Delay Time, AS or ALE to DS, $\overline{WR}$ or $\overline{RD}$	t_{ASED}	10			ns	
Output Data Delay Time from DS or $\overline{RD}$	t_{DDR}	20		80	ns	
Data Setup Time	t_{DSW}	50			ns	

See Figures 12-1 to 12-3 for details.

TRANSMIT LINE INTERFACE AC SIDE TIMING Figure 12-7



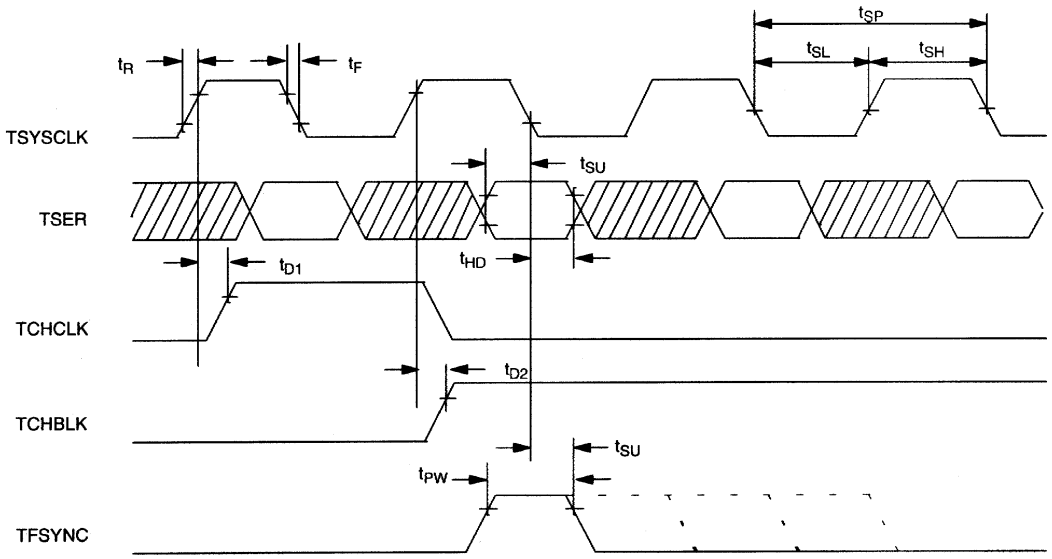
TRANSMIT SIDE AC TIMING Figure 12-8



NOTES:

1. TSYNC is in the output mode (TCR1.0=1).
2. TSYNC is in the input mode (TCR1.0=0).
3. TSER is sampled on the falling edge of TCLK when the transmit side elastic store is disabled.
4. TCHCLK and TCHBLK are synchronous with TCLK when the transmit side elastic store is disabled.
5. TLINK is only sampled during Sa bit locations as defined in TCR2; no relationship between TLCLK/TLINk and TSYNC is implied.

TRANSMIT SYSTEM SIDE AC TIMING Figure 12-9



NOTES:

1. TSER is only sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.
2. TCHCLK and TCHBLK are synchronous with TSYSCLK when the transmit side elastic store is enabled.

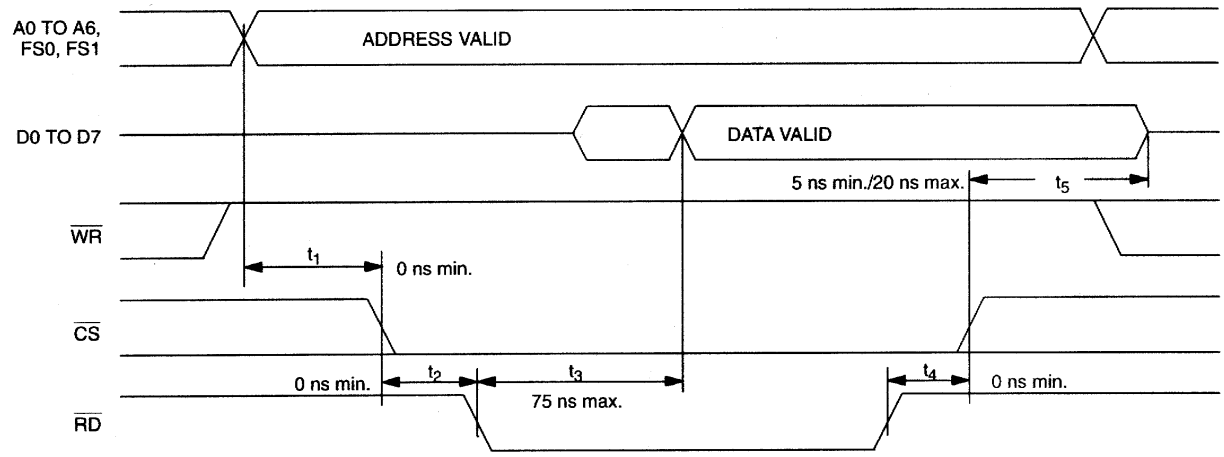
AC CHARACTERISTICS - NON-MULTIPLEXED PARALLEL PORT (MUX=0)

(0°C to 70°C; V_{DD}=5V ± 10% for DS21Q43AT; -40°C to +85°C; V_{DD}=5V ± 10% for DS21Q43ATN)

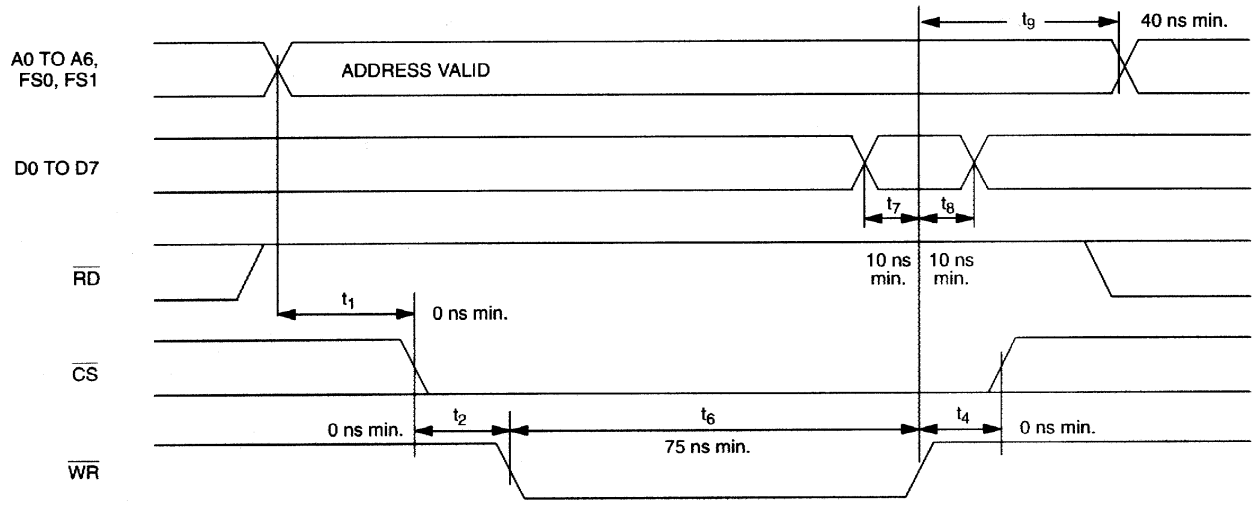
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Set Up Time for A0 to A6, FS0, FS1 Valid to $\overline{CS}$ Active	t_1	0			ns	
Set Up Time for $\overline{CS}$ Active to either $\overline{RD}$, $\overline{WR}$, or DS Active	t_2	0			ns	
Delay Time from either $\overline{RD}$ or DS Active to Data Valid	t_3			75	ns	
Hold Time from either $\overline{RD}$, $\overline{WR}$, or DS Inactive to $\overline{CS}$ Inactive	t_4	0			ns	
Hold Time from $\overline{CS}$ Inactive to Data Bus 3-State	t_5	5		20	ns	
Wait Time from either $\overline{WR}$ or DS Active to Latch Data	t_6	75			ns	
Data Set Up Time to either $\overline{WR}$ or DS Inactive	t_7	10			ns	
Data Hold Time from either $\overline{WR}$ or DS Inactive	t_8	10			ns	
Address Hold Time	t_9	10			ns	

See Figures 13-10 to 13-13 for details.

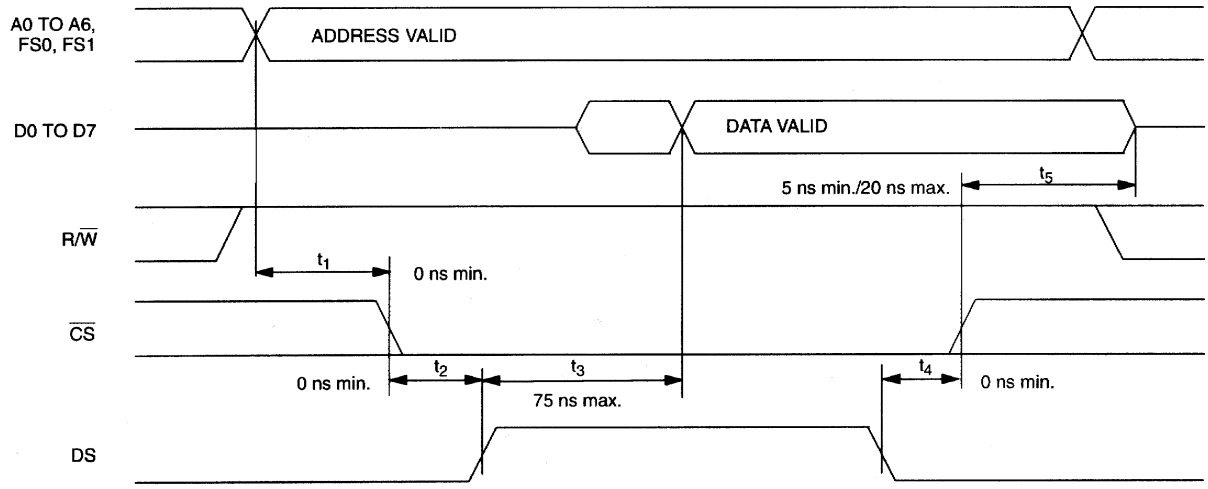
INTEL BUS READ AC TIMING (BTS=0/MUX=0) Figure 12-10



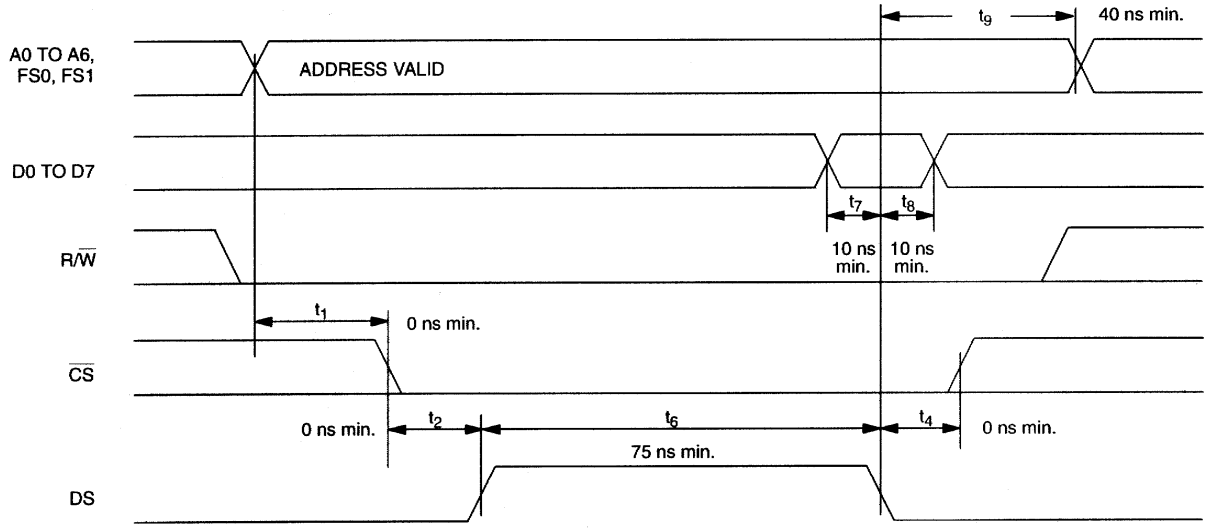
INTEL BUS WRITE AC TIMING (BTS=0/MUX=0) Figure 12-11



MOTOROLA BUS READ AC TIMING (BTS=1/MUX=0) Figure 12-12



MOTOROLA BUS WRITE AC TIMING (BTS=1/MUX=0) Figure 12-13



DS21Q43A 128-PIN TQFP

PKG	128-PIN	
DIM	MIN	MAX
A	-	1.60
A1	0.05	-
A2	1.35	1.45
B	0.17	0.27
C	0.09	0.20
D	21.80	22.20
D1	20.00 BSC	
E	15.80	16.20
E1	14.00 BSC	
e	0.50 BSC	
L	0.45	0.75

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