



CY8CKIT-030

PSoC[®] 3 Development Kit Guide

Doc. # 001-61038 Rev. *J

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1. Introduction



Thank you for your interest in the CY8CKIT-030 PSoC[®] 3 Development Kit. This kit allows you to develop precision analog and low-power designs using PSoC 3. You can design your own projects with PSoC Creator[™] or alter the sample projects provided with this kit.

The CY8CKIT-030 PSoC 3 Development Kit is based on the PSoC 3 family of devices. PSoC 3 is a Programmable System-on-Chip[™] platform for 8-bit and 16-bit applications. It combines precision analog and digital logic with a high-performance CPU. With PSoC, you can create the exact combination of peripherals and integrated proprietary IP to meet your application requirements.

1.1 Kit Contents

The PSoC 3 Development Kit contains:

- Development board
- Kit DVD
- Quick start guide
- USB A to mini-B cable
- 3.3-V LCD module

Inspect the contents of the kit; if you find any part missing, contact your nearest Cypress sales office for help.

1.2 PSoC Creator

Cypress's PSoC Creator software is a state-of-the-art, easy-to-use integrated development environment (IDE) that introduces a hardware and software design environment based on classic schematic entry and revolutionary embedded design methodology.

With PSoC Creator, you can:

- Create and share user-defined, custom peripherals using hierarchical schematic design.
- Automatically place and route select components and integrate simple glue logic, normally located in discrete muxes.
- Trade off hardware and software design considerations allowing you to focus on what matters and getting to market faster.

PSoC Creator also enables you to tap into an entire tools ecosystem with integrated compiler tool chains, RTOS solutions, and production programmers to support both PSoC 3 and PSoC 5LP.

1.3 Additional Learning Resources

Visit <http://www.cypress.com> for additional learning resources in the form of datasheets, application notes, and technical reference manual.

1.3.1 Beginner Resources

[AN54181 - Getting Started with PSoC® 3](#)

[PSoC Creator Training](#)

1.3.2 Engineers Looking for More

[AN54460 - PSoC 3®, PSoC 4, and PSoC 5LP Interrupts](#)

[AN52705 - PSoC 3® and PSoC 5LP - Getting Started with DMA](#)

[AN52701 - PSoC 3® and PSoC 5LP - Getting Started with Controller Area Network \(CAN\)](#)

[AN54439 - PSoC 3® and PSoC 5LP External Crystal Oscillators](#)

[AN52927 - PSoC 3® and PSoC 5LP - Segment LCD Direct Drive](#)

Cypress continually strives to provide the best support. Click [here](#) to view a growing list of application notes for PSoC 3, PSoC 4, and PSoC 5LP.

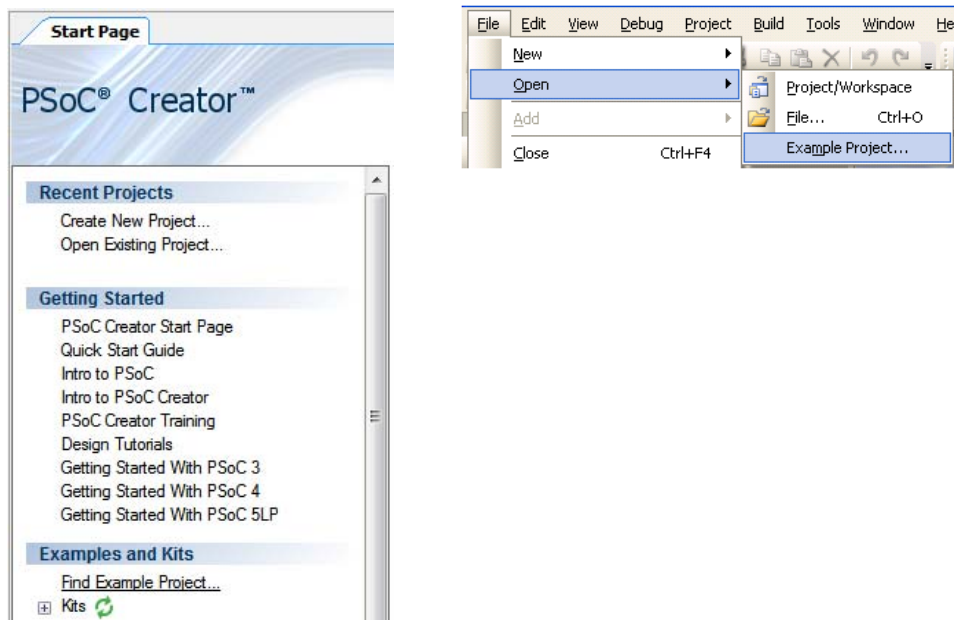
1.3.3 Learning from Peers

[Cypress Developer Community Forums](#)

1.3.4 More Code Examples

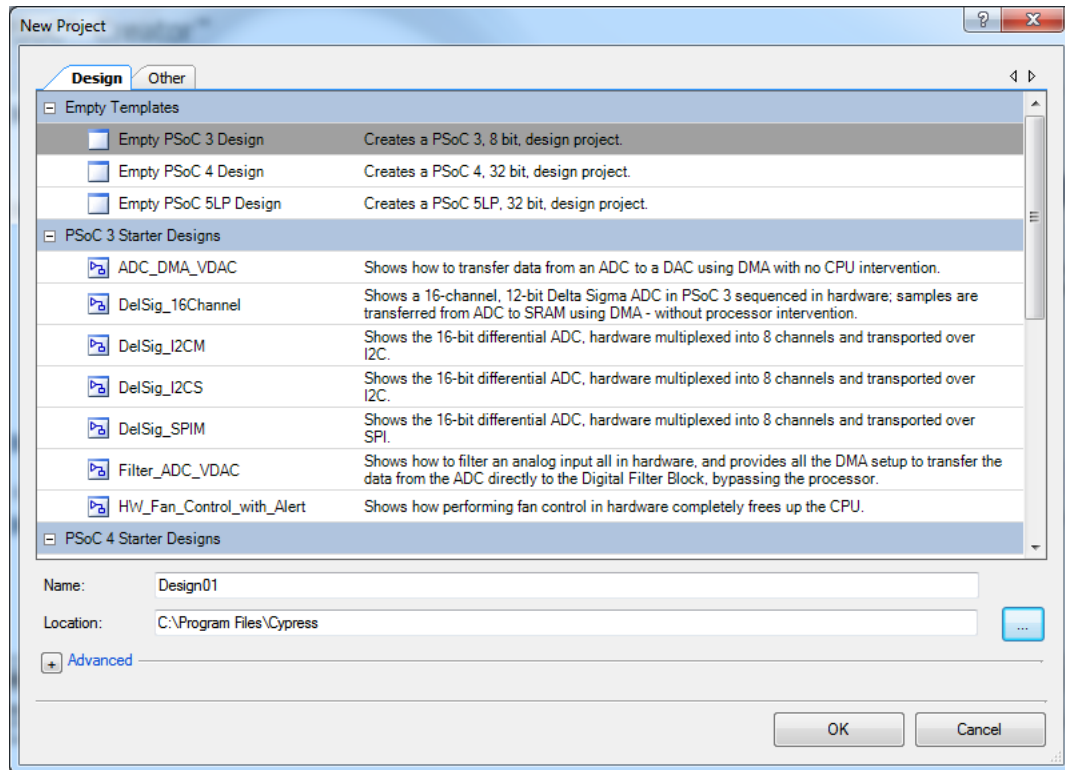
PSoC Creator provides several example projects that make code development fast and easy. To access these example projects, click on **Find Example Project...** under the **Example and Kits** section in the **Start Page** of PSoC Creator or navigate to **File > Open > Example Project....**

Figure 1-1. Find Example Project



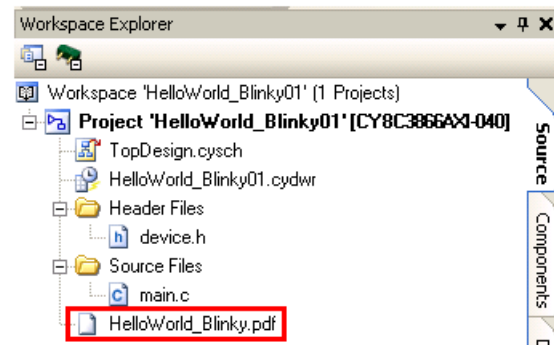
The **Find Example Project** section has various filters that help you locate the most relevant project. PSoC Creator provides several starter designs. These designs highlight features that are unique to PSoC devices. They allow you to create a design with various components, instead of creating an empty design; the code is also provided. To use a starter design for your project, navigate to **File > New > Project** and select the design required.

Figure 1-2. New Project



The starter designs and the example project contain a PDF within the project that explains the features of the project and its configuration.

Figure 1-3. Project PDF Location



The example projects and starter designs are designed for the CY8CKIT-001 PSoC Development Kit. However, these projects can be converted for use with the CY8CKIT-030 PSoC 3 Development Kit or CY8CKIT-050 PSoC 5 Development Kit by following the procedure in the knowledge base article [Migrating Project from CY8CKIT-001 to CY8CKIT-030 or CY8CKIT-050](#).

1.4 Documentation Conventions

Table 1-1. Document Conventions for Guides

| Convention | Usage |
|--------------------------|--|
| Courier New | Displays file locations, user entered text, and source code: C:\...cd\icc\ |
| <i>Italics</i> | Displays file names and reference documentation: Read about the <i>sourcefile.hex</i> file in the <i>PSoC Designer User Guide</i> . |
| [Bracketed, Bold] | Displays keyboard commands in procedures: [Enter] or [Ctrl] [C] |
| File > Open | Represents menu paths: File > Open > New Project |
| Bold | Displays commands, menu paths, and icon names in procedures: Click the File icon and then click Open . |
| Times New Roman | Displays an equation: $2 + 2 = 4$ |
| Text in gray boxes | Describes cautions or unique functionality of the product. |

2. Getting Started



This chapter describes how to install and configure the PSoC 3 Development Kit. The [Kit Operation chapter on page 11](#) explains how to program a PSoC 3 device with PSoC Programmer and use the kit with the help of a code example. To reprogram the PSoC device with PSoC Creator, see the installation instructions for PSoC Creator. The [Hardware chapter on page 14](#) details the hardware operation. The [Code Examples chapter on page 30](#) provides instructions to create a simple code example. The Appendix section provides the [Schematics](#), [Board Layout](#), [Bill of Materials \(BOM\)](#) and other useful information regarding the PSoC 3 Development Kit.

2.1 DVD Installation

Follow these steps to install the PSoC 3 Development Kit software:

1. Insert the kit DVD into the DVD drive of your PC. The DVD is designed to auto-run and the kit menu appears.

Figure 2-1. Kit Menu



Note If auto-run does not execute, double-click *cyautorun.exe* on the root directory of the DVD.



After the installation is complete, the kit contents are available at the following location:

```
<Install_Directory>\Cypress\PSoC 3 Development Kit\<version>
```

2.2 Install Hardware

No hardware installation is required for this kit.

2.3 Install Software

When installing the PSoC 3 Development Kit, the installer checks if your system has the required software. These include PSoC Creator, PSoC Programmer, Windows Installer, .NET, and Keil Compiler. If these applications are not installed, the installer installs them in your PC before installing the kit. If the Acrobat Reader application is not installed in your PC, then the installer provides the link to install the same; this does not prevent kit installation. Note that Acrobat Reader is required to view the kit documents. Install the following software from the kit DVD:

- PSoC Creator 3.0 or later
- PSoC Programmer 3.19.1 or later
 - Note** When installing PSoC Programmer, select **Typical** on the Installation Type page.
- Code examples (provided in the Firmware folder)

Important for Win7 and Vista Users: Rename the `_tools.ini` file in `<Install_Directory>:\PSoC Creator\<version>\PSoC Creator\import\keil\pk51\<version>` to `tools.ini` for the Keil registration to be successful.

2.4 Uninstall Software

The software can be uninstalled using one of the following methods:

- Go to **Start > Control Panel > Programs > Uninstall a program**; select the **Uninstall** button in Windows 7.
- Go to **Start > All Programs > Cypress > Cypress Update Manager > Cypress Update Manager**; select the **Uninstall** button next to the software to be uninstalled.
- Insert the installation DVD and click **Install PSoC 3 Development Kit** button. In the **CyInstaller for PSoC 3 Development Kit 1.0** window, select **Remove** from the Installation Type drop-down menu. Follow the instructions to uninstall.

2.5 Verify Kit Version

To know the kit revision, look for the white sticker on the bottom left, on the reverse of the kit box. If the revision reads CY8CKIT-030A, then, you own the latest version.

To upgrade CY8CKIT-030 to CY8CKIT-030A, you can purchase our latest kits at:

<http://www.cypress.com/go/CY8CKIT-030>

3. Kit Operation

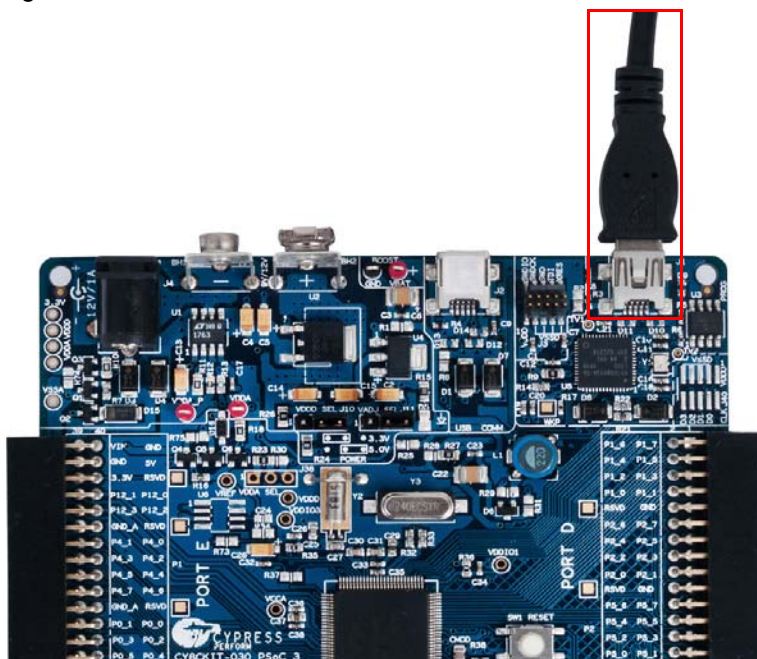


The code examples in the PSoC 3 Development Kit help you develop precision analog applications using the PSoC 3 family of devices. The board also has hooks to enable low-power measurements for low-power application development and evaluation.

3.1 Programming PSoC 3 Device

The default programming interface for the board is a USB-based onboard programming interface. To program the device, plug the USB cable to the programming USB connector J1, as shown in [Figure 3-1](#).

Figure 3-1. Connect USB Cable to J1



When plugged in, the board enumerates as DVKProg (unconfigured). The DVKProg is configured after opening either the PSoC Creator or PSoC Programmer application. If either of these applications are opened before connecting the DVK to the PC, the DVKProg configuration happens instantaneously.

After enumeration, initiate a build of the code example and program using PSoC Creator.

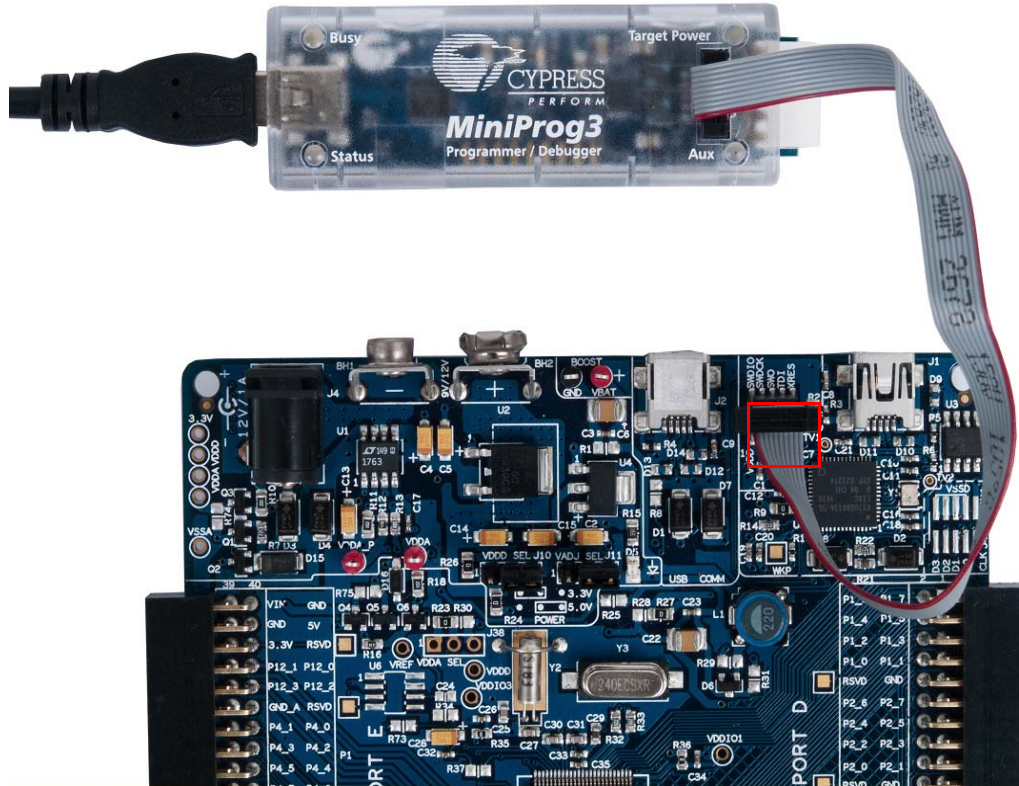
When using onboard programming, it is not necessary to power the board from the 12-V or 9-V DC supply or a battery. You can use the USB power to the programming section.

If the board is already powered from another source, plugging in the programming USB does not damage the board.

The PSoC 3 device on the board can also be programmed using a MiniProg3 (CY8CKIT-002). To use MiniProg3 for programming, use the connector J3 on the board, as shown in [Figure 3-2](#).

Note The MiniProg3 (CY8CKIT-002) is not part of the PSoC 3 Development Kit contents. It can be purchased from the [Cypress Online Store](#).

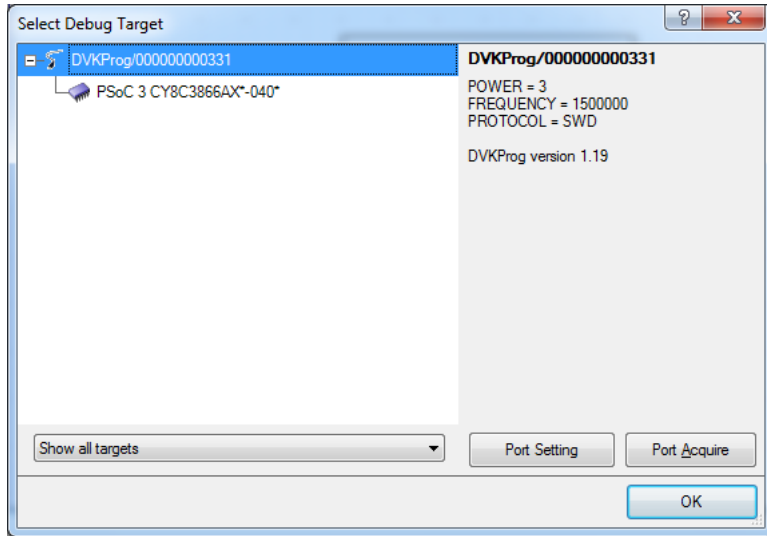
Figure 3-2. Connect MiniProg3



With the MiniProg3, programming is similar to the onboard programmer; however, the setup enumerates as a MiniProg3.

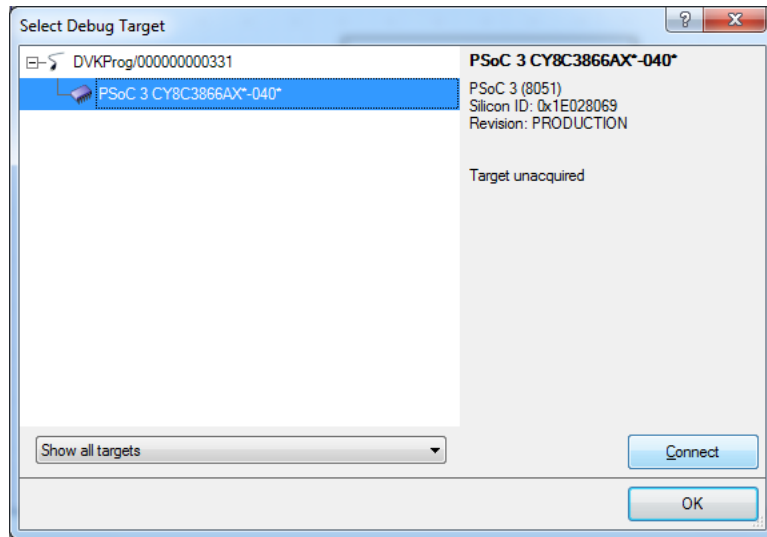
The Select Debug Target window may be displayed, as shown in [Figure 3-3](#).

Figure 3-3. Select Debug Target Window



Click **Port Acquire**. The window appears as follows. Click **Connect** to start programming.

Figure 3-4. Port Acquire > Connect



4. Hardware

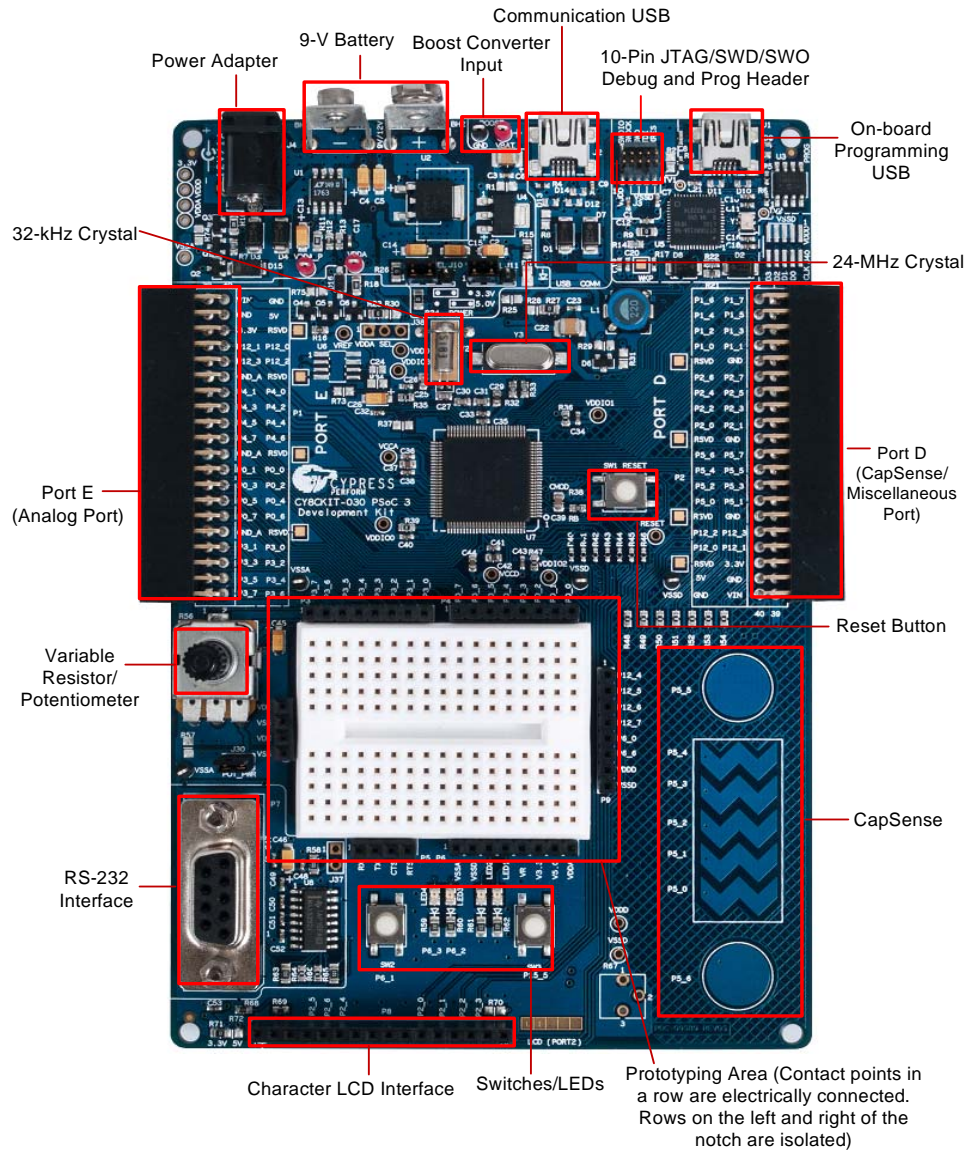


4.1 System Block Diagram

The PSoC 3 Development Kit has the following sections:

- Power supply system
- Programming interface
- USB communications
- Boost convertor
- PSoC 3 and related circuitry
- 32-kHz crystal
- 24-MHz crystal
- Port E (analog performance port) and port D (CapSense® or generic port)
- RS-232 communications interface
- Prototyping area
- Character LCD interface
- CapSense buttons and sliders

Figure 4-1. PSoC 3 Development Kit Details



4.2 Functional Description

4.2.1 Power Supply

The power supply system on this board is versatile; input supply can be from the following sources:

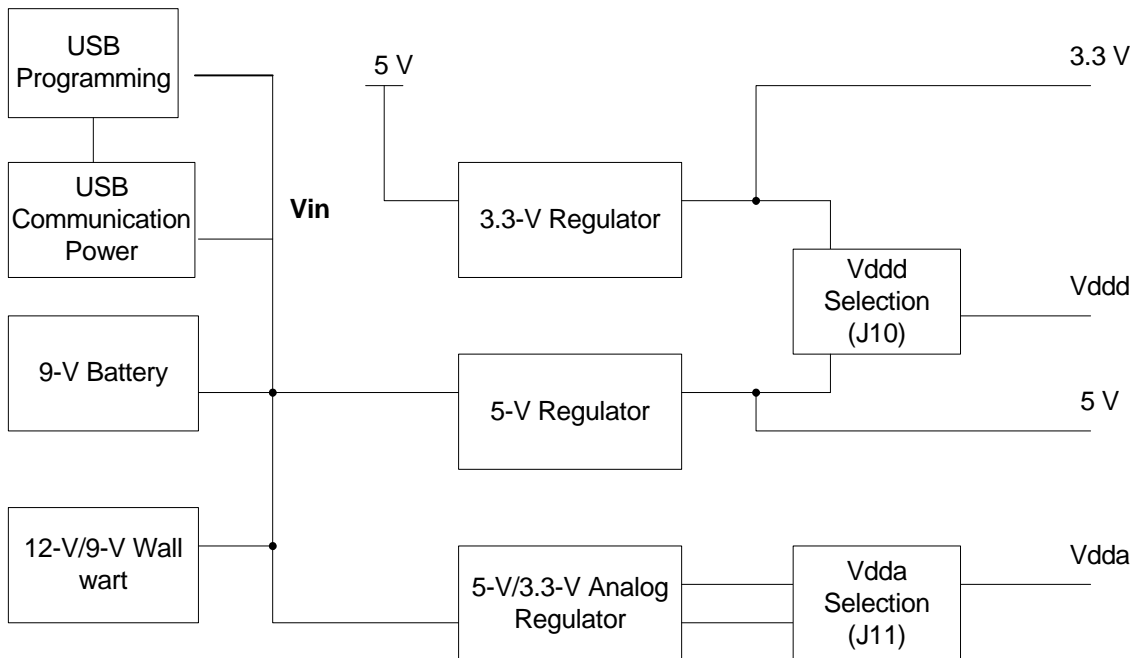
- 9-V or 12-V wall wart supply using connector J4
- 9-V battery connector using connectors BH1 and BH2
- USB power from communications section using connector J2
- USB power from the onboard programming section using connector J1
- Power from JTAG/SWD programming interface using connector J3
- Power through boost convertor that uses the input test points VBAT and GND

The board power domain has five rails:

- **Vin rail:** This is where the input of the onboard regulators are connected. This domain is powered through protection diodes.
- **5-V rail:** This is the output of the 5-V regulator U2. The rail has a fixed 5-V output regardless of jumper settings. The voltage in this rail can be less than 5 V only when the board is powered by the USB. This 5-V rail powers the circuits that require fixed 5-V supply.
- **3.3-V rail:** This is the output of the 3.3-V regulator U4. This rail remains 3.3 V regardless of jumper settings or power source changes. It powers the circuits requiring fixed 3.3-V supply such as the onboard programming section.
- **Vddd rail:** This rail provides power to the digital supply for the PSoC device. It can be derived from either the 5-V or 3.3-V rail. The selection is made using J10 (3-pin jumper).
- **Vdda rail:** This rail provides power to the analog supply of the PSoC device. It is the output of a low-noise regulator U1. The regulator is a variable output voltage and can be either 3.3 V or 5 V. This is done by changing the position on J11 (3-pin jumper).

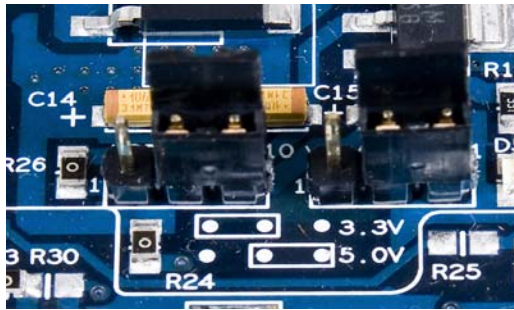
The following block diagram shows the structure of the power system on the board.

Figure 4-2. Power System Structure



4.2.1.1 Power Supply Jumper Settings

Figure 4-3. Jumper Settings



Two jumpers govern the power rails on the board. J10 is responsible for the selection of V_{ddd} (digital power) and J11 selects V_{dda} (analog power).

The jumper settings for each power scheme are as follows.

| Powering Scheme | Jumper Settings |
|--|---|
| V _{dda} = 5 V, V _{ddd} = 5 V | J10 in 5-V setting and J11 in 5-V setting. |
| V _{dda} = 3.3 V, V _{ddd} = 3.3 V | J10 in 3.3-V setting and J11 in 3.3-V setting. |
| V _{dda} = 5 V, V _{ddd} = 3.3 V | J10 in 3.3-V setting and J11 in 5-V setting. |
| V _{dda} = 3.3 V, V _{ddd} = 5 V | Can be achieved, but is an invalid condition because the PSoC 3 silicon performance cannot be guaranteed. |

Warning

- Ensure that the V_{dda} is always higher than V_{ddd}—J11 should not be set to 3.3-V position when J10 is at 5-V position.
- The power supply of the I/Os, V_{ddio}, is connected to V_{ddd}. Therefore, any input voltage to the PSoC I/Os must not exceed the V_{ddd}.
- When USB power is used, ensure a 3.3-V setting on both J10 and J11. This is because the 5-V rail of the USB power is not accurate and is not recommended. If you require 5-V operation, it is recommended to use an external power supply adapter or a 9-V battery

4.2.1.2 Grounding Scheme

The board design considers analog designs as major target applications. Therefore, the grounding scheme in the board is unique to ensure precision analog performance.

The board has three types of ground:

- GND - This is the universal ground where all the regulators are referred. Both V_{ssd} and V_{ssa} connect to this ground through a star connection.
- V_{ssd} - This is the digital ground and covers the digital circuitry on the board, such as RS-232 and LCD.
- V_{ssa} - This is the analog ground and covers the grounding for analog circuitry present on the board, such as the reference block.

When creating custom circuitry in the prototyping area provided on the board, remember to use the V_{ssa} for the sensitive analog circuits and V_{ssd} for the digital ones.

Port E on the board is the designated analog expansion connector. This connector brings out ports 0, 3, and 4, which are the best performing analog ports on PSoC 3 and PSoC 5 devices. Port E has two types of grounds. One is the analog ground (GND_A in the silkscreen, Vssa in the schematic), which connects directly to the analog ground on the board. The other ground, known as GND, is used for the digital and high-current circuitry on the expansion board. This differentiation on the connector grounds helps the expansion board designer to separate the analog and digital ground on any high-precision analog boards being designed for port E.

4.2.1.3 *Low-Power Functionality*

The kit also facilitates application development, which requires low power consumption. Low-power functions require a power measurement capability, also available in this kit.

The analog supply is connected to the device through the 0- Ω resistor (R23). By removing this resistor and connecting an ammeter in series using the test points, Vdda_p and Vdda, you can measure the analog power used by the system.

The digital supply can be monitored by removing the connection on jumper J10 and connecting an ammeter in place of the short. This allows to measure the digital power used by the system.

The board provides the ability to measure analog and digital power separately. To measure power at a single point, rather than at analog and digital separately, remove resistor R23 to disconnect the analog regulator from powering the Vdda and short Vdda and Vddd through R30. The net power can now be measured at jumper J10 similar to the digital power measurement. To switch repeatedly between R23 and R30, moving around the 0- Ω resistors can be discomforting. Hence, a J38 (unpopulated) is provided to populate a male 3-pin header and have a shorting jumper in the place of R23/R30.

While measuring device power, make the following changes in the board to avoid leakage through other components that are connected to the device power rails.

- Disconnect the RS-232 power by disconnecting R58. An additional jumper capability is available as J37 if you populate it with a 2-pin male header.
- Disconnect the potentiometer by disconnecting J30.
- Ground the boost pins if boost operation is not used by populating R1, R28, and R29. Also, make sure R25 and R31 are not populated.

4.2.2 Programming Interface

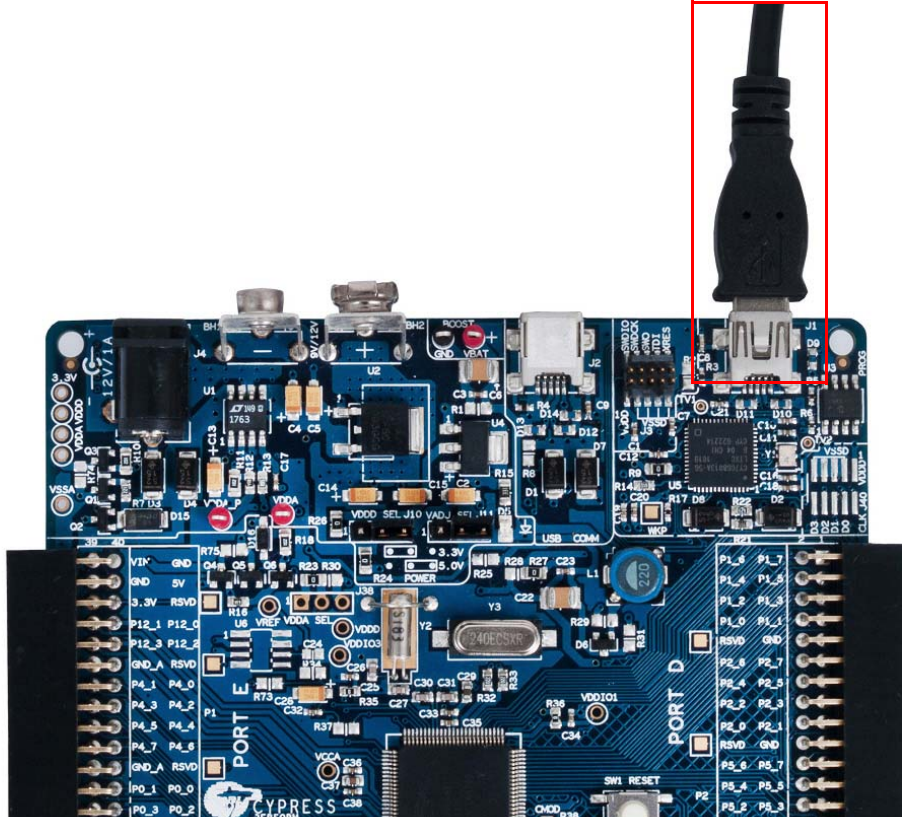
This kit allows programming in two modes:

- Using the onboard programming interface
- Using the JTAG/SWD programming interface with a MiniProg3

4.2.2.1 *Onboard Programming Interface*

The onboard programmer interfaces with your PC through a USB connector, as shown in [Figure 4-4](#).

Figure 4-4. Onboard Programming Interface



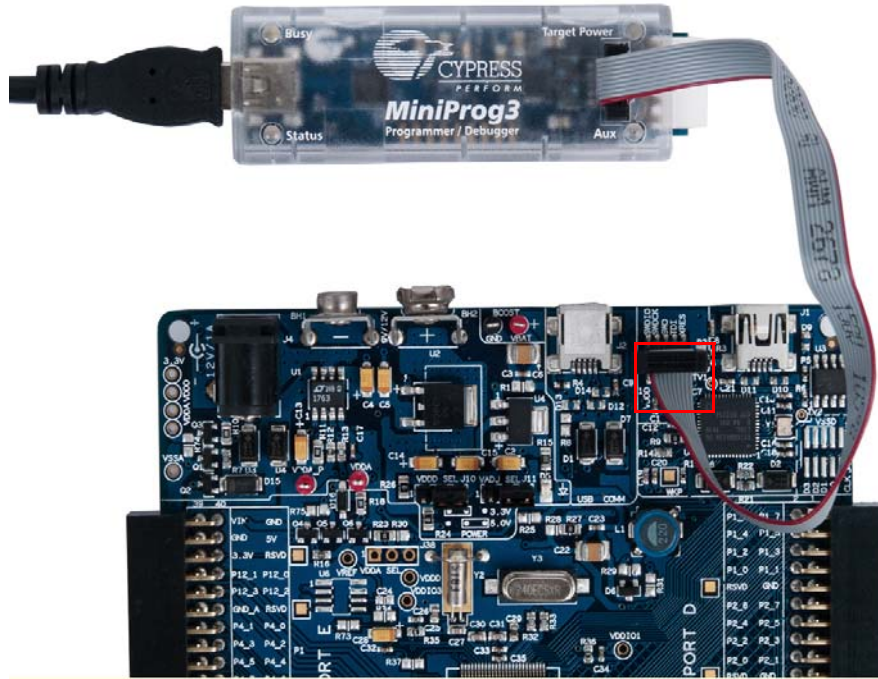
When the USB programming is plugged into the PC, it enumerates as DVKProg and you can use the normal programming interface from PSoC Creator to program this board through the onboard programmer. Pins P1[0] and P1[1] are connected to the onboard programmer. If you are using the onboard programmer, these pins should not be used for any other function.

A 0-Ω resistor R9 is provided on the board to disconnect power to the onboard programmer.

4.2.2.2 JTAG/SWD Programming

Apart from the onboard programming interface, the board also provides the option of using the MiniProg3. This interface is much faster than the onboard program interface. The JTAG/SWD programming is done through the 10-pin connector, J3.

Figure 4-5. JTAG/SWD Programming

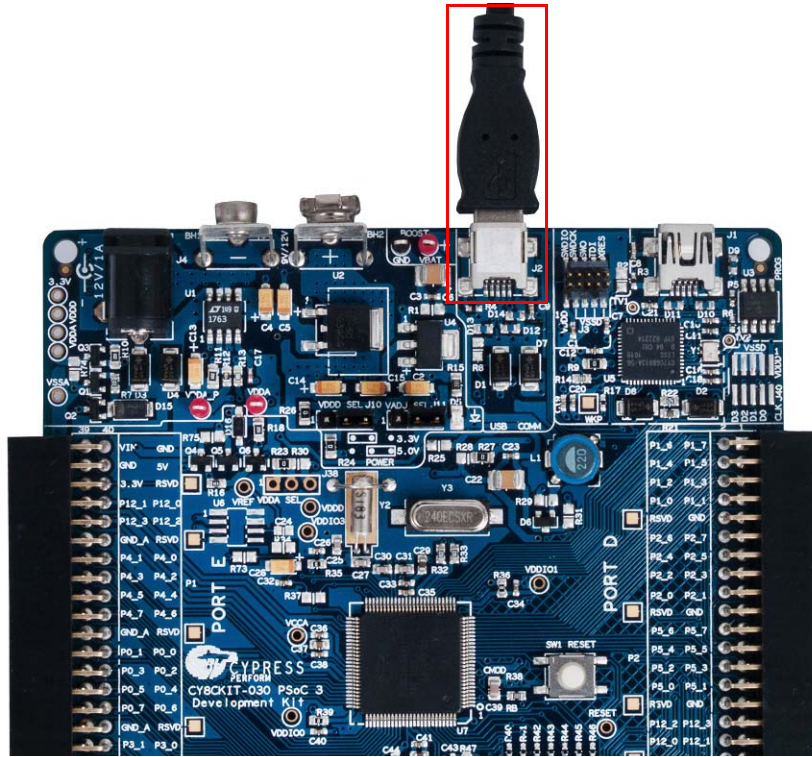


The JTAG/SWD programming using J3 requires the MiniProg3 programmer, which can be purchased from <http://www.cypress.com/go/CY8CKIT-002>.

4.2.3 USB Communication

The board has a USB communications interface that uses the connector, as shown in [Figure 4-6](#). The USB connector connects to the D+ and D– lines on the PSoC to enable development of USB applications using the board. This USB interface can also supply power to the board, as discussed in [Power Supply on page 15](#).

Figure 4-6. USB Interface



4.2.4 Boost Converter

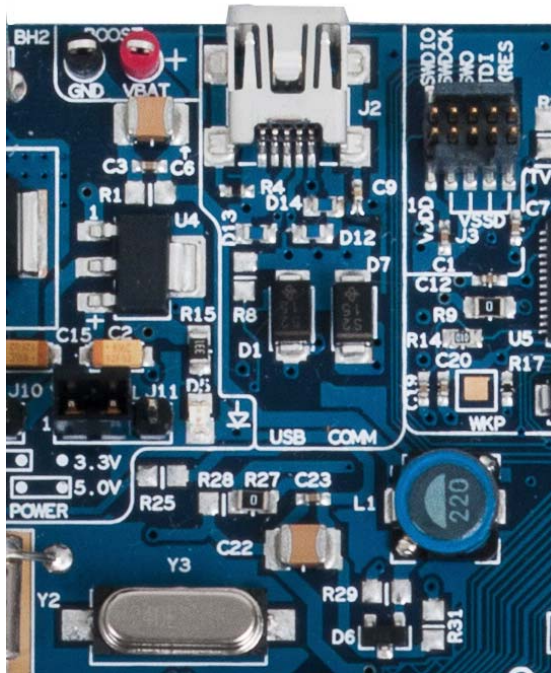
The PSoC 3 device has the unique capability of working from a voltage supply as low as 0.5 V. This is possible using the boost converter. The boost converter uses an external inductor and a diode. These components are prepopulated on the board. [Figure 4-7](#) shows the boost converter.

To enable the boost converter functionality, make the following hardware changes on the board:

- Populate resistors R25, R27, R29, and R31
- Ensure that R1 and R28 are not populated

After making these changes, you can configure the project to make a boost converter-based design. The input power supply to the boost converter must be provided through the test points marked Vbat and GND.

Figure 4-7. Boost Converter



4.2.5 32-kHz and 24-MHz Crystal

PSoC 3 has an on-chip real time clock (RTC), which can function in sleep. This requires an external 32-kHz crystal, which is provided on the board to facilitate RTC-based designs. The PSoC 3 also has an external MHz crystal option in applications where the IMO tolerance is not satisfactory. In these applications, the board has a 24-MHz crystal to provide an accurate main oscillator.

4.2.6 Protection Circuit

A reverse-voltage and over-voltage protection circuit is added to the expansion port on the 5-V and 3.3-V lines.

The protection circuit consists of two P-channel MOSFET on the power line, allowing the current to flow from input to output depending on the voltages applied at the external board connector. [Figure 4-8](#) and [Figure 4-9](#) are protection circuits placed between EBK and the onboard components on the 5-V and 3.3-V lines.

Figure 4-8. Schematic for Protection Circuit on 5-V Power Line

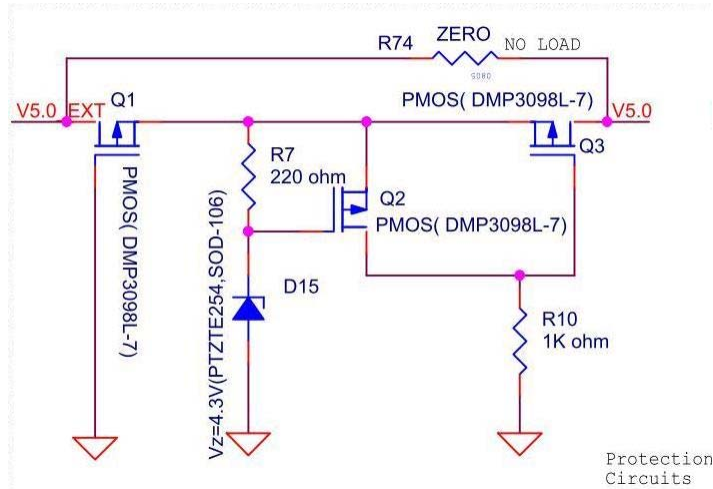
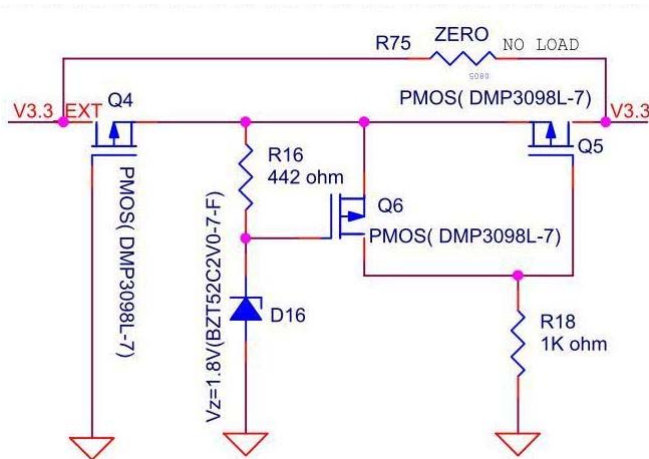


Figure 4-9. Schematic for Protection Circuit on 3.3-V Power Line



4.2.6.1 Functional Description

The protection circuit will protect from a maximum over-voltage or reverse-voltage of 12 V. The cut-off voltage on the 5-V line is 5.7 V and on the 3.3-V line is 3.6 V. This means, if you apply more than this voltage level from the external board connector side, the p-MOS Q5 will turn off, thus protecting PSoC and other onboard components. The current consumption of these protection circuits is less than 6 mA.

When voltage from the external connector is between 1.8 V and 3.3 V, the p-MOS Q4 conducts. Because the voltage across R16 is less than the threshold voltage (V_{th}) of p-MOS Q6, it will turn off and the p-MOS Q5 conducts, allowing voltage supply to the DVK.

When the external power supply exceeds 3.3 V, the p-MOS Q5 starts conducting. This eventually turns off p-MOS Q6 at 3.6 V, protecting the DVK from over-voltage.

When a reverse voltage is applied across the protection circuit from the external connector side, Q4 P-MOS will turn off, thus protecting the components on the board from reverse voltage.

If you are using the regulator power supply from the board to power the external modules, both the P-MOS Q4 and Q5 will always be in the On state, allowing the flow of current with a maximum of 22 mV drop across the circuit when the current consumed by the external module is 150 mA.

Note The working of protection circuit on the 3.3-V and 5-V lines is as described. For the purpose of explanation, the annotation of 3.3-V protection circuitry ([Figure 4-9](#)) is used.

4.2.7 PSoC 3 Development Kit Expansion Ports

The PSoC 3 Development Kit has two expansion ports, port D and port E, each with their own unique features.

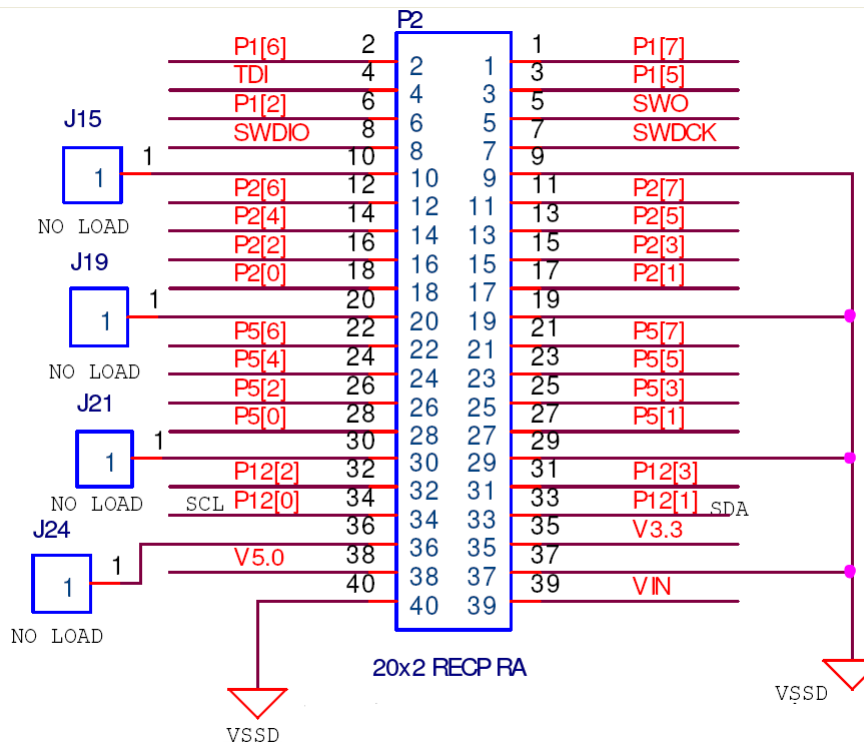
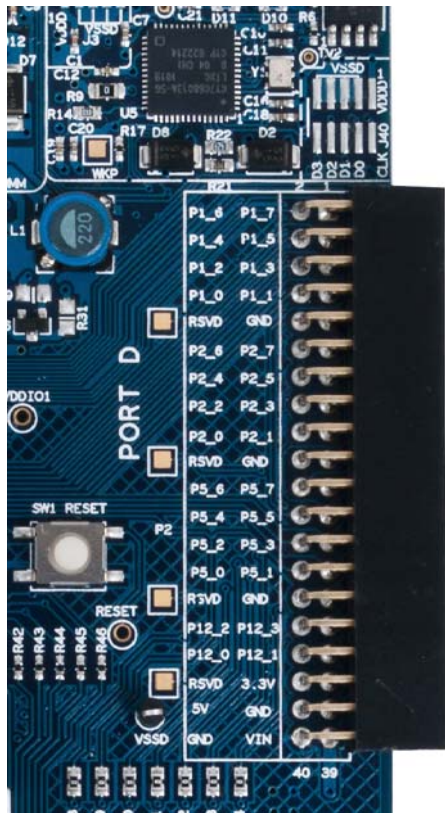
4.2.7.1 *Port D*

This is the miscellaneous port designed to handle CapSense-based application boards and digital application boards. The signal routing to this port adheres to the stringent requirements needed to provide good performance CapSense. This port can also be used for other functions and expansion board kits (EBKs).

This port is not designed for precision analog performance. The pins on the port are functionally compatible to port B of the PSoC Development Kit. Any project made to function on port B of the PSoC Development Kit can be easily ported over to port D on this board. A caveat to this is that there is no opamp available on this port; therefore, opamp-based designs are not recommended for use on this port.

The following figure shows the pin mapping for the port.

Figure 4-10. Port D

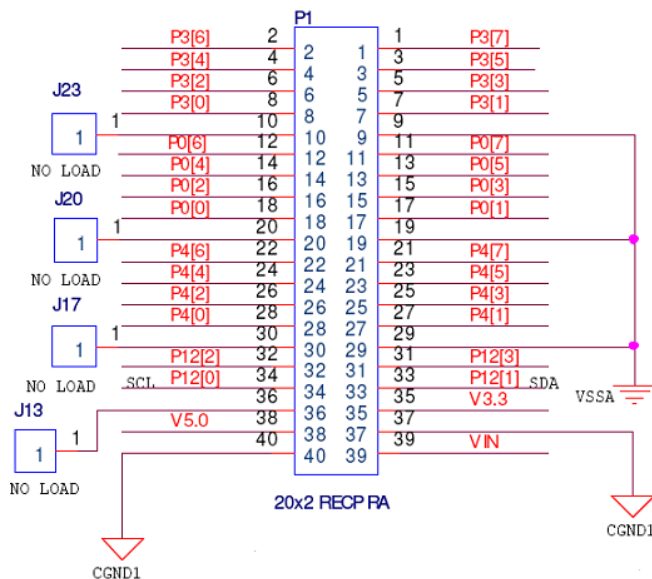
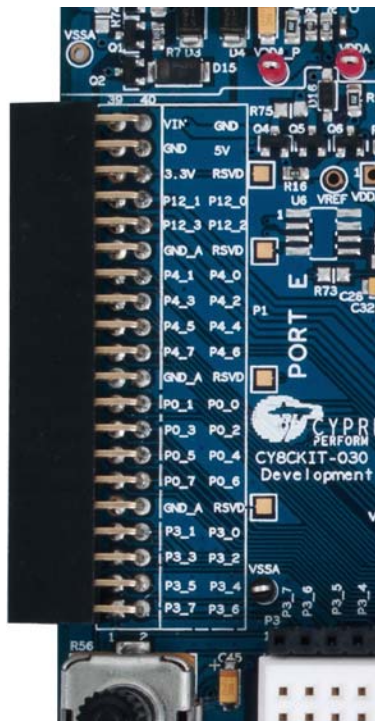


4.2.7.2 Port E

This is the analog port on the kit and has special layout considerations. It also brings out all analog resources such as dedicated opamps to a single connect. Therefore, this port is ideal for precision analog design development. This port is functionally compatible to port A of the PSoC Development Kit and it is easy to port an application developed on port A.

The port has two types of grounds, CGND1 and CGND2. The two grounds are connected to the GND on the board, but are provided for expansion boards designed for analog performance. The expansion boards have an analog and digital ground. The two grounds on this port help to keep it distinct even on this board until it reaches the GND plane.

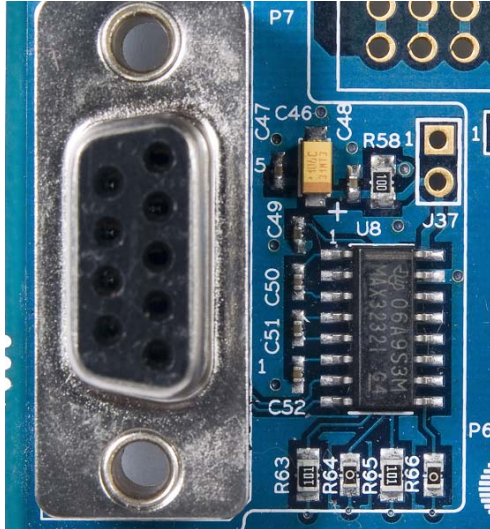
Figure 4-11. Port E



4.2.8 RS-232 Interface

The board has an RS-232 transceiver for designs using RS-232 (UART). The RS-232 section power can be disconnected through a single resistor R58. This is useful for low-power designs.

Figure 4-12. RS-232 Interface

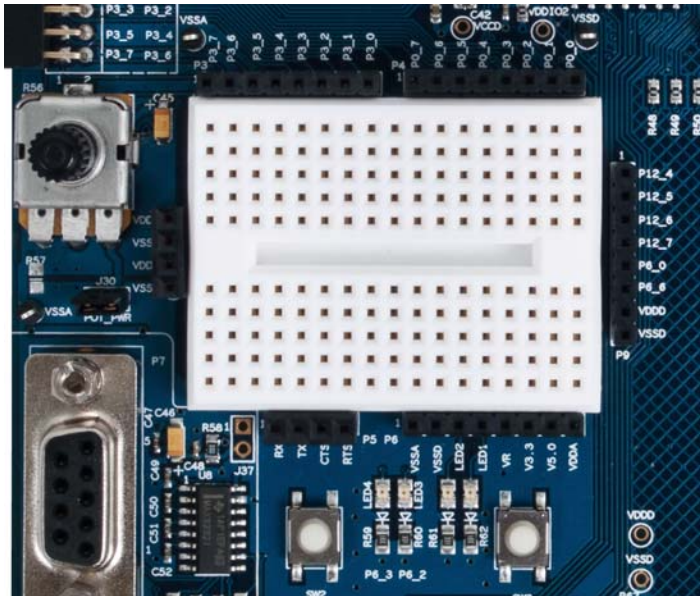


4.2.9 Prototyping Area

The prototyping area on the board has two complete ports of the device for simple custom circuit development. The ports in the area are port 0 and port 3, which bring out the four dedicated opamp pins on the device. Therefore, these ports can be used with the prototyping area to create simple yet elegant analog designs. It also brings SIOs such as port 12[4], port 12[5], port 12[6], and port 12[7] and GPIOs such as port P6[0] and port P6[6]. Power and ground connections are available close to the prototyping space for convenience.

The area also has four LEDs and two switches for applications development. The two switches on the board are hard-wired to port 15[5] and port 6[1]. Two LEDs out of the four are hard-wired to port 6[2] and port 6[3] and the other two are brought out on pads closer to the prototyping area.

Figure 4-13. Prototyping Area



This area also comprises of a potentiometer to be used for analog system development work. The potentiometer connects from V_{dda}, which is a noise-free supply and is hence capable of being used for low-noise analog applications. The potentiometer output is available on P6[5] and VR on header P6 in the prototyping area.

4.2.10 Character LCD

The kit has a character LCD module, which goes into the character LCD header, P8. The LCD runs on a 3.3-V supply and can function regardless of the voltage on which PSoC is powered. A 0-Ω resistor setting is available on the LCD section (R71/R72), making it possible to convert it to a 3.3-V LCD.

CAUTION When the resistor is shifted to support a 5-V LCD module, plugging in a 3.3-V LCD module into the board can damage the LCD module.

Figure 4-14. Pin 1 Indication

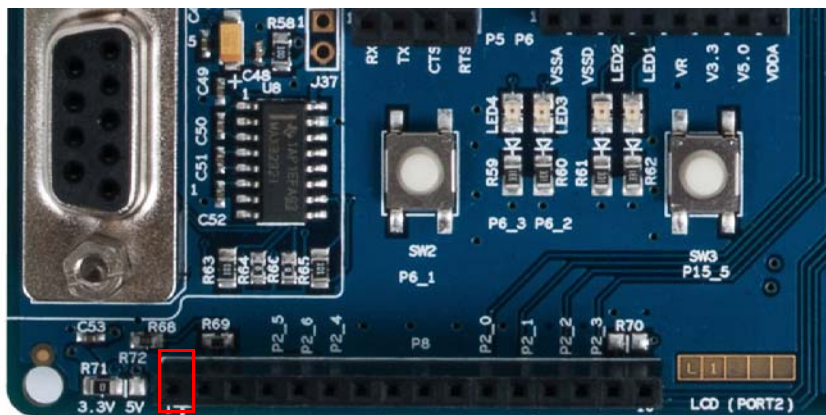
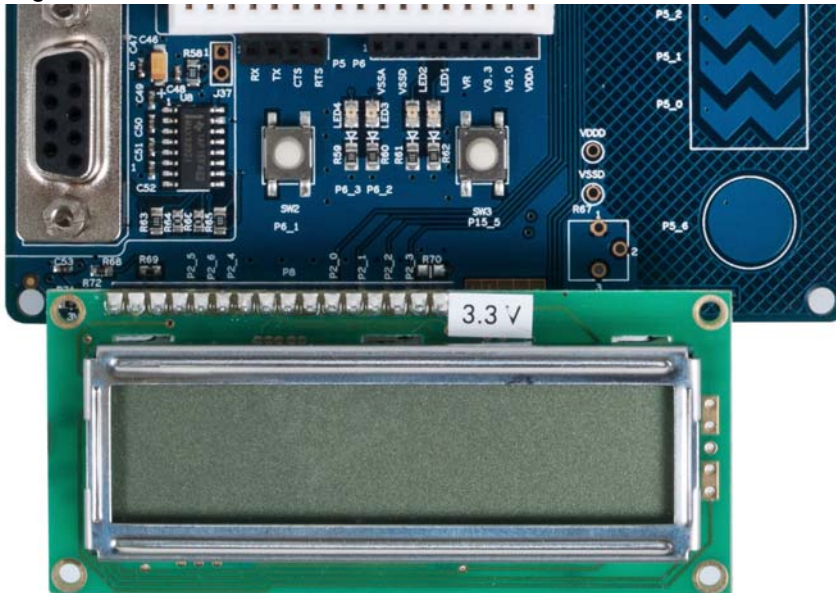


Figure 4-15. LCD Connected on P8 Connector

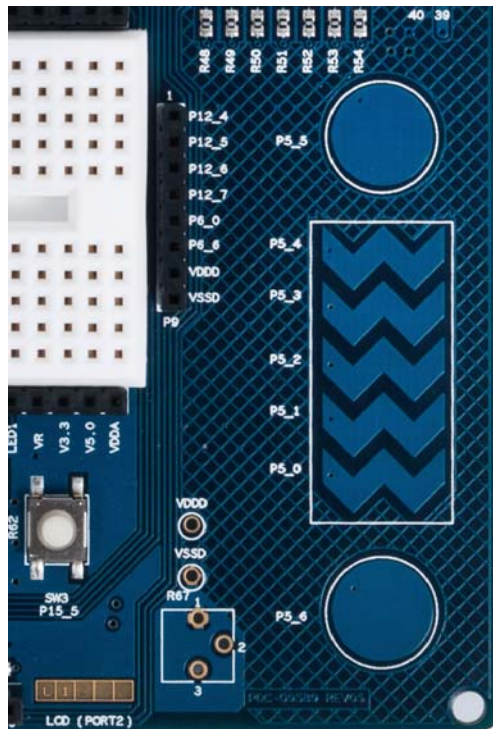


4.2.11 CapSense Sensors

The board layout considers the special requirements for CapSense. It has two CapSense buttons and a five-element CapSense slider. The CapSense buttons are connected to pins P5[6] and P5[5]. The slider elements are connected to pins P5[0:4].

The Cmod (modulation capacitor) is connected to pin P6[4] and an optional Rb (bleeder resistor) is available on P15[4].

Figure 4-16. CapSense Sensors



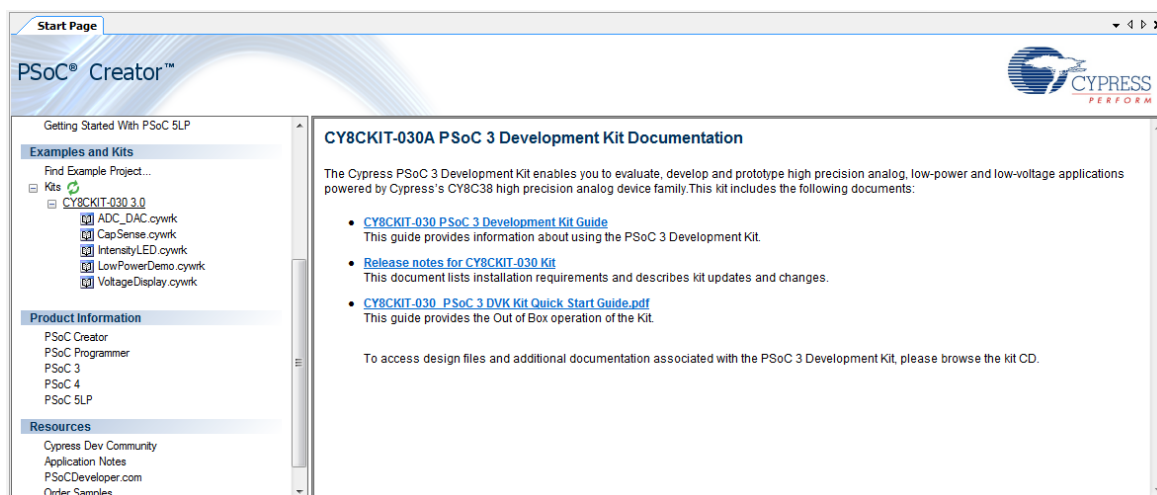
5. Code Examples



5.1 Introduction

To access code examples described in this section, open the PSoC Creator Start Page. For additional code examples, visit <http://www.cypress.com>.

Figure 5-1. PSoC Creator Start Page



5.1.1 Programming the Code Examples

Follow these steps to open and program code examples:

1. In the PSoC Creator start page, go to **Examples and Kits > Kits > CY8CKIT-030 3.0** and click on a code example.
2. Create a folder in the desired location and click **OK**.
3. The project opens in PSoC Creator and is saved to that folder.
4. Build the code example to generate the hex file.
5. To program, connect the board to a computer using the USB cable connected to port J1, as described in [Onboard Programming Interface on page 18](#). The board is detected as DVKProg.
6. Click **Debug > Program**.
7. The programming window opens up. If the silicon is not yet acquired, select the DVKProg and click on the **Port Acquire** button.
8. After the silicon is acquired, it is shown in a tree structure below the DVKProg. Click **Connect**.
9. Click **OK** to exit the window and start programming.
10. Click the **Program** icon to program the board.

5.2 VoltageDisplay

5.2.1 Project Description

This example code measures a simple analog voltage controlled by the potentiometer. The code uses the internal Delta-Sigma ADC configured for a 20-bit operation; the ADC range is 0 to V_{dda}. The voltage measurement resolution is in microvolts. The results are displayed on the character LCD module.

Note The PSoC 3 Development Kit is factory-programmed with the Voltage Display code example.

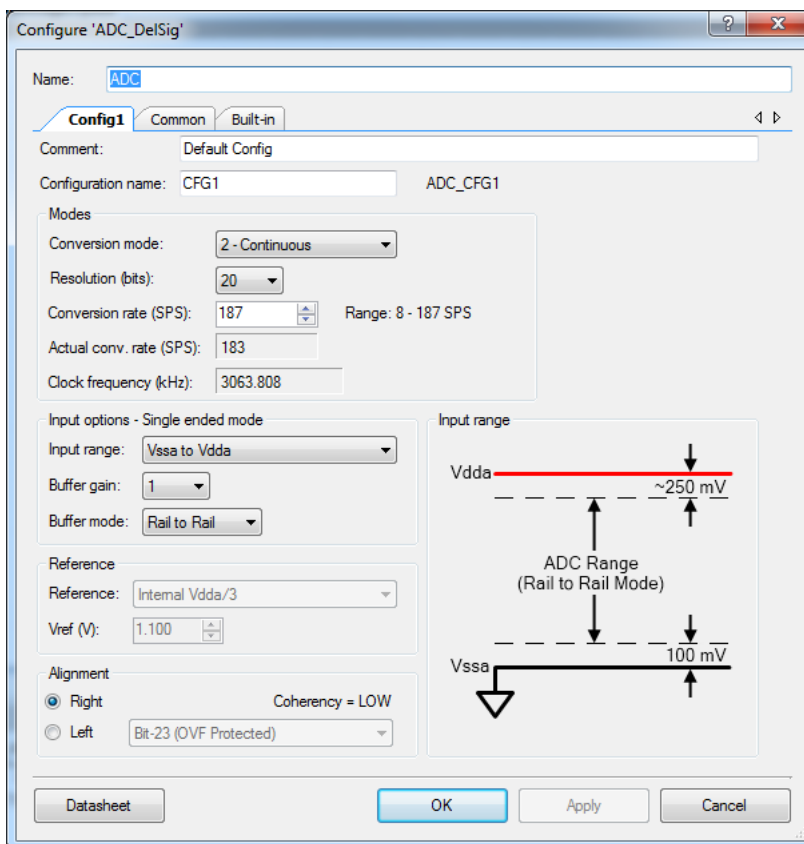
5.2.2 Hardware Connections

The example requires the character LCD on P8. Because it uses the potentiometer, the jumper POT_PWR (J30) should be in place. This connects the potentiometer to the V_{dda}.

5.2.3 DelSig ADC Configuration

To view or configure the DelSig ADC component, double-click the component in the *TopDesign.cysch* file.

Figure 5-2. Delta-Sigma ADC Configuration



The DelSig ADC is configured as follows:

- Continuous mode of operation is selected because the ADC scans only one channel.
- Conversion rate is set to 187 samples/sec, which is the maximum sample rate possible at 20-bit resolution.

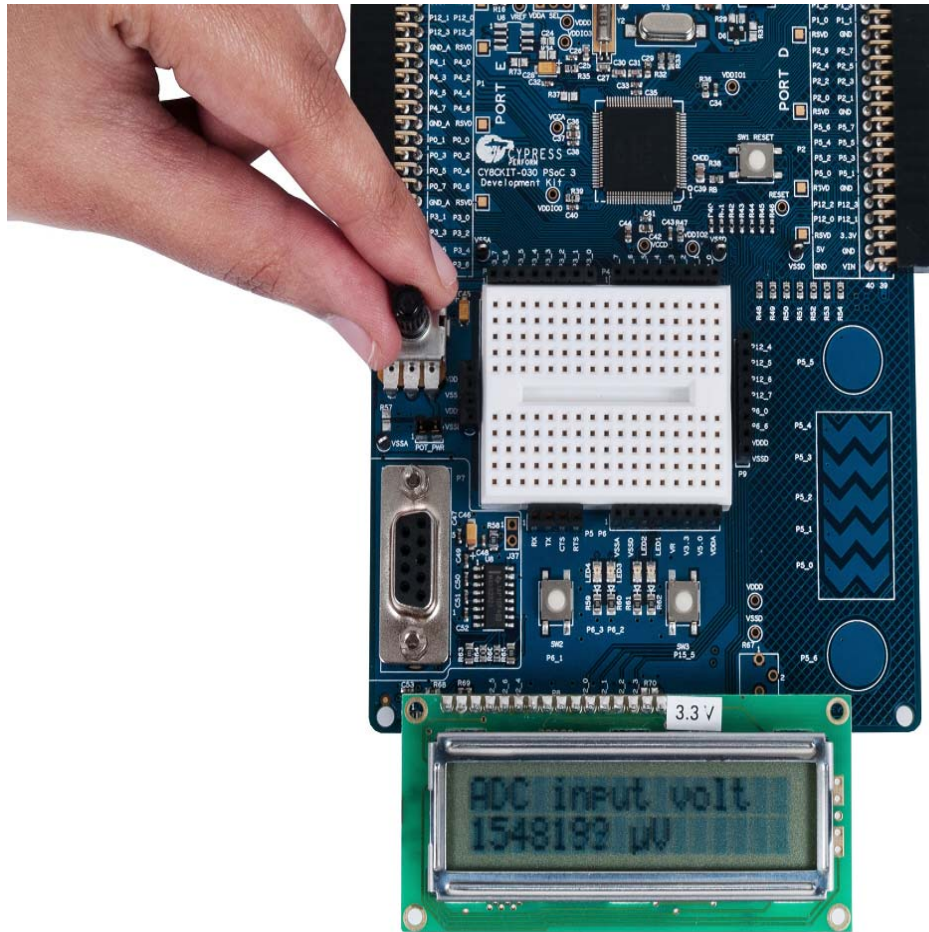
- Range is set to Vssa to Vdda in single-ended mode because the potentiometer output is a single-ended signal that can go from 0 to Vdda. Therefore, at 20-bit resolution, the ADC will resolve in steps of $Vdda/2^{20}$.

5.2.4 Verify Output

Build and program the code example, as explained in [5.1.1 Programming the Code Examples](#), and reset the device. The LCD shows the voltage reading corresponding to the voltage on the potentiometer. [Figure 5-3](#) demonstrates the functionality. When you turn the potentiometer, the voltage value changes. You can also verify the voltage on the potentiometer using a precision multimeter.

Note The potentiometer connects to a differential ADC, which works in single-ended mode. This means the ADC input is measured against internal Vssa. Any offset in the measurement can be positive or negative. This can result in a small offset voltage even when the potentiometer is zero.

Figure 5-3. Voltage Display



5.3 IntensityLED

5.3.1 Project Description

This example code uses a pulse-width modulator (PWM) to illuminate an LED. When the pulse width of the PWM varies, the LED brightness changes. By continuously varying the pulse width of the PWM, the example code makes an LED go from low brightness to a high brightness and back.

5.3.2 Hardware Connections

No hardware connections are required for this project, because all the connections are hard-wired to specific pins on the board.

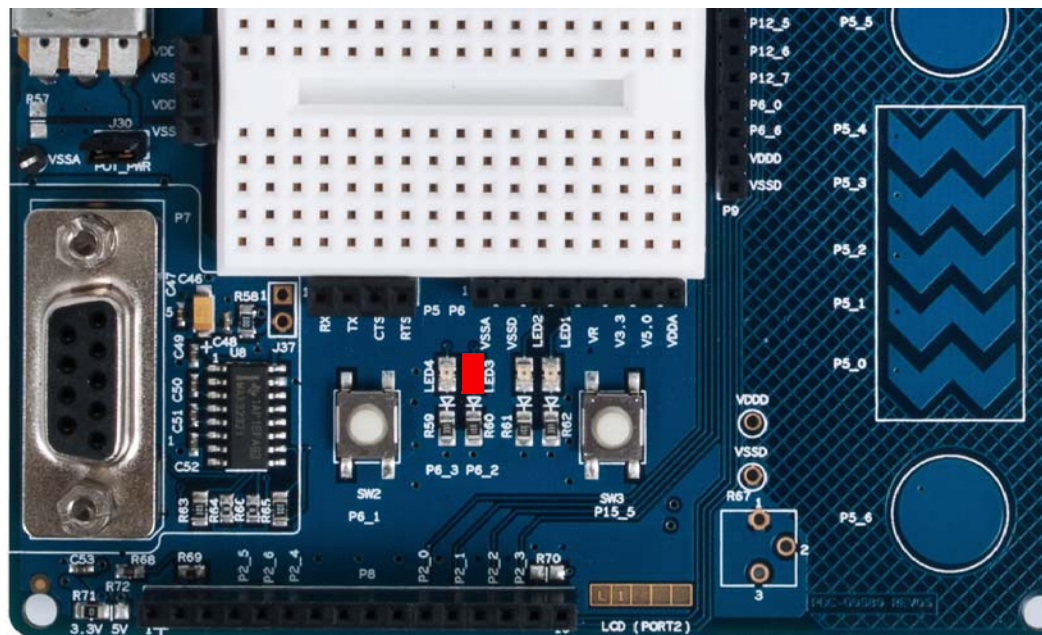
5.3.3 Verify Output

When the example code is built and programmed into the device, reset the device by pressing the **Reset** button or power cycling the board.

The project output is LED3 glowing with a brightness control that changes with time (see [Figure 5-4](#)).

Note If the CY8CKIT-030 is programmed with any other code example involving LCD display before programming the *IntensityLED.hex* file, the LCD continues to display the output of the previous project because the LCD component is not used in the IntensityLED project. The LCD display is cleared by power cycling the board.

Figure 5-4. Verify Output - Code Example



5.4 LowPowerDemo

5.4.1 Project Description

This code example demonstrates the low-power functionality of PSoC 3. The project implements an RTC based code, which goes to sleep and wakes up on the basis of switch inputs.

The RTC uses an accurate 32-kHz clock generated using the external crystal provided on the board. When there is a key press, the device is put to sleep while the RTC is kept active.

5.4.2 Hardware Connections

The project requires a 3.3-V LCD to view the time display. No extra connections are required for project functionality. To make low-power measurements using this project, implement the changes proposed in [Low-Power Functionality on page 18](#).

5.4.3 Verify Output

In normal operation, the project displays the time starting from 00:00:00 and LED3 is in On state. When you press the SW2 button, the device is put to sleep and LED3 is in Off state. If an ammeter is connected to measure the system current (see [Low-Power Functionality on page 18](#) for details), a system current of less than 2 μA is displayed.

The device wakes up when SW2 is pressed again and displays the time on the LCD. The following figures show the output display.

Figure 5-5. PSoC 3 in Active Mode

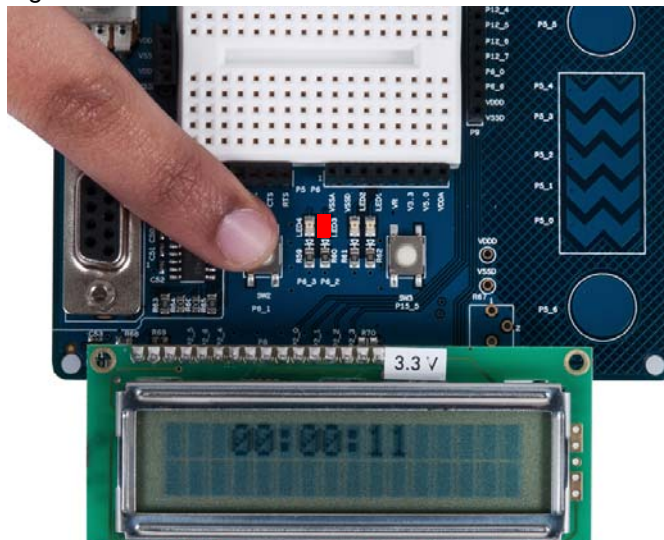
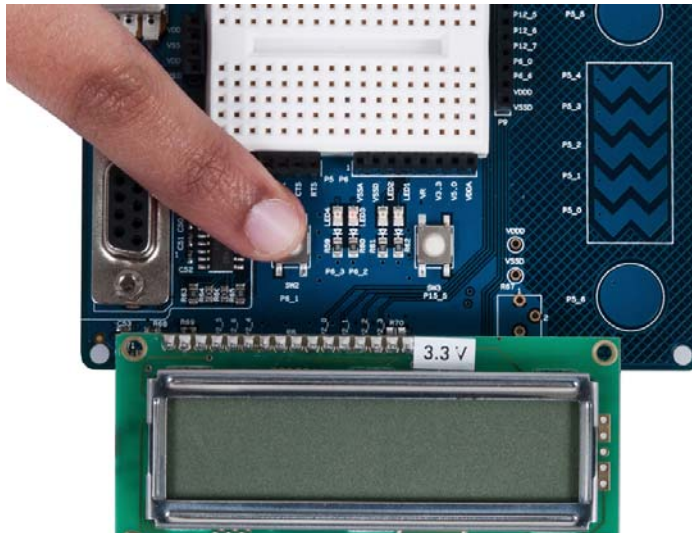


Figure 5-6. PSoC 3 in Sleep Mode



5.5 CapSense Example

5.5.1 Project Description

This code example provides a platform to build CapSense-based projects using PSoC 3. The example uses two CapSense buttons and one five-element slider provided on the board. Each capacitive sensor on the board is scanned using the Cypress CSD algorithm. The buttons are pre-tuned in the example code to take care of factors such as board parasitic.

5.5.2 Hardware Connections

This project uses the LCD for display; therefore, ensure that it is plugged into the port. No specific hardware connections are required for this project because all connections are hard-wired on the board.

5.5.3 Verify Output

Build and program the code example, and reset the device. The LCD displays the status of the two buttons as On/Off. The LCD also shows the slider touch position as a percentage. When you touch either of the buttons, the corresponding button's state changes on the LCD. When you touch the slider, the corresponding finger position is displayed as a percentage on the LCD.

Figure 5-7. CapSense Slider

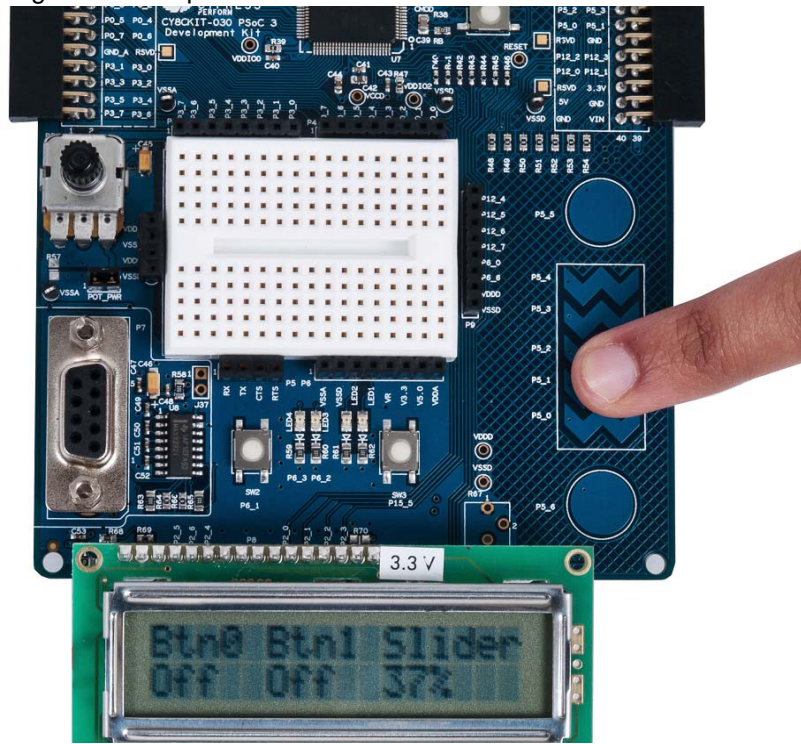
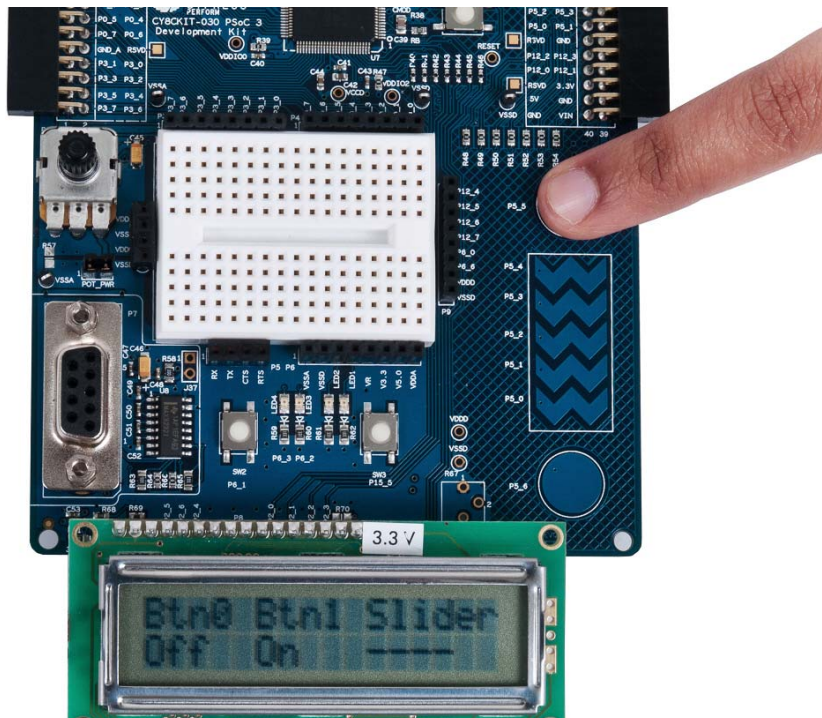


Figure 5-8. CapSense Button



5.6 ADC_DAC Example

5.6.1 Project Description

This project demonstrates sine wave generation by using an 8-bit DAC and DMA. The sine wave period is based on the current value of the ADC value of the potentiometer.

The firmware reads the voltage output by the board potentiometer and displays the raw counts on the board character LCD display. An 8-bit DAC outputs a table generated sine wave to an LED using DMA at a frequency proportional to the ADC count.

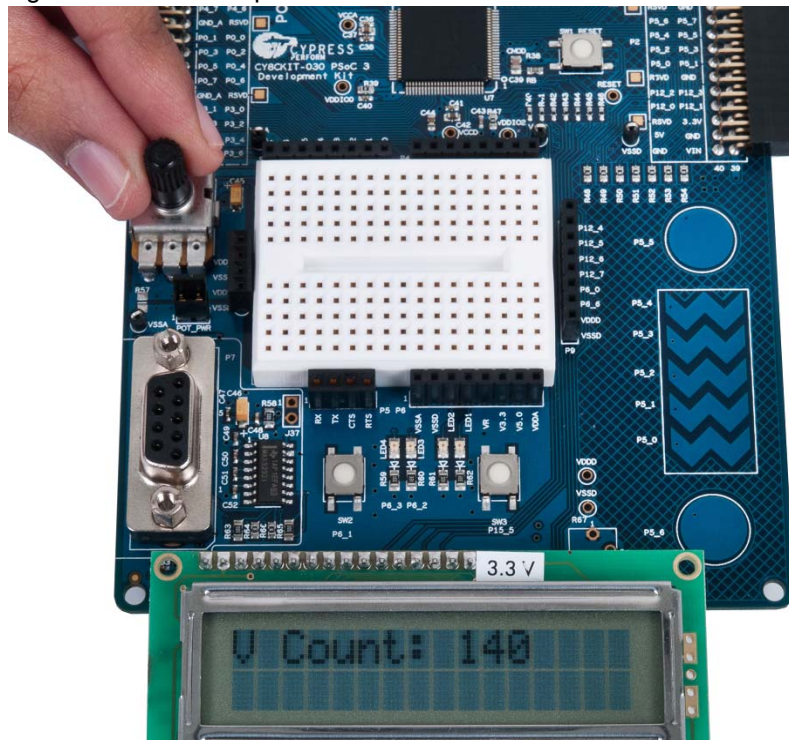
5.6.2 Hardware Connections

For this example, the character LCD must be installed on P8. The example uses the potentiometer; therefore, the jumper POT_PWR (J30) should also be in place. This jumper connects the potentiometer to the Vdda.

5.6.3 Verify Output

Build, program the device, and press the **Reset** button on the PSoC 3 Development Kit to see the ADC output displayed on the LCD. LED4 is an AC signal output whose period is based on the ADC. Turning the potentiometer results in LCD value change. This also results in change in the period of the sine wave fed into LED4, which can also be observed.

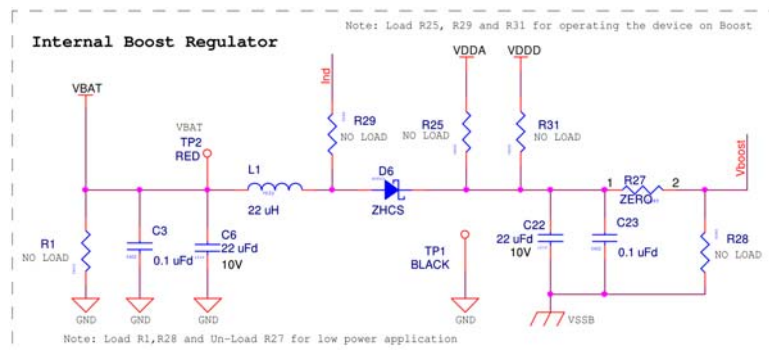
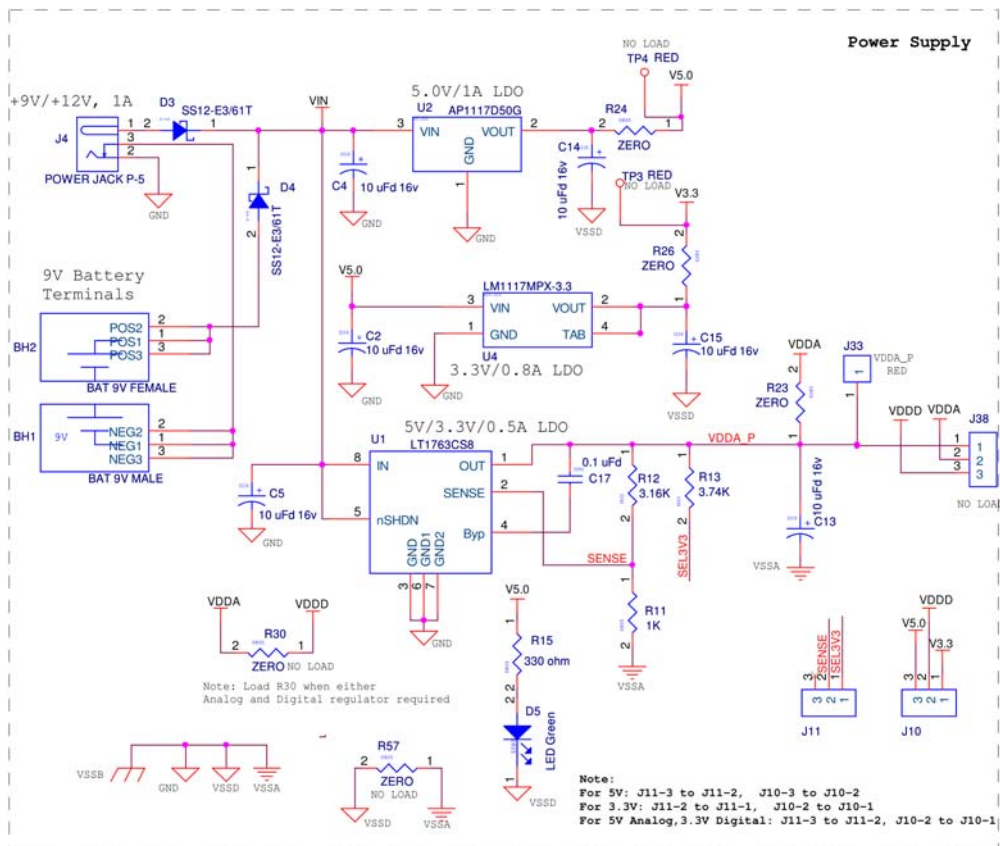
Figure 5-9. ADC Output

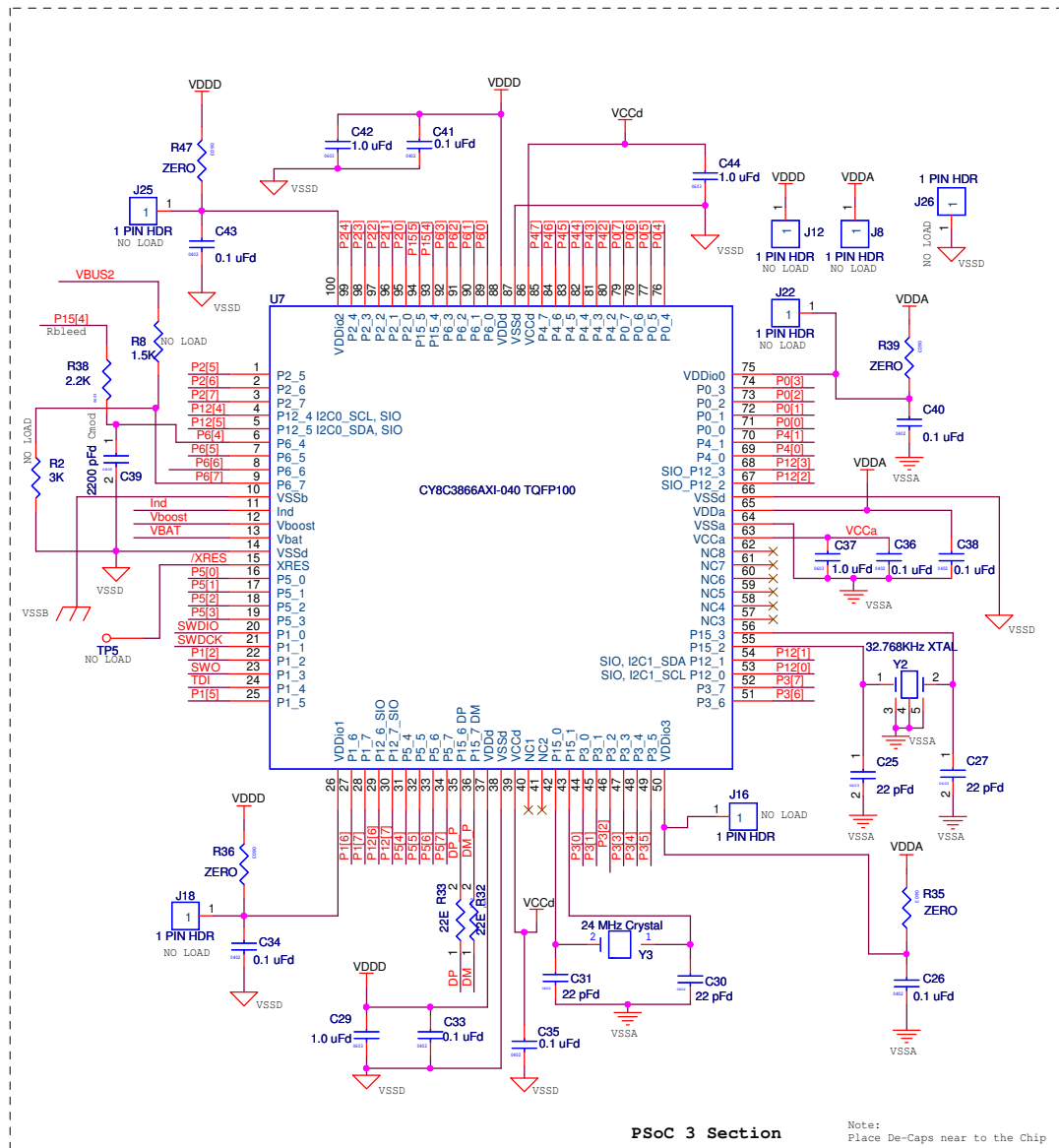


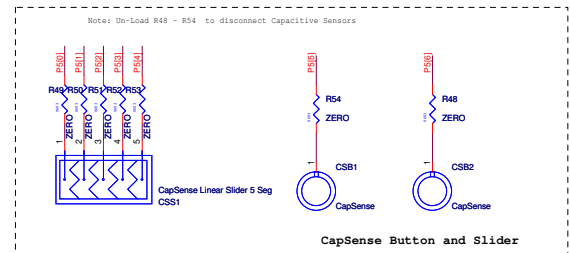
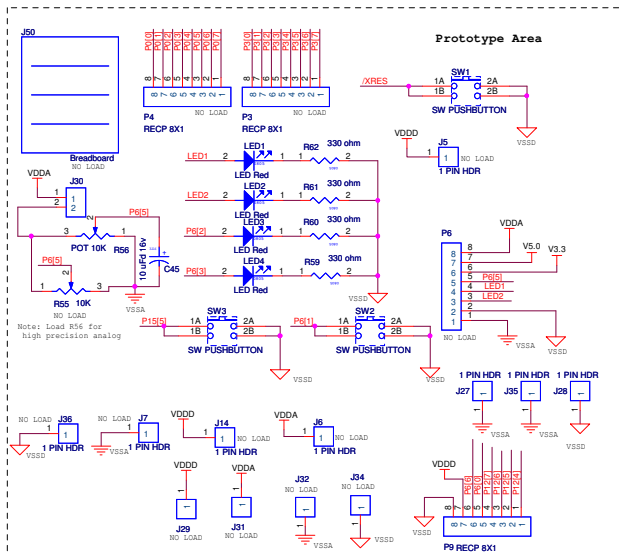
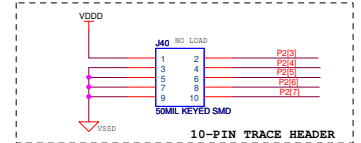
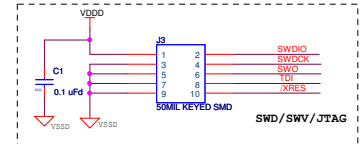
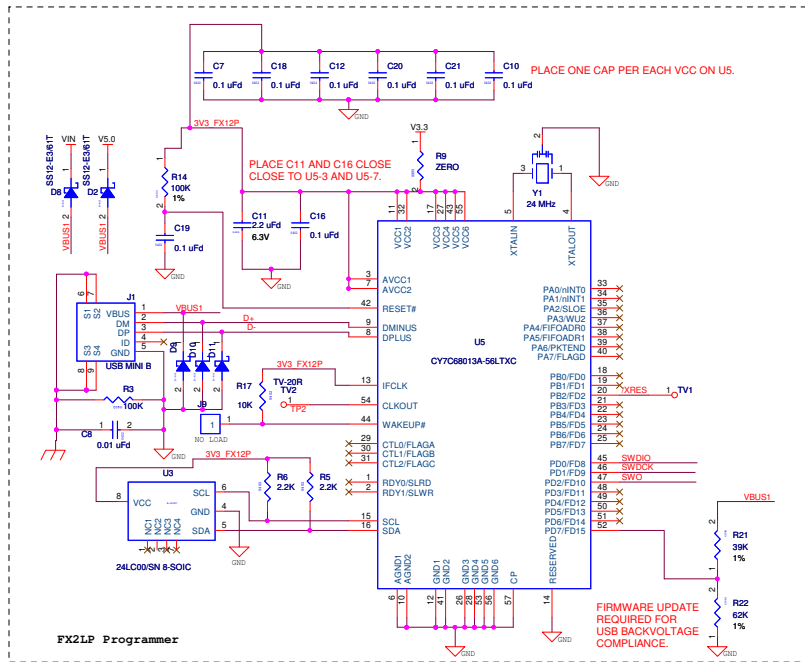
A. Appendix

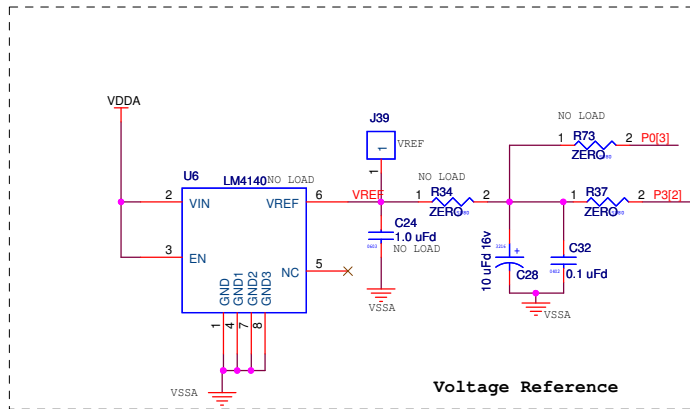
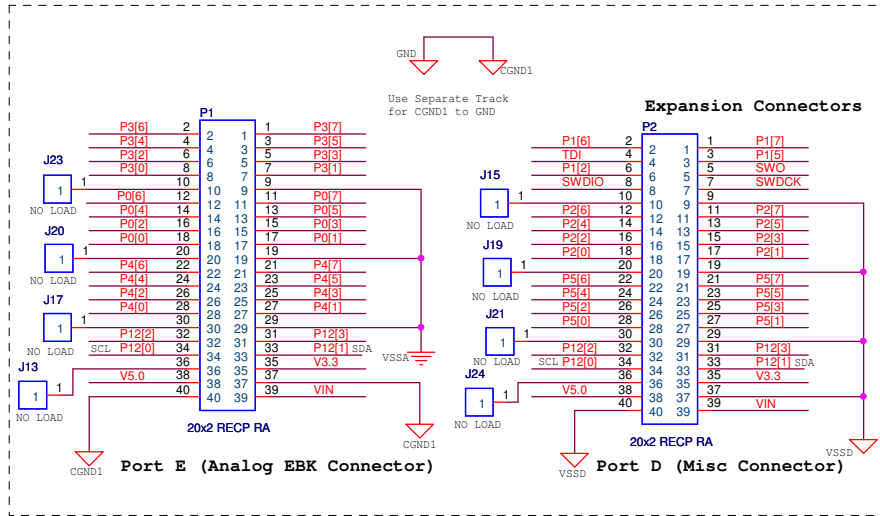


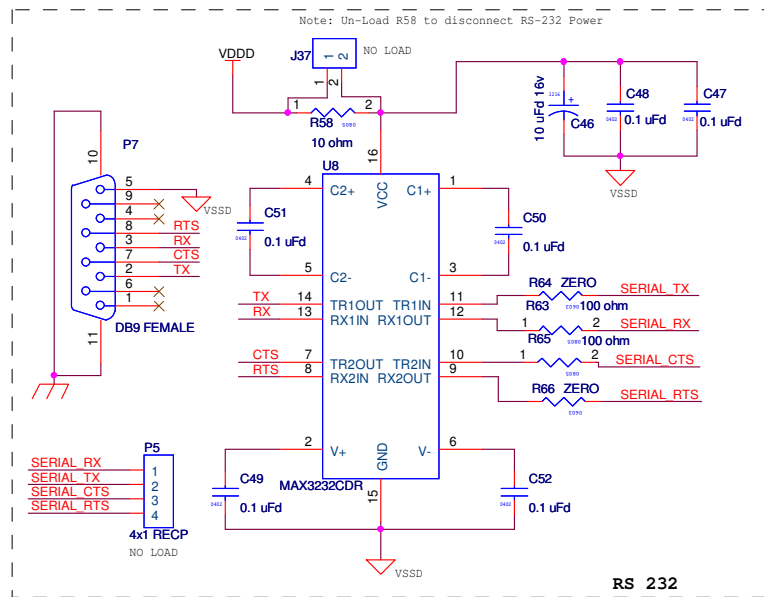
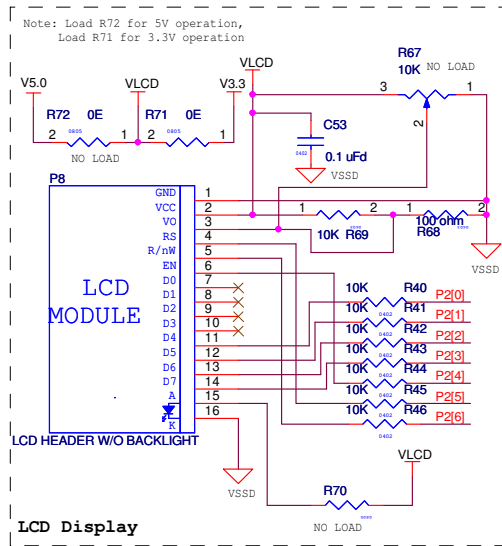
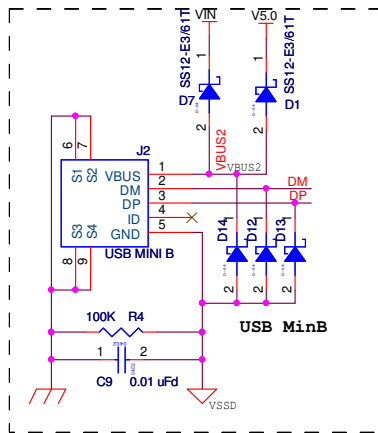
A.1 Schematics





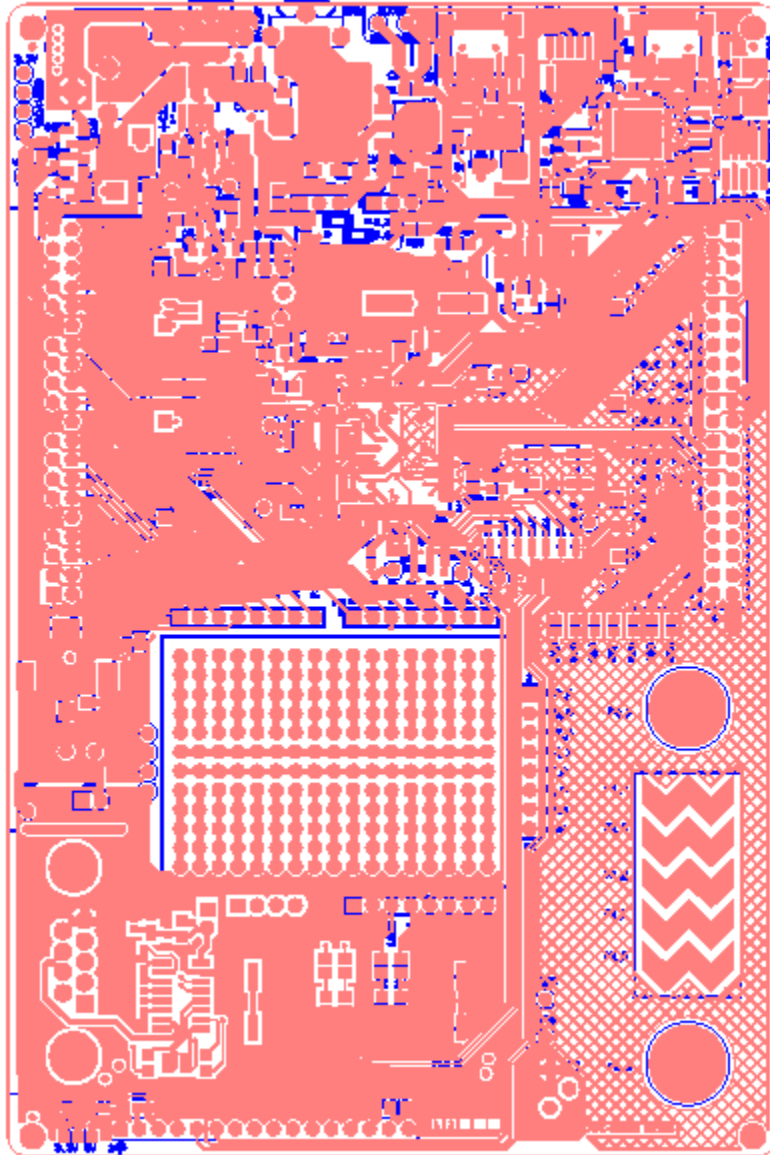




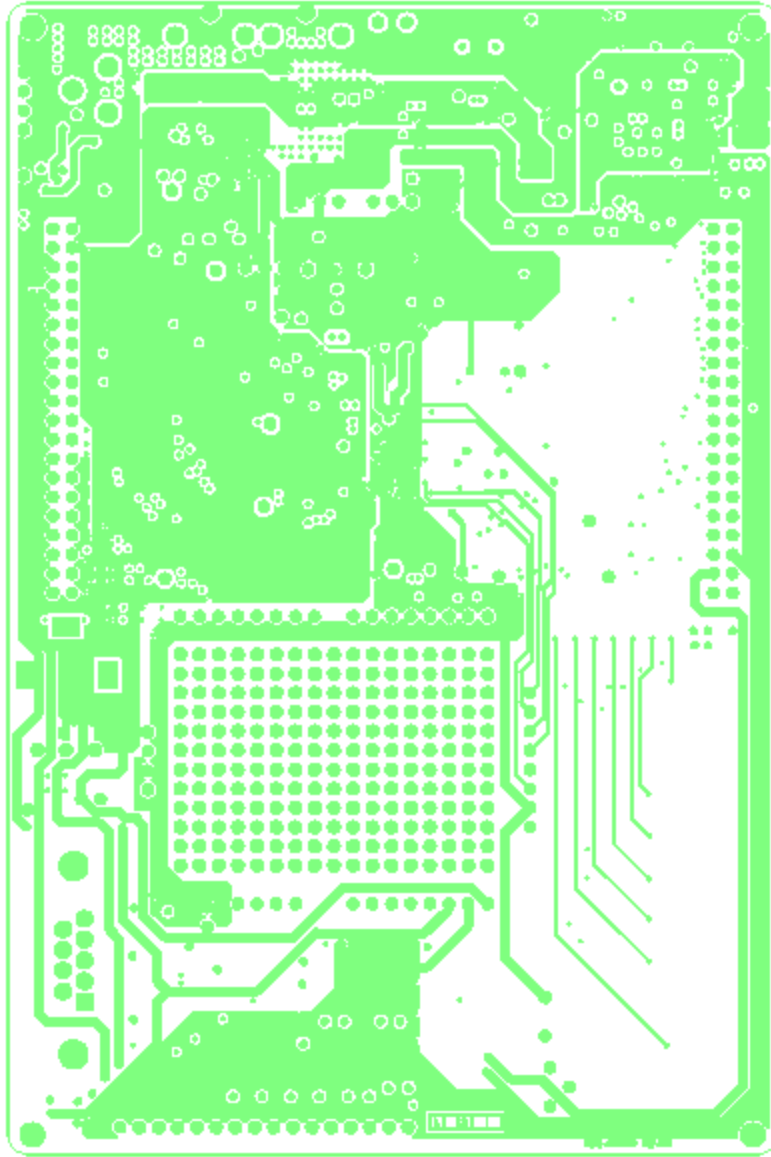


A.2 Board Layout

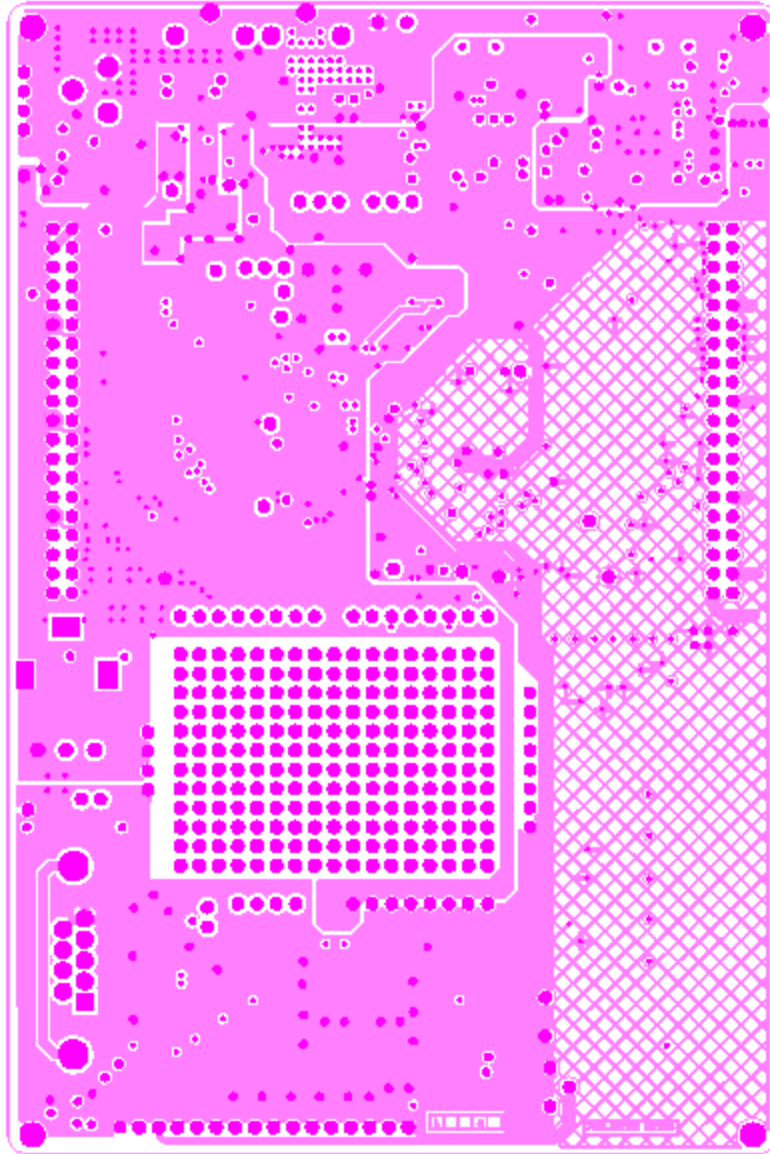
A.2.1 PDC-09589 Top



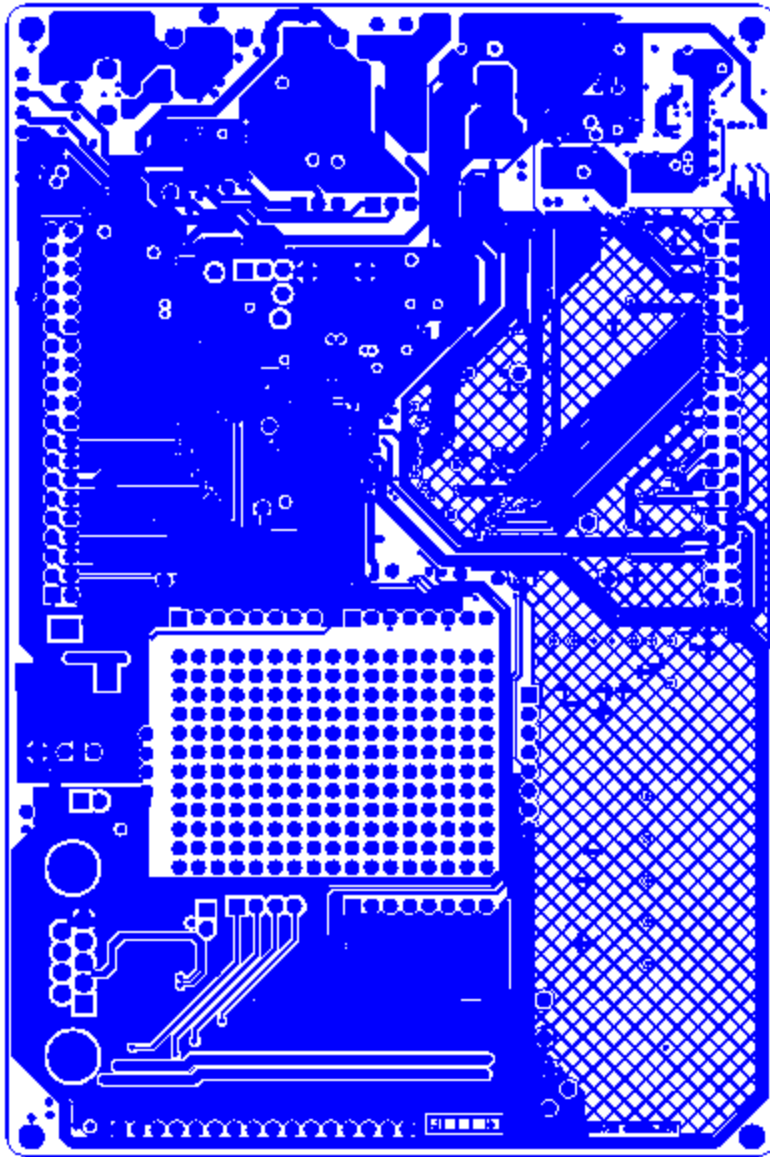
A.2.2 PDC-09589 Power



A.2.3 PDC-09589 Ground



A.2.4 PDC-09589 Bottom



A.3 Bill of Materials (BOM)

| Item | Qty | Reference | Value | Description | Manufacturer | Mfr Part Number |
|------|-----|---|---------------------|---|---------------------------------|------------------------|
| 1 | 1 | BH1 | BAT 9V MALE | BATTERY HOLDER 9V Male PC MT | Keystone Electronics | 593 |
| 2 | 1 | BH2 | BAT 9V FEMALE | BATTERY HOLDER 9V Female PC MT | Keystone Electronics | 594 |
| 3 | 9 | C2,C4,C5,C13,C14, C15,C28,C45,C46 | 10 uFd 16v | CAP 10UF 16V TANTALUM 10% 3216 | AVX | TAJA106K016R |
| 4 | 2 | C6,C22 | 22 uFd | CAP CER 22UF 10V 10% X5R 1210 | Kemet | C1210C226K8PACT U |
| 5 | 29 | C7,C10,C12,C16,C 17,C18,C19,C20,C2 1,C26,C32,C33,C34 ,C35,C36,C38,C40, C41,C43,C47,C48, C49,C50,C51,C52, C53, C1, C3, C23 | 0.1 uFd | CAP .1UF 16V CERAMIC Y5V 0402 | Panasonic - ECG | ECJ-0EF1C104Z |
| 6 | 2 | C8,C9 | 0.01 uFd | CAP 10000PF 16V CERAMIC 0402 SMD | Panasonic - ECG | ECJ-0EB1C103K |
| 7 | 1 | C11 | 2.2 uFd | CAP CER 2.2UF 6.3V 20% X5R 0402 | Panasonic - ECG | ECJ-0EB0J225M |
| 8 | 4 | C29,C37,C42,C44 | 1.0 uFd | CAP CERAMIC 1.0UF 25V X5R 0603 10% | Taiyo Yuden | TMK107BJ105KA-T |
| 9 | 4 | C30,C31,C25, C27 | 22pF | CAP, CER, 22 pF, 50V, 5%, COG, 0603, SMD | Panasonic - ECG | ECJ-0EC1H220J |
| 10 | 1 | C39 | 2200 pFd | SMD/SMT 0805 2200pF 50volts COG 5% | Murata | GRM2165C1H222JA 01D |
| 11 | 6 | D1,D2,D3,D4, D7, D8 | SS12-E3/61T | DIODE SCHOTTKY 20V 1A SMA | Vishay/General Semiconductor | SS12-E3/61T |
| 12 | 1 | D5 | LED Green | LED GREEN CLEAR 0805 SMD | Chicago Miniature | CMD17-21VGC/TR8 |
| 13 | 1 | D6 | ZHCS | DIODE SCHOTTKY 40V 1.0A SOT23-3 | Zetex | ZHCS1000TA |
| 14 | 6 | D9, D10, D11, D12, D13, D14 | ESD diode | SUPPRESSOR ESD 5VDC 0603 SMD | Bourns Inc. | CG0603MLC-05LE |
| 15 | 2 | J1,J2 | USB MINI B | CONN USB MINI B SMT RIGHT ANGLE | TYCO | 1734035-2 |
| 16 | 1 | D15 | 4.3V Zener Diode | DIODE ZENER 4.3V 1W SOD-106 | Rohm Semiconductor | PTZTE254.3B |
| 17 | 1 | D16 | 2.0V Zener Diode | DIODE ZENER 2V 500MW SOD-123 | Diodes Inc | BZT52C2V0-7-F |
| 18 | 1 | J3 | 50MIL KEYED SMD | CONN HEADER 10 PIN 50MIL KEYED SMD | Samtec | FTSH-105-01-L-DV- K |
| 19 | 1 | J4 | POWER JACK P-5 | CONN JACK POWER 2.1mm PCB RA | CUI | PJ-102A |
| 20 | 1 | J50 | Breadboard | BREADBOARD 17x5x2 | 3M | 923273-I |

| Item | Qty | Reference | Value | Description | Manufacturer | Mfr Part Number |
|------|-----|----------------------------------|---|------------------------------------|---------------------------|-----------------------|
| 21 | 5 | TP1, J26, J27, J35, J28 | BLACK TEST POINT | TEST POINT PC MINI .040"D Black | Keystone Electronics | 5001 |
| 22 | 4 | LED1,LED2,LED3,LED4 | LED Red | LED RED CLEAR 0805 SMD | Rohm Semiconductor | SML-210LTT86 |
| 23 | 1 | L1 | 22 uH | INDUCTOR SHIELD PWR 22UH 7032 | TDK Corporation | SLF7032T-220MR96-2-PF |
| 24 | 2 | P1,P2 | 20x2 RECP RA | CONN FEMALE 40POS DL .100 R/A GOLD | Sullins Electronics Corp. | PPPC202LJBN-RC |
| 25 | 1 | P7 | DB9 FEMALE | CONN DB9 FEMALE VERT PRESSFIT SLD | Norcomp Inc. | 191-009-223R001 |
| 26 | 1 | P8 | LCD HEADER W/O BACKLIGHT | CONN RECEPT 16POS .100 VERT AU | Tyco Electronics | 1-534237-4 |
| 27 | 4 | P3,P4,P6,P9 | RECP 8X1 | CONN RECT 8POS .100 VERT | 3M | 929850-01-08-RA |
| 28 | 6 | Q1,Q2,Q3,Q4,Q5,Q6 | P-MOS, 30V 3.8A SOT23 in Protection circuit | MOSFET P-CH 30V 3.8A SOT23-3 | Diodes Inc | DMP3098L-7 |
| 29 | 1 | R7 | RES 220 OHM 1/10W 1% 0603 SMD | Panasonic - ECG | ERJ-3EKF2200V | ERJ-3EKF2200V |
| 30 | 1 | R16 | RES 442 OHM 1/10W 1% 0603 SMD | Panasonic - ECG | ERJ-3EKF4420V | ERJ-3EKF4420V |
| 31 | 2 | R3,R4 | 100K | RES 100K OHM 1/16W 5% 0402 SMD | Panasonic - ECG | ERJ-2GEJ104X |
| 32 | 6 | R9,R23,R24,R26,R27,R71 | ZERO | RES 0.0 OHM 1/10W 5% 0805 SMD | Panasonic-ECG | ERJ-6GEY0R00V |
| 33 | 2 | R5,R6 | 2.2K | RES 2.2K OHM 1/16W 5% 0402 SMD | Panasonic - ECG | ERJ-2GEJ222X |
| 34 | 3 | R11,R10,R18 | 1K | RES 1.0K OHM 1/8W 5% 0805 SMD | Panasonic - ECG | ERJ-6GEYJ102V |
| 35 | 1 | R12 | 3.16K | RES 3.16K OHM 1/10W .5% 0603 SMD | Yageo | RT0603DRD073K16L |
| 36 | 1 | R13 | 3.74K | RES 3.74K OHM 1/10W 1% 0603 SMD | Panasonic - ECG | ERJ-3EKF3741V |
| 37 | 1 | R14 | 100K | RES 100K OHM 1/10W 1% 0603 SMD | Yageo | RC0603FR-07100KL |
| 38 | 5 | R15,R59,R60,R61,R62 | 330 ohm | RES 330 OHM 1/10W 5% 0805 SMD | Panasonic - ECG | ERJ-6GEYJ331V |
| 39 | 8 | R17,R40,R41,R42,R43,R44,R45, R46 | 10K | RES 10K OHM 1/16W 5% 0402 SMD | Stackpole Electronics Inc | RMCF 1/16S 10K 5% R |

| Item | Qty | Reference | Value | Description | Manufacturer | Mfr Part Number |
|------|-----|---|-----------------------------|--|--------------------------------|--------------------------|
| 40 | 13 | R35,R36,R39,R47, R48,R49,R50, R51,R52,R53,R54, R64,R66 | ZERO | RES ZERO OHM 1/16W 5% 0603 SMD | Panasonic - ECG | ERJ-3GEY0R00V |
| 41 | 2 | R32,R33 | 22E | RES 22 OHM 1/16W 1% 0603 SMD | Panasonic - ECG | ERJ-3EKF22R0V |
| 42 | 2 | R63,R65 | 100 ohm | RES 100 OHM 1/8W 5% 0805 SMD | Rohm | MCR10EZJH101 |
| 43 | 1 | R56 | POT 10K | POT 10K OHM 1/8W CARB VERTICAL | CTS Electrocomponents | 296UD103B1N |
| 44 | 1 | R58 | 10E | RES 10 OHM 1/8W 5% 0805 SMD | Stackpole Electronics Inc | RMCF 1/10 10 5% R |
| 45 | 1 | R68 | 100 ohm | RES 100 OHM 1/16W 5% 0603 SMD | Panasonic - ECG | ERJ-3GEYJ101V |
| 46 | 1 | R69 | 10K | RES 10K OHM 1/16W 5% 0603 SMD | Panasonic - ECG | ERJ-3GEYJ103V |
| 47 | 3 | SW1,SW2,SW3 | SW PUSHBUTTON | LT SWITCH 6MM 160GF H=2.5MM SMD | Panasonic - ECG | EVQ-Q2P02W |
| 48 | 1 | U1 | LT1763CS8 | IC LDO REG LOW NOISE ADJ 8-SOIC | Linear Technology | LT1763CS8#PBF |
| 49 | 1 | U2 | AP1117D50G | IC REG LDO 1.0A 5.0V TO- 252 | Diodes Inc | AP1117D50G-13 |
| 50 | 1 | U3 | 24LC00/SN | IC EEPROM 128BIT 400KHZ 8SOIC | Microchip Technology | 24LC00/SN |
| 51 | 1 | U4 | LM1117MPX- 3.3 | IC REG 3.3V 800MA LDO SOT-223 | National Semiconductor | LM1117IMP-3.3/ NOPB |
| 52 | 1 | U5 | CY7C68013A- 56LTXC | IC, FX2 HIGH-SPEED USB PERIPHERAL CONTROLLER QFN56 | Cypress Semiconductor | CY7C68013A- 56LTXC |
| 53 | 1 | U7 | CY8C3866AXI- 040 TQFP100 | PSoC3 Mixed-Signal Array | Cypress Semiconductor | CY8C3866AXI-040 |
| 54 | 1 | U8 | MAX3232CDR | IC 3-5.5V LINE DRVR/ RCVR 16-SOIC | Texas Instrumts | MAX3232IDR |
| 55 | 1 | Y1 | 24 MHz | CER RESONATOR 24.0 MHz SMD | Murata | CSTCW24M0X53-R0 |
| 56 | 1 | Y2 | 32.768KHz XTAL | CRYSTAL 32.768 KHZ CYL 12.5PF CFS308 | Citizen America Corporation | CFS308- 32.768KDZF-UB |
| 57 | 1 | Y3 | 24 MHz Crystal | CRYSTAL 24.000MHZ 20PF SMD | ECS Inc | ECS-240-20-5PX-TR |
| 58 | 3 | J8,J33, TP2 | RED TEST POINT | TEST POINT PC MINI .040"D RED | Keystone Electronics | 5000 |
| 59 | 1 | R38 | 2.2K | RES 2.2KOHM 1/16W 2700PPM 5%0603 | Panasonic - ECG | ERA-V27J222V |
| 60 | 2 | J10,J11 | 3p_jumper | CONN HEADER VERT SGL 3POS GOLD | 3M | 961103-6404-AR |

| Item | Qty | Reference | Value | Description | Manufacturer | Mfr Part Number |
|---------------------------|-----|--|---|--|---------------------------|---------------------|
| 61 | 1 | J30 | 2p_jumper | CONN HEADER VERT SGL 2POS GOLD | 3M | 961102-6404-AR |
| 62 | 1 | NA | 3.3V LCD Module 16POS w/16 pin header installed | 3.3V LCD Module 16POS w/ 16 pin header installed | Lumex | LCM-S01602DTR/A-3 |
| 63 | 1 | NA | 16 pin header | CONN HEADER VERT SGL 16POS GOLD | 3M | 961116-6404-AR |
| 64 | 1 | R21 | 39K | RES 39.0K OHM 1/10W 1% 0603 SMD | Rohm Semiconductor | MCR03EZPFX3902 |
| 65 | 1 | R22 | 62K | RES 62.0K OHM 1/10W 1% 0603 SMD | Rohm Semiconductor | MCR03EZPFX6202 |
| 66 | 1 | P5 | 4x1 RECP | CONN RECEPT 4POS .100 VERT GOLD | 3M | 929850-01-04-RA |
| 67 | 1 | J31, J32, J29, J34 | 4x1 RECP | CONN RECEPT 4POS .100 VERT GOLD | 3M | 929850-01-04-RA |
| No Load Components | | | | | | |
| 68 | 1 | C24 | 1.0 uFd | CAP CERAMIC 1.0UF 25V X5R 0603 10% | Taiyo Yuden | TMK107BJ105KA-T |
| 69 | 11 | J5,J6,J12,J14,J18,J22,J25,TP3,TP4,J16,J39 | RED | TEST POINT PC MINI .040"D RED | Keystone Electronics | 5000 |
| 70 | 2 | J7,J36 | BLACK | TEST POINT PC MINI .040"D Black | Keystone Electronics | 5001 |
| 71 | 1 | TP5 | WHITE | TEST POINT PC MINI .040"D WHITE | Keystone Electronics | 5002 |
| 72 | 1 | R67 | 10K | POT 10K OHM 1/4" SQ CERM SL ST | Bourns Inc. | 3362P-1-103LF |
| 73 | 12 | R30,R34,R57,R72,R25,R31,R70,R37,R29, R73,R74,R75 | ZERO | RES 0.0 OHM 1/10W 5% 0805 SMD | Panasonic-ECG | ERJ-6GEY0R00V |
| 74 | 1 | R55 | 10K | TRIMPOT 10K OHM 4MM TOP ADJ SMD | Bourns Inc. | 3214W-1-103E |
| 75 | 2 | R1,R28, | ZERO | RES ZERO OHM 1/10W 5% 0603 SMD | Panasonic - ECG | ERJ-3GEY0R00V |
| 76 | 1 | U6 | LM4140 | IC REF PREC VOLT MICROPWR 8-SOIC | National Semiconductor | LM4140ACM-1.0/ NOPB |
| 77 | 1 | R8 | 1.5K | RES 1.5KOHM 1/10W 1500PPM 5%0805 | Panasonic - ECG | ERA-S15J152V |
| 78 | 1 | R2 | 3K | RES 1/10W 3K OHM 0.1% 0805 | Stackpole Electronics Inc | RNC 20 T9 3K 0.1% R |
| 79 | 1 | J38 | 3p_jumper | CONN HEADER VERT SGL 3POS GOLD | 3M | 961103-6404-AR |
| 80 | 1 | J37 | 2p_jumper | CONN HEADER VERT SGL 2POS GOLD | 3M | 961102-6404-AR |

| Item | Qty | Reference | Value | Description | Manufacturer | Mfr Part Number |
|---|-----|--|---|---|-------------------|--------------------|
| 81 | 1 | J40 | 50MIL KEYED SMD | CONN HEADER 10 PIN 50MIL KEYED SMD | Samtec | FTSH-105-01-L-DV-K |
| 82 | 2 | CSB1,CSB2 | CapSense | CapSense Button | Cypress | |
| 83 | 1 | CSS1 | CapSense Linear Slider 5 Seg | CapSense Slider | Cypress | |
| 84 | 11 | J9,J13,J15,J17,J19,J20,J21,J23,J24,J41,J42 | PADS | PADS | | |
| 85 | 2 | TV1,TV2 | PADS | PADS | | |
| Install On Bottom of PCB As Close To Corners As Possible | | | | | | |
| 86 | 5 | | | BUMPER CLEAR .500X.23" SQUARE | Richco Plastic Co | RBS-3R |
| Special Jumper Installation Instructions | | | | | | |
| 87 | 1 | J30 | Install jumper across pins 1 and 2 | Rectangular Connectors MINI JUMPER GF 13.5 CLOSE TYPE BLACK | Kobiconn | 151-8030-E |
| 88 | 2 | J10, J11 | Install jumper across pins 1 and 2 | Rectangular Connectors MINI JUMPER GF 13.5 CLOSE TYPE BLACK | Kobiconn | 151-8030-E |
| External Assembly | | | | | | |
| 89 | 1 | | Install 3.3V label as per assembly spec | 3.3V label | | |
| 90 | 2 | | 4-40 X 5 +13 Brass Spacer Stud with Nut | Spacer and nut for RS232 Connector P7 | | |

A.4 Pin Assignment Table

| Port | Pin | Pin Name | Description |
|--------|-----|----------|---|
| Port 0 | 71 | P0[0] | Connected to pin 18 on port E |
| | 72 | P0[1] | Connected to pin 17 on port E |
| | 73 | P0[2] | Connected to pin 16 on port E |
| | 74 | P0[3] | Connected to two points: 1. Voltage reference chip* 2. Connected to pin 15 on port E |
| | 76 | P0[4] | Connected to pin 14 on port E |
| | 77 | P0[5] | Connected to pin 13 on port E |
| | 78 | P0[6] | Connected to pin 12 on port E |
| | 79 | P0[7] | Connected to pin 11 on port E |
| Port 1 | 20 | P1[0] | Connected to three points: 1. Connected to pin 2 on programming header J3 2. Connected to pin 45 on U5 3. Connected to pin 8 (SWDIO) on port D |
| | 21 | P1[1] | Connected to three points: 1. Connected to pin 4 on programming header 2. Connected to pin 56 on U5 3. Connected to pin 7 (SWDCK) on port D |
| | 22 | P1[2] | Connected to pin 6 on port D |
| | 23 | P1[3] | Connected to three points: 1. Connected to pin 6 on programming header 2. Connected to pin 47 on U5 3. Connected to pin 5 (SWO) on port D |
| | 24 | P1[4] | Connected to two points: 1. Connected to pin 8 on programming header 2. Connected to pin 4 (TDI) on port D |
| | 25 | P1[5] | Connected to pin 3 on port D |
| | 27 | P1[6] | Connected to pin 2 on port D |
| | 28 | P1[7] | Connected to pin 1 on port D |

| Port | Pin | Pin Name | Description |
|--------|-----|----------|--|
| Port 2 | 95 | P2[0] | Connected to two points: 1. Connected to LCD module 2. Connected to pin 18 on port D |
| | 96 | P2[1] | Connected to two points: 1. Connected to LCD module 2. Connected to pin 17 on port D |
| | 97 | P2[2] | Connected to two points: 1. Connected to LCD module 2. Connected to pin 16 on port D |
| | 98 | P2[3] | Connected to three points: 1. Connected to pin 2 on trace header J40 2. Connected to LCD module 3. Connected to pin 15 on port D |
| | 99 | P2[4] | Connected to three points: 1. Connected to pin 4 on trace header J40 2. Connected to LCD module 3. Connected to pin 14 on port D |
| | 1 | P2[5] | Connected to three points: 1. Connected to pin 6 on trace header J40 2. Connected to LCD module 3. Connected to pin 13 on port D |
| | 2 | P2[6] | Connected to three points: 1. Connected to pin 8 on trace header J40 2. Connected to LCD module 3. Connected to pin 12 on port D |
| | 3 | P2[7] | Connected to three points: 1. Connected to pin 10 on trace header J40 2. Connected to LCD module 3. Connected to pin 11 on port D |
| Port 3 | 44 | P3[0] | Connected to pin 8 on port E |
| | 45 | P3[1] | Connected to pin 7 on port E |
| | 46 | P3[2] | Connected to two points: 1. Voltage reference chip* 2. Connected to pin 6 on port E |
| | 47 | P3[3] | Connected to pin 5 on port E |
| | 48 | P3[4] | Connected to pin 4 on port E |
| | 49 | P3[5] | Connected to pin 3 on port E |
| | 51 | P3[6] | Connected to pin 2 on port E |
| | 52 | P3[7] | Connected to pin 1 on port E |
| Port 4 | 69 | P4[0] | Connected to pin 28 on port E |
| | 70 | P4[1] | Connected to pin 27 on port E |
| | 80 | P4[2] | Connected to pin 26 on port E |
| | 81 | P4[3] | Connected to pin 25 on port E |
| | 82 | P4[4] | Connected to pin 24 on port E |
| | 83 | P4[5] | Connected to pin 23 on port E |
| | 84 | P4[6] | Connected to pin 22 on port E |
| | 85 | P4[7] | Connected to pin 21 on port E |

| Port | Pin | Pin Name | Description |
|---------|-----|----------|---|
| Port 5 | 16 | P5[0] | Connected to two points: 1. Connected to CapSense slider segment 2. Connected to pin 28 on port D |
| | 17 | P5[1] | Connected to two points: 1. Connected to CapSense slider segment 2. Connected to pin 27 on port D |
| | 18 | P5[2] | Connected to two points: 1. Connected to CapSense slider segment 2. Connected to pin 26 on port D |
| | 19 | P5[3] | Connected to two points: 1. Connected to CapSense slider segment 2. Connected to pin 25 on port D |
| | 31 | P5[4] | Connected to two points: 1. Connected to CapSense slider segment 2. Connected to pin 24 on port D |
| | 32 | P5[5] | Connected to two points: 1. Connected to CapSense button CSB1 2. Connected to pin 23 on port D |
| | 33 | P5[6] | Connected to two points: 1. Connected to CapSense button CSB2 2. Connected to pin 22 on port D |
| | 34 | P5[7] | Connected to pin 21 on port D |
| Port 6 | 89 | P6[0] | Connected to pin 5 on P9 |
| | 90 | P6[1] | Connected to SW2 push button |
| | 91 | P6[2] | Connected to LED3 |
| | 92 | P6[3] | Connected to LED4 |
| | 6 | P6[4] | Connected to CapSense Modulation Capacitor CMOD |
| | 7 | P6[5] | Connected to two points: 1. Connected to VR POT 2. Connected to pin 5 on P6 |
| | 8 | P6[6] | Connected to pin 6 on P9 |
| | 9 | P6[7] | Unused/No Connect |
| Port 12 | 53 | P12[0] | Connected to pin 34 (SCL) on port D and port E |
| | 54 | P12[1] | Connected to pin 33 (SDA) on port D and port E |
| | 67 | P12[2] | Connected to pin 32 on port D and port E |
| | 68 | P12[3] | Connected to pin 31 on port D and port E |
| | 4 | P12[4] | Connected to pin 1 on P9 |
| | 5 | P12[5] | Connected to pin 2 on P9 |
| | 29 | P12[6] | Connected to pin 3 on P9 |
| | 30 | P12[7] | Connected to pin 4 on P9 |
| Port 15 | 42 | P15[0] | Connected to 24-MHz crystal |
| | 43 | P15[1] | Connected to 24-MHz crystal |
| | 55 | P15[2] | Connected to 32-kHz crystal |
| | 56 | P15[3] | Connected to 32-kHz crystal |
| | 93 | P15[4] | Connected to Rbleed resistor |
| | 94 | P15[5] | Connected to SW3 push button |
| | 35 | P15[6] | Connected to USB D+ |
| | 36 | P15[7] | Connected to USB D- |

| Port | Pin | Pin Name | Description |
|------------|-----|-------------------|---|
| Other Pins | 13 | Vbat | Connected to Vbat |
| | 12 | Vboost | Connected to Vboost |
| | 63 | VCCa | Connected to VCCa |
| | 39 | VCCd | Connected to VCCd |
| | 86 | VCCd | Connected to VCCd |
| | 65 | VDDa | Connected to VDDa |
| | 37 | VDDd | Connected to VDDd |
| | 88 | VDDd | Connected to VDDd |
| | 75 | VDDio0 | Connected to VDDio0 |
| | 26 | VDDio1 | Connected to VDDio1 |
| | 100 | VDDio2 | Connected to VDDio2 |
| | 50 | VDDio3 | Connected to VDDio3 |
| | 64 | VSSa | Connected to GND |
| | 10 | VSSb | Connected to GND |
| | 14 | VSSd | Connected to GND |
| | 38 | VSSd | Connected to GND |
| | 66 | VSSd | Connected to GND |
| | 87 | VSSd | Connected to GND |
| | 15 | XRES | Connected to three points: 1. Connected to pin 10 on J3 2. Connected to SW1 3. Connected to pin 20 on U5 |
| | 11 | Ind | Connected to inductor |
| | 40 | NC1 | Unused/No Connect |
| | 41 | NC2 | Unused/No Connect |
| | 57 | NC3 | Unused/No Connect |
| 58 | NC4 | Unused/No Connect | |
| 59 | NC5 | Unused/No Connect | |
| 60 | NC6 | Unused/No Connect | |
| 61 | NC7 | Unused/No Connect | |
| 62 | NC8 | Unused/No Connect | |

Note* To enable voltage reference, populate resistors R34, R37, R73, and low dropout voltage reference IC LM4140. See “[Bill of Materials \(BOM\)](#)” on [page 47](#) for more details of components.

A.5 Using RBLEED Resistor for CapSense

An RBLEED resistor value of 2.2 K provides good SNR values for the onboard CapSense buttons and sliders. However, tuning CapSense with a fixed RBLEED value is difficult because the analog switch divider and scan resolution are the only tunable parameters.

For onboard CapSense buttons and sliders, with RBLEED of 2.2 K, the following SNR is achieved.

| Sensor | Parameter | Value |
|--------------------------|-------------------------|---------|
| Button 0 | Analog Switch Divider | 2 |
| | Scan Resolution | 10 bits |
| | SNR | 74 |
| Button 1 | Analog Switch Divider | 3 |
| | Scan Resolution | 10 bits |
| | SNR | 76 |
| Linear Slider, Element 0 | Analog Switch Divider | 2 |
| | Scan Resolution | 10 bits |
| | SNR (individual sensor) | 85 |
| Linear Slider, Element 1 | Analog Switch Divider | 2 |
| | Scan Resolution | 10 bits |
| | SNR (individual sensor) | 85 |
| Linear Slider, Element 2 | Analog Switch Divider | 2 |
| | Scan Resolution | 10 bits |
| | SNR (individual sensor) | 85 |
| Linear Slider, Element 3 | Analog Switch Divider | 2 |
| | Scan Resolution | 10 bits |
| | SNR (individual sensor) | 85 |
| Linear Slider, Element 4 | Analog Switch Divider | 2 |
| | Scan Resolution | 10 bits |
| | SNR (individual sensor) | 85 |

If RBLEED is used for CapSense, remember the following:

- Use RBLEED only if all IDACs in the device are used for other purposes. IDAC sourcing/sinking method is recommended because it provides better flexibility and automatic tuning feature.
- Use multiple RBLEED resistors if there are different types of sensors in the design. PSoC 3 and PSoC 5 supports up to three RBLEED resistors per channel.
- Use variable resistors for RBLEED, for better tunability.

Revision History



CY8CKIT-030 PSoC® 3 Development Kit Guide Revision History

| Document Title: CY8CKIT-030 PSoC® 3 Development Kit Guide | | | | |
|---|---------|------------|------------------|---|
| Document Number: 001-61038 | | | | |
| Revision | ECN# | Issue Date | Origin of Change | Description of Change |
| ** | 3159150 | 01/06/2011 | QVS | Initial version of kit guide. |
| *A | 3243290 | 04/28/2011 | RKAD | Updated Appendix chapter on page 38 : Updated " Schematics " on page 38. |
| *B | 3475749 | 12/02/2011 | SASH | Updated Appendix chapter on page 38 : Added " Pin Assignment Table " on page 52. Minor content updates across the document. |
| *C | 3607165 | 05/03/2012 | SASH | Updated Introduction chapter on page 5 : Updated " Additional Learning Resources " on page 6: Added " Beginner Resources " on page 6. Added " Engineers Looking for More " on page 6. Added " Learning from Peers " on page 6. |
| *D | 3670374 | 07/09/2012 | SASH | Updated Getting Started chapter on page 9 : Updated " DVD Installation " on page 9: Updated description. Updated Code Examples chapter on page 30 : Updated Figure 5-1 . |
| *E | 3737318 | 09/07/2012 | SASH | Updated images across the document. |
| *F | 3857898 | 01/03/2013 | SASH | Updated Introduction chapter on page 5 : Updated " Additional Learning Resources " on page 6: Added " More Code Examples " on page 6. Updated Appendix chapter on page 38 : Added " Using RBLEED Resistor for CapSense " on page 56. |
| *G | 4069046 | 02/28/2013 | SASH | Updated Getting Started chapter on page 9 : Updated " DVD Installation " on page 9: Updated Figure 2-1 . Updated Code Examples chapter on page 30 : Updated Figure 5-1 . Minor content updates across the document (for PSoC Creator 2.2). |

CY8CKIT-030 PSoC® 3 Development Kit Guide Revision History (continued)

| Document Title: CY8CKIT-030 PSoC® 3 Development Kit Guide | | | | |
|---|---------|------------|------------------|--|
| Document Number: 001-61038 | | | | |
| Revision | ECN# | Issue Date | Origin of Change | Description of Change |
| *H | 4131903 | 09/23/2013 | SASH | Updated Kit Operation chapter on page 11: Updated " Programming PSoC 3 Device " on page 11: Updated description (Added programming steps). Updated PSoC Creator images across the document. |
| *I | 4241192 | 01/09/2014 | RKAD | No technical updates. Completing Sunset Review. |
| *J | 5613735 | 02/01/2017 | RKAD | Updated to new template. Completing Sunset Review. |